



# 128Kx8 MONOLITHIC SRAM, SMD 5962-96691

## FEATURES

- Access Times 70, 85, 100, 120ns
- Revolutionary, Center Power/Ground Pinout JEDEC Approved
  - 32 lead Ceramic SOJ (Package 101)
- Evolutionary, Corner Power/Ground Pinout JEDEC Approved
  - 32 pin Ceramic DIP (Package 300)
  - 32 lead Ceramic SOJ (Package 101)
  - 32 lead Ceramic Flat Pack (Package 206)
- MIL-STD-883 Compliant Devices Available
- Commercial, Industrial and Military Temperature Range
- 5 Volt Power Supply
- Low Power CMOS
- 2V Data Retention Devices Available (Low Power Version)
- TTL Compatible Inputs and Outputs

### REVOLUTIONARY PINOUT

32 CSOJ (DR)

#### TOP VIEW

|                 |    |    |                 |
|-----------------|----|----|-----------------|
| A0              | 1  | 32 | A16             |
| A1              | 2  | 31 | A15             |
| A2              | 3  | 30 | A14             |
| A3              | 4  | 29 | A13             |
| $\overline{CS}$ | 5  | 28 | $\overline{OE}$ |
| I/O1            | 6  | 27 | I/O8            |
| I/O2            | 7  | 26 | I/O7            |
| Vcc             | 8  | 25 | GND             |
| GND             | 9  | 24 | Vcc             |
| I/O3            | 10 | 23 | I/O6            |
| I/O4            | 11 | 22 | I/O5            |
| $\overline{WE}$ | 12 | 21 | A12             |
| A4              | 13 | 20 | A11             |
| A5              | 14 | 19 | A10             |
| A6              | 15 | 18 | A9              |
| A7              | 16 | 17 | A8              |

### EVOLUTIONARY PINOUT

32 DIP (C)  
32 CSOJ (DE)  
32 FLATPACK (FE)

#### TOP VIEW

|      |    |    |                 |
|------|----|----|-----------------|
| NC   | 1  | 32 | Vcc             |
| A16  | 2  | 31 | A15             |
| A14  | 3  | 30 | NC              |
| A12  | 4  | 29 | $\overline{WE}$ |
| A7   | 5  | 28 | A13             |
| A6   | 6  | 27 | A8              |
| A5   | 7  | 26 | A9              |
| A4   | 8  | 25 | A11             |
| A3   | 9  | 24 | $\overline{OE}$ |
| A2   | 10 | 23 | A10             |
| A1   | 11 | 22 | $\overline{CS}$ |
| A0   | 12 | 21 | I/O7            |
| I/O0 | 13 | 20 | I/O6            |
| I/O1 | 14 | 19 | I/O5            |
| I/O2 | 15 | 18 | I/O4            |
| GND  | 16 | 17 | I/O3            |

### PIN DESCRIPTION

|                 |                   |
|-----------------|-------------------|
| A0-16           | Address Inputs    |
| I/O0-7          | Data Input/Output |
| $\overline{CS}$ | Chip Select       |
| $\overline{OE}$ | Output Enable     |
| $\overline{WE}$ | Write Enable      |
| Vcc             | +5.0V Power       |
| GND             | Ground            |



**ABSOLUTE MAXIMUM RATINGS**

| Parameter                      | Symbol           | Min  | Max                  | Unit |
|--------------------------------|------------------|------|----------------------|------|
| Operating Temperature          | T <sub>A</sub>   | -55  | +125                 | °C   |
| Storage Temperature            | T <sub>STG</sub> | -65  | +150                 | °C   |
| Signal Voltage Relative to GND | V <sub>G</sub>   | -0.5 | V <sub>CC</sub> +0.5 | V    |
| Junction Temperature           | T <sub>J</sub>   |      | 150                  | °C   |
| Supply Voltage                 | V <sub>CC</sub>  | -0.5 | 7.0                  | V    |

**TRUTH TABLE**

| $\overline{CS}$ | $\overline{OE}$ | $\overline{WE}$ | Mode        | Data I/O | Power   |
|-----------------|-----------------|-----------------|-------------|----------|---------|
| H               | X               | X               | Standby     | High Z   | Standby |
| L               | L               | H               | Read        | Data Out | Active  |
| L               | H               | H               | Out Disable | High Z   | Active  |
| L               | X               | L               | Write       | Data In  | Active  |

**RECOMMENDED OPERATING CONDITIONS**

| Parameter          | Symbol          | Min  | Max                   | Unit |
|--------------------|-----------------|------|-----------------------|------|
| Supply Voltage     | V <sub>CC</sub> | 4.5  | 5.5                   | V    |
| Input High Voltage | V <sub>IH</sub> | 2.2  | V <sub>CC</sub> + 0.3 | V    |
| Input Low Voltage  | V <sub>IL</sub> | -0.5 | +0.8                  | V    |

**CAPACITANCE  
(TA = +25°C)**

| Parameter          | Symbol           | Condition                         | Package                                     | Max | Unit |
|--------------------|------------------|-----------------------------------|---|-----|------|
| Input capacitance  | C <sub>IN</sub>  | V <sub>IN</sub> = 0V, f = 1.0MHz  | 32 Pin CSOJ, DIP,<br>Flat Pack Evolutionary | 12  | pF   |
|                    |                  |                                   | 32 Pin CSOJ Revolutionary                   | 20  | pF   |
| Output capacitance | C <sub>OUT</sub> | V <sub>OUT</sub> = 0V, f = 1.0MHz | 32 Pin CSOJ, DIP,<br>Flat Pack Evolutionary | 12  | pF   |
|                    |                  |                                   | 32 Pin CSOJ Revolutionary                   | 20  | pF   |

*This parameter is guaranteed by design but not tested.*

**DC CHARACTERISTICS  
(VCC = 5.0V, GND = 0V, TA = -55°C TO +125°C)**

| Parameter                | Sym             | Conditions   | -70 |     | -85 |     | -100 |     | -120 |     | Units |
|--------------------------|-----------------|--|-----|-----|-----|-----|------|-----|------|-----|-------|
|                          |                 |  | Min | Max | Min | Max | Min  | Max | Min  | Max |       |
| Input Leakage Current    | I <sub>LI</sub> | V <sub>CC</sub> = 5.5, V <sub>IN</sub> = GND to V <sub>CC</sub>                    |     | 10  |     | 10  |      | 10  |      | 10  | μA    |
| Output Leakage Current   | I <sub>LO</sub> | $\overline{CS} = V_{IH}, \overline{OE} = V_{IH}, V_{OUT} = GND \text{ to } V_{CC}$ |     | 10  |     | 10  |      | 10  |      | 10  | μA    |
| Operating Supply Current | I <sub>CC</sub> | $\overline{CS} = V_{IH}, \overline{OE} = V_{IH}, f = 5\text{MHz}, V_{CC} = 5.5$    |     | 30  |     | 30  |      | 30  |      | 30  | mA    |
| Standby Current          | I <sub>SB</sub> | $\overline{CS} = V_{IH}, \overline{OE} = V_{IH}, f = 5\text{MHz}, V_{CC} = 5.5$    |     | 5   |     | 5   |      | 5   |      | 5   | mA    |
| Output Low Voltage       | V <sub>OL</sub> | I <sub>OL</sub> = 2.1mA, V <sub>CC</sub> = 4.5                                     |     | 0.4 |     | 0.4 |      | 0.4 |      | 0.4 | V     |
| Output High Voltage      | V <sub>OH</sub> | I <sub>OH</sub> = -1.0mA, V <sub>CC</sub> = 4.5                                    | 2.4 |     | 2.4 |     | 2.4  |     | 2.4  |     | V     |

NOTE: DC test conditions: V<sub>IH</sub> = V<sub>CC</sub> - 0.3V, V<sub>IL</sub> = 0.3V

**DATA RETENTION CHARACTERISTICS  
(TA = -55°C TO +125°C)**

| Parameter                     | Symbol             | Conditions                         | -70 |     | -85 |     | -100 |     | -120 |     | Units |
|-------------------------------|--------------------|------------------------------------|-----|-----|-----|-----|------|-----|------|-----|-------|
|                               |                    |                                    | Min | Max | Min | Max | Min  | Max | Min  | Max |       |
| Data Retention Supply Voltage | V <sub>DR</sub>    | $\overline{CS} \geq V_{CC} - 0.2V$ | 2.0 | 5.5 | 2.0 | 5.5 | 2.0  | 5.5 | 2.0  | 5.5 | V     |
| Data Retention Current        | I <sub>CCDR1</sub> | V <sub>CC</sub> = 3V               |     | 1   |     | 1   |      | 1   |      | 1   | mA    |



**AC CHARACTERISTICS**  
(VCC = 5.0V, TA = -55°C To +125°C)

| Parameter                          | Symbol                        | -70 |     | -85 |     | -100 |     | -120 |     | Units |
|------------------------------------|-------------------------------|-----|-----|-----|-----|------|-----|------|-----|-------|
|                                    |                               | Min | Max | Min | Max | Min  | Max | Min  | Max |       |
| Read Cycle                         |                               |     |     |     |     |      |     |      |     |       |
| Read Cycle Time                    | t <sub>RC</sub>               | 70  |     | 85  |     | 100  |     | 120  |     | ns    |
| Address Access Time                | t <sub>AA</sub>               |     | 70  |     | 85  |      | 100 |      | 120 | ns    |
| Output Hold from Address Change    | t <sub>OH</sub>               | 3   |     | 3   |     | 3    |     | 3    |     | ns    |
| Chip Select Access Time            | t <sub>ACS</sub>              |     | 70  |     | 85  |      | 100 |      | 120 | ns    |
| Output Enable to Output Valid      | t <sub>OE</sub>               |     | 35  |     | 45  |      | 50  |      | 60  | ns    |
| Chip Select to Output in Low Z     | t <sub>CLZ</sub> <sup>1</sup> | 3   |     | 3   |     | 3    |     | 3    |     | ns    |
| Output Enable to Output in Low Z   | t <sub>OLZ</sub> <sup>1</sup> | 0   |     | 0   |     | 0    |     | 0    |     | ns    |
| Chip Disable to Output in High Z   | t <sub>CHZ</sub> <sup>1</sup> |     | 25  |     | 25  |      | 35  |      | 35  | ns    |
| Output Disable to Output in High Z | t <sub>OHZ</sub> <sup>1</sup> |     | 25  |     | 25  |      | 35  |      | 35  | ns    |

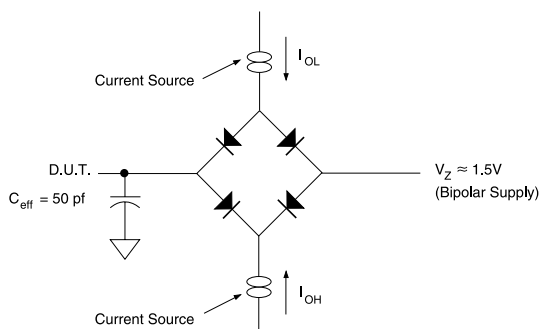
1. This parameter is guaranteed by design but not tested.

**AC CHARACTERISTICS**  
(VCC = 5.0V, TA = -55°C To +125°C)

| Parameter                        | Symbol                        | -70 |     | -85 |     | -100 |     | -120 |     | Units |
|----------------------------------|-------------------------------|-----|-----|-----|-----|------|-----|------|-----|-------|
|                                  |                               | Min | Max | Min | Max | Min  | Max | Min  | Max |       |
| Write Cycle                      |                               |     |     |     |     |      |     |      |     |       |
| Write Cycle Time                 | t <sub>WC</sub>               | 70  |     | 85  |     | 100  |     | 120  |     | ns    |
| Chip Select to End of Write      | t <sub>CW</sub>               | 60  |     | 75  |     | 80   |     | 100  |     | ns    |
| Address Valid to End of Write    | t <sub>AW</sub>               | 60  |     | 75  |     | 80   |     | 100  |     | ns    |
| Data Valid to End of Write       | t <sub>DW</sub>               | 30  |     | 35  |     | 40   |     | 50   |     | ns    |
| Write Pulse Width                | t <sub>WP</sub>               | 50  |     | 55  |     | 70   |     | 80   |     | ns    |
| Address Setup Time               | t <sub>AS</sub>               | 0   |     | 0   |     | 0    |     | 0    |     | ns    |
| Address Hold Time                | t <sub>AH</sub>               | 5   |     | 5   |     | 5    |     | 5    |     | ns    |
| Output Active from End of Write  | t <sub>OW</sub> <sup>1</sup>  | 5   |     | 5   |     | 5    |     | 5    |     | ns    |
| Write Enable to Output in High Z | t <sub>WHZ</sub> <sup>1</sup> |     | 25  |     | 30  |      | 35  |      | 35  | ns    |
| Data Hold Time                   | t <sub>DH</sub>               | 0   |     | 0   |     | 0    |     | 0    |     | ns    |

1. This parameter is guaranteed by design but not tested.

**AC TEST CIRCUIT**



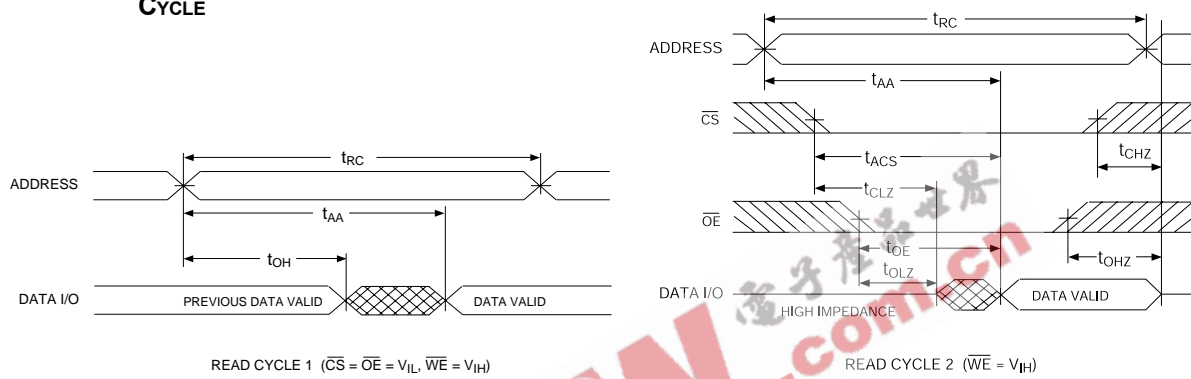
**AC TEST CONDITIONS**

| Parameter                        | Typ                        | Unit |
|----------------------------------|----------------------------|------|
| Input Pulse Levels               | $V_{IL} = 0, V_{IH} = 3.0$ | V    |
| Input Rise and Fall              | 5                          | ns   |
| Input and Output Reference Level | 1.5                        | V    |
| Output Timing Reference Level    | 1.5                        | V    |

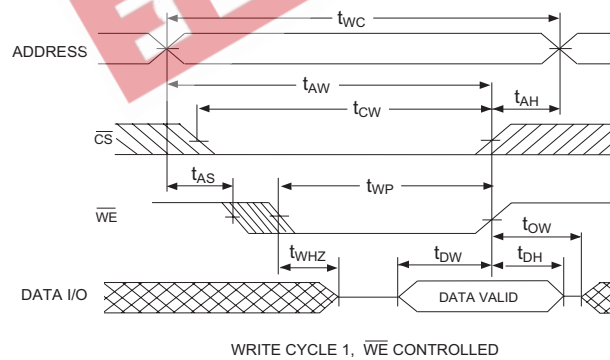
Notes:  
 $V_Z$  is programmable from -2V to +7V.  
 $I_{OL}$  &  $I_{OH}$  programmable from 0 to 16mA.  
 Tester Impedance  $Z_0 = 75\Omega$ .  
 $V_Z$  is typically the midpoint of  $V_{OH}$  and  $V_{OL}$ .  
 $I_{OL}$  &  $I_{OH}$  are adjusted to simulate a typical resistive load circuit.  
 ATE tester includes jig capacitance.



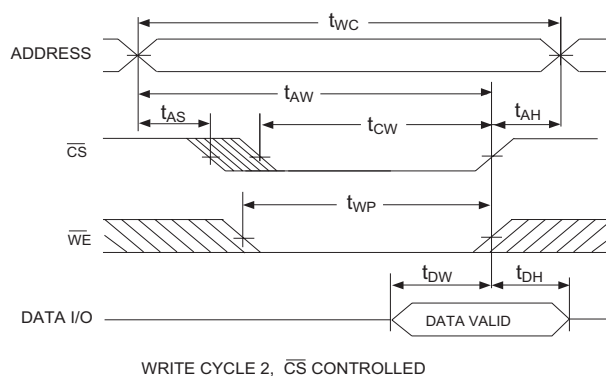
**TIMING WAVEFORM - READ CYCLE**



**WRITE CYCLE -  $\overline{WE}$  CONTROLLED**

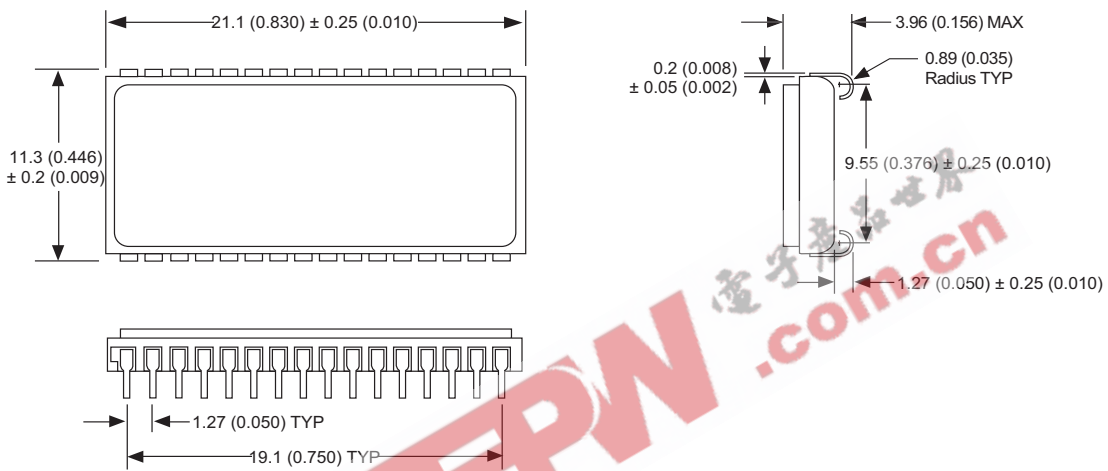


**WRITE CYCLE -  $\overline{CS}$  CONTROLLED**



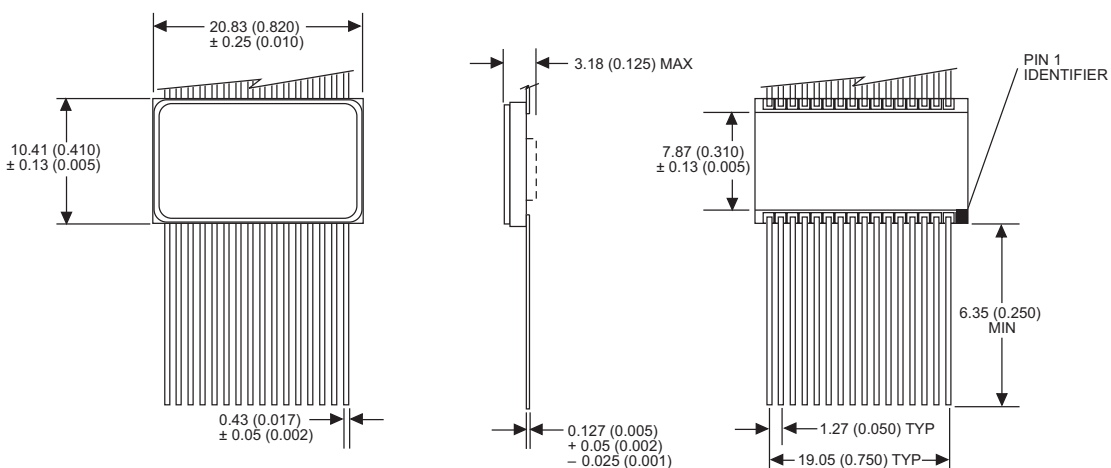


**PACKAGE 101: 32 LEAD, CERAMIC SOJ**



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

**PACKAGE 206: 32 LEAD, CERAMIC FLAT PACK**



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES



**PACKAGE 300: 32 PIN, CERAMIC DIP, SINGLE CAVITY SIDE BRAZED**



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES



**DATA RETENTION CHARACTERISTICS**  
**(TA = -55°C TO +125°C)**  
**LOW POWER VERSION ONLY**

| Parameter                     | Symbol | Conditions                         |     |     | Units   |
|-------------------------------|--------|------------------------------------|-----|-----|---------|
|                               |        |                                    | Min | Max |         |
| Data Retention Supply Voltage | VDR    | $\overline{CS} \geq V_{CC} - 0.2V$ | 2.0 | 5.5 | V       |
| Data Retention Current        | ICCDR3 | VCC = 2V                           |     | 750 | $\mu A$ |

**ORDERING INFORMATION**

W M S 128K 8 X - XXX X X X

**LEAD FINISH:**

- Blank = Gold plated leads
- A = Solder clip leads

**DEVICE GRADE:**

- M = Military Screened -55°C to +125°C
- I = Industrial -40°C to +85°C
- C = Commercial 0°C to +70°C

**PACKAGE:**

- C = 32 Pin Ceramic .600" DIP (Package 300)
- DE = 32 Lead Ceramic SOJ (Package 101) Evolutionary
- DR = 32 Lead Ceramic SOJ (Package 101) Revolutionary
- FE = 32 Lead Ceramic Flat Pack (Package 206)

**ACCESS TIME (ns)**

**IMPROVEMENT MARK**

- L = Low Power for 2V Data Retention

**ORGANIZATION, 128Kx8**

**SRAM**

**MONOLITHIC**

**WHITE ELECTRONIC DESIGNS CORP.**



| DEVICE TYPE              | SPEED | PACKAGE                | SMD NO.          |
|--------------------------|-------|------------------------|------------------|
| 128K x 8 SRAM Monolithic | 120ns | 32 lead SOJ Revol (DR) | 5962-96691 01HUX |
| 128K x 8 SRAM Monolithic | 100ns | 32 lead SOJ Revol (DR) | 5962-96691 02HUX |
| 128K x 8 SRAM Monolithic | 85ns  | 32 lead SOJ Revol (DR) | 5962-96691 03HUX |
| 128K x 8 SRAM Monolithic | 70ns  | 32 lead SOJ Revol (DR) | 5962-96691 04HUX |
| 128K x 8 SRAM Monolithic | 120ns | 32 lead SOJ Evol (DE)  | 5962-96691 01HTX |
| 128K x 8 SRAM Monolithic | 100ns | 32 lead SOJ Evol (DE)  | 5962-96691 02HTX |
| 128K x 8 SRAM Monolithic | 85ns  | 32 lead SOJ Evol (DE)  | 5962-96691 03HTX |
| 128K x 8 SRAM Monolithic | 70ns  | 32 lead SOJ Evol (DE)  | 5962-96691 04HTX |
| 128K x 8 SRAM Monolithic | 120ns | 32 pin DIP (C)         | 5962-96691 01HYX |
| 128K x 8 SRAM Monolithic | 100ns | 32 pin DIP (C)         | 5962-96691 02HYX |
| 128K x 8 SRAM Monolithic | 85ns  | 32 pin DIP (C)         | 5962-96691 03HYX |
| 128K x 8 SRAM Monolithic | 70ns  | 32 pin DIP (C)         | 5962-96691 04HYX |
| 128K x 8 SRAM Monolithic | 120ns | 32 pin Flatpack (FE)   | 5962-96691 01HNX |
| 128K x 8 SRAM Monolithic | 100ns | 32 pin Flatpack (FE)   | 5962-96691 02HNX |
| 128K x 8 SRAM Monolithic | 85ns  | 32 pin Flatpack (FE)   | 5962-96691 03HNX |
| 128K x 8 SRAM Monolithic | 70ns  | 32 pin Flatpack (FE)   | 5962-96691 04HNX |