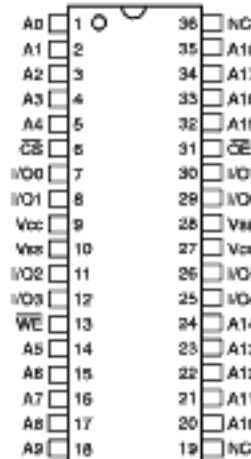




### 512Kx8 SRAM

PRELIMINARY \*

#### PIN CONFIGURATION TOP VIEW



#### PIN DESCRIPTION

A0-13	Address Inputs
I/O0-7	Data Input/Output
CS	Chip Select
OE	Output Enable
WE	Write Enable
Vcc	+5.0V Power
Vss	Ground
NC	No Connect

#### PLASTIC PLUS™ FEATURES

- Access Times of 15, 20, 25ns
- Standard Commercial Off-The-Shelf (COTS) Memory Devices for Extended Temperature Range
- JEDEC Standard 36 pin Plastic SOJ Package
- Electrical and Speed Characteristics for:
  - Military Temperature (-55°C to +125°C)
  - Industrial Temperature (-40°C to +85°C)
- Burn-in and Temperature Cycling Available
- Organized as 512K x 8
- Center Power/Ground Pins (Revolutionary)
- 5 Volt Power Supply
- Low Power (L) Version Available
- Battery Back-Up Operation
- Reliability Test Data Available:
  - High Temperature Operating Life
  - High Temperature Storage
  - Pressure Cooker Test
  - Wet High Temperature Operating Life
  - Thermal Shock
  - Temperature Cycling

\* This data sheet describes a product under development, not fully characterized, and is subject to change without notice.



**ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Min	Max	Unit
Operating Temperature (Mil.)	T <sub>A</sub>	-55	+125	°C
Operating Temperature (Ind.)	T <sub>A</sub>	-40	+85	°C
Storage Temperature	T <sub>STG</sub>	-65	+150	°C
Signal Voltage Relative to V <sub>SS</sub>	V <sub>G</sub>	-0.5	V <sub>CC</sub> + 0.5	V
Supply Voltage	V <sub>CC</sub>	-0.5	7.0	V

**TRUTH TABLE**

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	V <sub>CC</sub> Current
H	X	X	Power Down	High-Z	I <sub>SB</sub>
L	H	H	Out Disable	High-Z	I <sub>CC</sub>
L	H	L	Read	D <sub>OUT</sub>	I <sub>CC</sub>
L	L	X	Write	D <sub>IN</sub>	I <sub>CC</sub>

**RECOMMENDED OPERATING CONDITIONS**

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V <sub>CC</sub>	4.5	5.5	V
Input High Voltage	V <sub>IH</sub>	2.2	V <sub>CC</sub> + 0.5	V
Input Low Voltage	V <sub>IL</sub>	-0.3	+0.8	V
Operating Temperature (Mil.)	T <sub>A</sub>	-55	+125	°C
Operating Temperature (Ind.)	T <sub>A</sub>	-40	+85	°C

**CAPACITANCE**

(T<sub>A</sub> = +25°C)

Parameter	Symbol	Condition	Max	Unit
Input capacitance	C <sub>IN</sub>	V <sub>IN</sub> = 0V, f = 1.0MHz	6	pF
Output capacitance	C <sub>OUT</sub>	V <sub>OUT</sub> = 0V, f = 1.0MHz	8	pF

This parameter is guaranteed by design but not tested.

**DC CHARACTERISTICS**

(V<sub>CC</sub> = 5V, V<sub>SS</sub> = 0V, T<sub>A</sub> = -55°C to +125°C)

Parameter	Symbol	Conditions	Min		Max		Units
Input Leakage Current	I <sub>LI</sub>	V <sub>CC</sub> = 5.5, V <sub>IN</sub> = V <sub>SS</sub> to V <sub>CC</sub>			10		μA
Output Leakage Current	I <sub>LO</sub>	$\overline{CS} = V_{IH}, \overline{OE} = V_{IH}, V_{OUT} = V_{SS} \text{ to } V_{CC}$			10		μA
Operating Supply Current	I <sub>CC</sub>	$\overline{CS} = V_{IL}, \overline{OE} = V_{IH}, f = 5\text{MHz}, V_{CC} = 5.5$			180		mA
Standby Current	I <sub>SB</sub>	$\overline{CS} = V_{IH}, \overline{OE} = V_{IH}, f = 5\text{MHz}, V_{CC} = 5.5$			15		mA
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 8.0mA, V <sub>CC</sub> = 4.5			0.4		V
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -4.0mA, V <sub>CC</sub> = 4.5	2.4				V

NOTE: DC test conditions: V<sub>IL</sub> = 0.3V, V<sub>IH</sub> = V<sub>CC</sub> - 0.3V

**DATA RETENTION CHARACTERISTICS**

(T<sub>A</sub> = -55°C to +125°C)

Parameter	Symbol	Conditions	Min			Units
			Min	Typ	Max	
Data Retention Supply Voltage	V <sub>DR</sub>	$\overline{CS} \geq V_{CC} - 0.2V$	2.0		5.5	V
Data Retention Current	I <sub>CCDR1</sub>	V <sub>CC</sub> = 3V		0.5	8	mA
Low Power Data Retention (L)	I <sub>CCDR1</sub>	V <sub>CC</sub> = 3V		300	800	μA

**AC CHARACTERISTICS**

(Vcc = 5.0V, Vss = 0V, TA = -55°C to +125°C)

Parameter	Symbol	-15*		-20		-25		Units
		Min	Max	Min	Max	Min	Max	
Read Cycle								
Read Cycle Time	t <sub>RC</sub>	15		20		25		ns
Address Access Time	t <sub>AA</sub>		15		20		25	ns
Output Hold from Address Change	t <sub>OH</sub>	0		0		0		ns
Chip Select Access Time	t <sub>ACS</sub>		15		20		25	ns
Output Enable to Output Valid	t <sub>OE</sub>		8		10		12	ns
Chip Select to Output in Low Z	t <sub>CLZ'</sub>	3		3		3		ns
Output Enable to Output in Low Z	t <sub>OLZ'</sub>	0		0		0		ns
Chip Disable to Output in High Z	t <sub>CHZ'</sub>		7		8		10	ns
Output Disable to Output in High Z	t <sub>OHZ'</sub>		7		8		10	ns

\* 15ns not available in the lower power option.

1. This parameter is guaranteed by design but not tested.

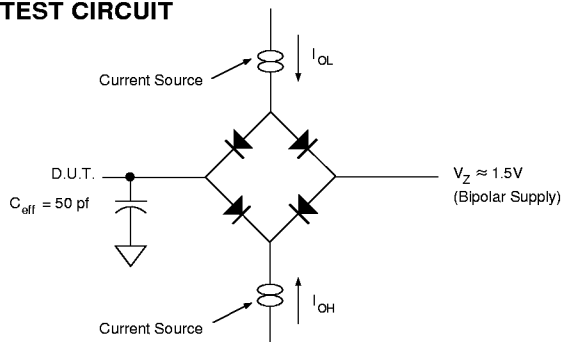
**AC CHARACTERISTICS**

(Vcc = 5.0V, TA = -55°C to +125°C)

Parameter	Symbol	-15*		-20		-25		Units
		Min	Max	Min	Max	Min	Max	
Write Cycle								
Write Cycle Time	t <sub>WC</sub>	15		20		25		ns
Chip Select to End of Write	t <sub>CW</sub>	12		13		15		ns
Address Valid to End of Write	t <sub>AW</sub>	12		13		15		ns
Data Valid to End of Write	t <sub>DW</sub>	8		9		10		ns
Write Pulse Width	t <sub>WP</sub>	12		13		15		ns
Address Setup Time	t <sub>AS</sub>	0		0		0		ns
Address Hold Time	t <sub>AH</sub>	0		0		0		ns
Output Active from End of Write	t <sub>OW'</sub>	0		0		0		ns
Write Enable to Output in High Z	t <sub>WHZ'</sub>		8		8		10	ns
Data Hold Time	t <sub>DH</sub>	0		0		0		ns

\* 15ns not available in the lower power option.

1. This parameter is guaranteed by design but not tested.

**AC TEST CIRCUIT****AC TEST CONDITIONS**

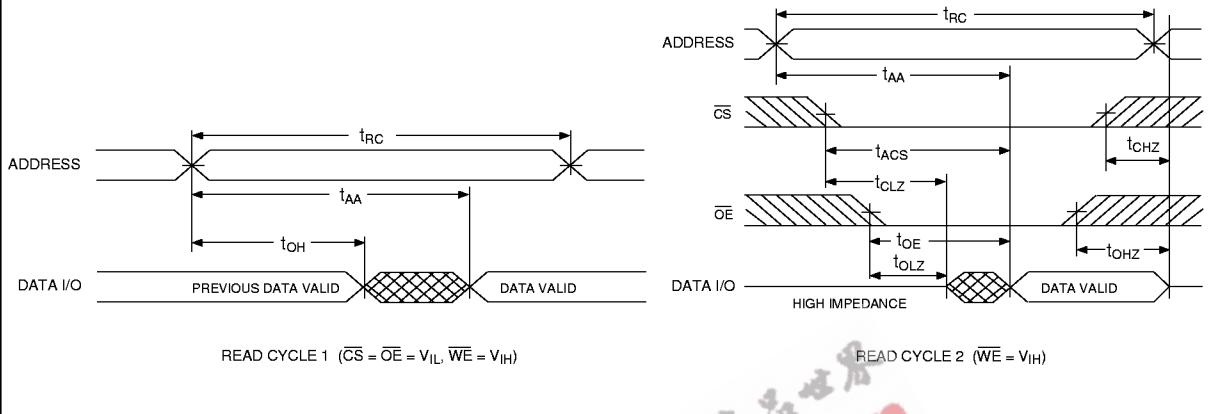
Parameter	Typ	Unit
Input Pulse Levels	V <sub>IL</sub> = 0, V <sub>IH</sub> = 3.0	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

**NOTES:**V<sub>Z</sub> is programmable from -2V to +7V.I<sub>OL</sub> & I<sub>OH</sub> programmable from 0 to 16mA.Tester Impedance Z<sub>0</sub> = 75 Ω.V<sub>Z</sub> is typically the midpoint of V<sub>OH</sub> and V<sub>OL</sub>.I<sub>OL</sub> & I<sub>OH</sub> are adjusted to simulate a typical resistive load circuit.

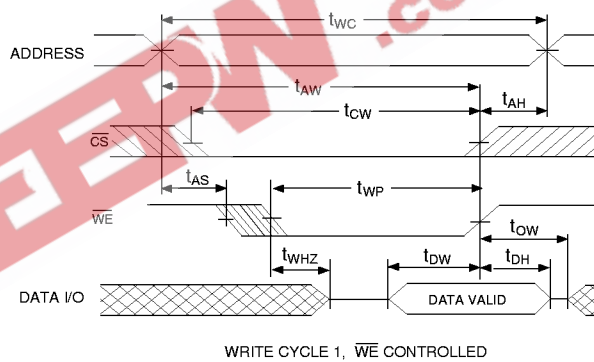
ATE tester includes jig capacitance.



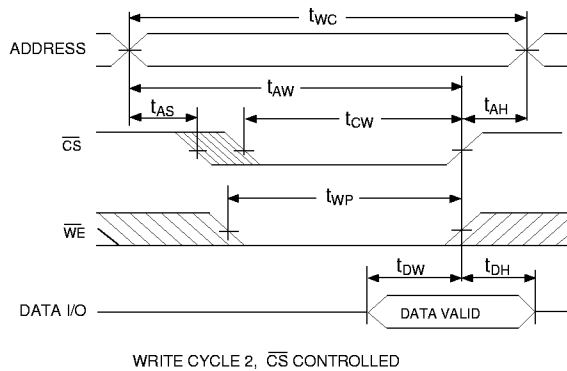
TIMING WAVEFORM - READ CYCLE



WRITE CYCLE -  $\overline{WE}$  CONTROLLED

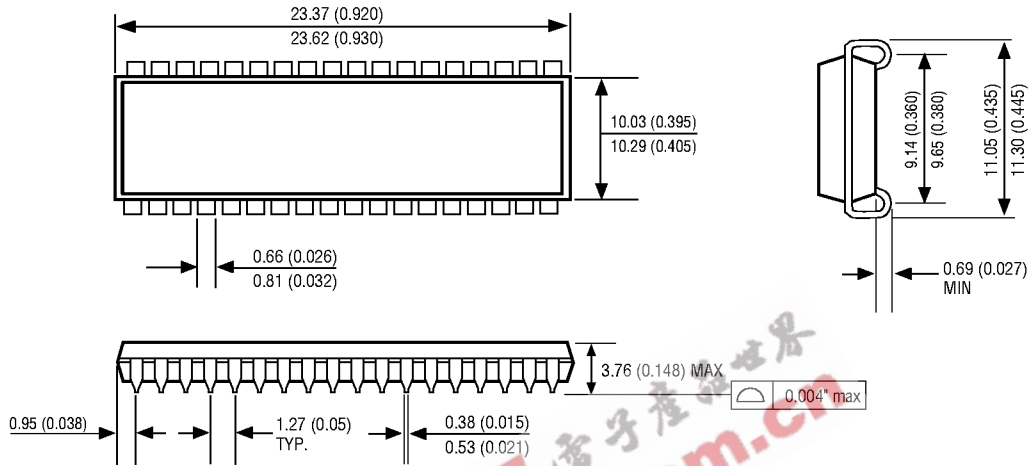


WRITE CYCLE -  $\overline{CS}$  CONTROLLED





PACKAGE DIMENSION



DIMENSIONS IN MILLIMETERS AND (INCHES)

ORDERING INFORMATION

W P S 512K 8 X X - XXX R J X X

SPECIAL PROCESS:

- Blank = CMOS
- B = Bi CMOS

DEVICE GRADE:

- M = Military Temperature -55°C to +125°C
- I = Industrial Temperature -40°C to +85°C

PACKAGE:

- RJ = Revolutionary SOJ

ACCESS TIME (ns)

IMPROVEMENT MARK

- B = Burn-in
- T = Temperature Cycling
- C = Burn-in and Temperature Cycle

Blank = Standard Power

L = Low Power

ORGANIZATION, 512K x 8

SRAM

PLASTIC PLUS™

WHITE MICROELECTRONICS