

STC X0205MN

Sensitive Gate

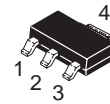
Silicon Controlled Rectifier

Reverse Blocking Thyristor

PNPN device designed for line-powered general purpose applications such as relay and lamp drivers, small motor controls, gate drivers for larger thyristors, and sensing and detection circuits. Supplied in a cost effective plastic SOT-223 package.

- Sensitive Gate Allows Direct Triggering by Microcontrollers and Other Logic Circuits
- On-State Current Rating of 1.25 Amperes RMS at 80°C
- Surge Current Capability – 20 Amperes
- Immunity to dV/dt – 20 V/ μ sec Minimum at 110°C
- Glass-Passivated Surface for Reliability and Uniformity
- Blocking Voltage to 600 Volts

SCR
1.25 AMPERES RMS
600 VOLTS



MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Peak Repetitive Off-State Voltage (Note 1.) ($T_J = -40$ to 110°C , Sine Wave, 50 to 60 Hz; Gate Open)	V_{DRM} , V_{RRM}	600	Volts
On-State RMS Current ($T_C = 80^\circ\text{C}$) 180° Conduction Angles	$I_{T(RMS)}$	1.25	Amp
Peak Non-Repetitive Surge Current (1/2 Cycle, Sine Wave, 60 Hz, $T_J = 25^\circ\text{C}$)	I_{TSM}	20	Amps
Circuit Fusing Consideration ($t = 10$ ms)	I^2t	0.415	A^2s
Forward Peak Gate Power ($T_A = 25^\circ\text{C}$, Pulse Width ≤ 1.0 μs)	P_{GM}	0.1	Watt
Forward Average Gate Power ($T_A = 25^\circ\text{C}$, $t = 20$ ms)	$P_{G(AV)}$	0.20	Watt
Forward Peak Gate Current ($T_A = 25^\circ\text{C}$, Pulse Width ≤ 1.0 μs)	I_{GM}	1.2	Amp
Reverse Peak Gate Voltage ($T_A = 25^\circ\text{C}$, Pulse Width ≤ 1.0 μs)	V_{GRM}	5.0	Volts
Operating Junction Temperature Range @ Rate V_{RRM} and V_{DRM}	T_J	-40 to 110	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-40 to 150	$^\circ\text{C}$

SOT-223

PIN ASSIGNMENT	
1	Cathode
2	Anode
3	Gate
4	Anode

(1) V_{DRM} and V_{RRM} for all types can be applied on a continuous basis. Ratings apply for zero or negative gate voltage; however, positive gate voltage shall not be applied concurrent with negative potential on the anode. Blocking voltages shall not be tested with a constant source such that the voltage ratings of the devices are exceeded.

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THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance – Junction to Case – Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	75 200	$^{\circ}C/W$
Lead Solder Temperature ($< 1/16''$ from case, 10 secs max)	T_L	260	$^{\circ}C$

ELECTRICAL CHARACTERISTICS ($T_C = 25^{\circ}C$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Peak Repetitive Forward or Reverse Blocking Current (Note 1.) ($V_D = \text{Rated } V_{DRM}$ and V_{RRM} ; $R_{GK} = 1.0 \text{ k}\Omega$)	I_{DRM}, I_{RRM}	– –	– –	10 0.1	μA mA
	$T_C = 25^{\circ}C$ $T_C = 110^{\circ}C$				

ON CHARACTERISTICS

Peak Forward On-State Voltage ^(*) ($I_{TM} = 1.0 \text{ Amp Peak @ } T_A = 25^{\circ}C$)	V_{TM}	–	–	1.7	Volts
Gate Trigger Current (Continuous dc) (Note 2.) ($V_{AK} = 12 \text{ V}, R_L = 100 \text{ Ohms}$)	I_{GT}	–	8	20	μA
Holding Current (Note 2.) ($V_{AK} = 12 \text{ V}, I_{GT} = 0.5 \text{ mA}$)	I_H	– –	0.5 –	5.0 10	mA
Latch Current ($V_{AK} = 12 \text{ V}, I_{GT} = 0.5 \text{ mA}, R_{GK} = 1.0 \text{ k}$)	I_L	– –	0.6 –	10 15	mA
Gate Trigger Voltage (Continuous dc) (Note 2.) ($V_{AK} = 12 \text{ V}, R_L = 100 \text{ Ohms}, I_{GT} = 10 \text{ mA}$)	V_{GT}	–	0.62	0.8 1.2	Volts
	$T_C = 25^{\circ}C$ $T_C = -40^{\circ}C$				

DYNAMIC CHARACTERISTICS

Critical Rate of Rise of Off-State Voltage ($V_D = \text{Rated } V_{DRM}$, Exponential Waveform, $R_{GK} = 1000 \text{ Ohms}$, $T_J = 110^{\circ}C$)	dV/dt	20	35	–	V/ μs
Critical Rate of Rise of On-State Current ($I_{PK} = 20 \text{ A}; P_w = 10 \mu sec; di/dt = 1.0 \text{ A}/\mu sec, I_{gt} = 20 \text{ mA}$)	di/dt	–	–	50	A/ μs

*Indicates Pulse Test: Pulse Width $\leq 1.0 \text{ ms}$, Duty Cycle $\leq 1\%$.

1. $R_{GK} = 1000 \text{ Ohms}$ included in measurement.
2. Does not include R_{GK} in measurement.

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Voltage Current Characteristic of SCR

Symbol	Parameter
V_{DRM}	Peak Repetitive Off State Forward Voltage
I_{DRM}	Peak Forward Blocking Current
V_{RRM}	Peak Repetitive Off State Reverse Voltage
I_{RRM}	Peak Reverse Blocking Current
V_{TM}	Peak on State Voltage
I_H	Holding Current

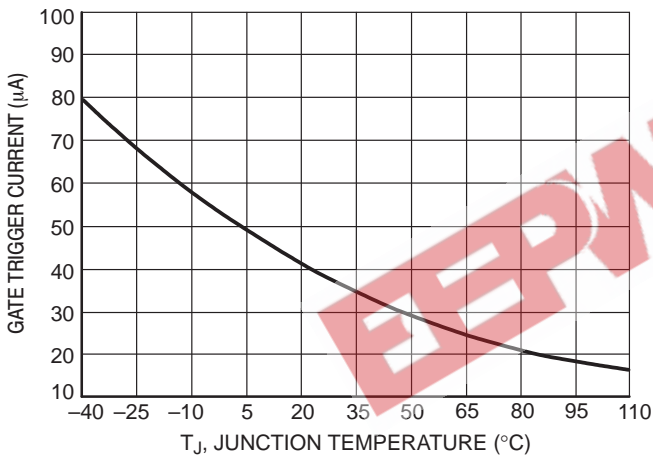
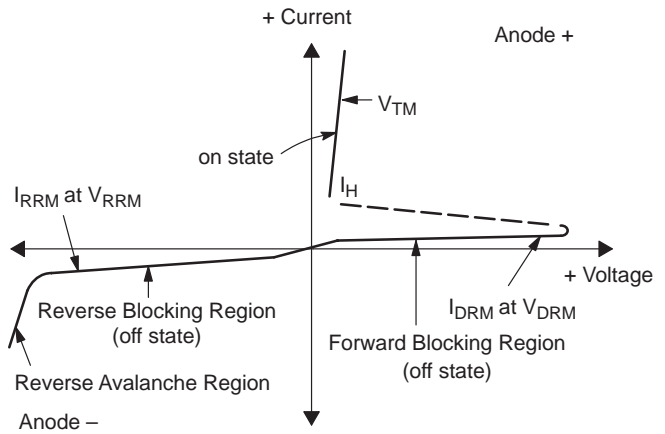


Figure 1. Typical Gate Trigger Current versus Junction Temperature

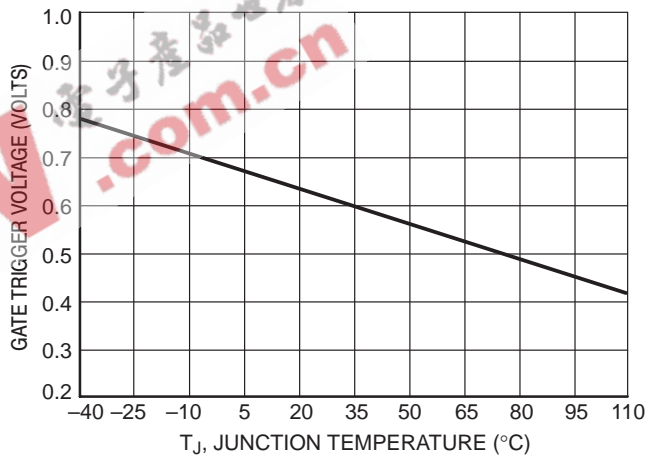


Figure 2. Typical Gate Trigger Voltage versus Junction Temperature

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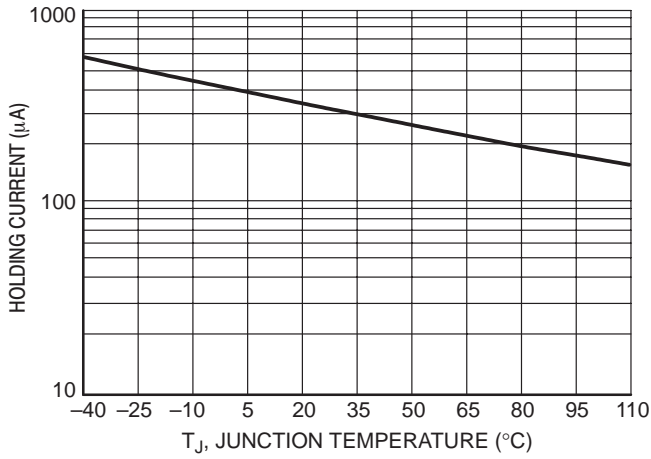


Figure 3. Typical Holding Current versus Junction Temperature

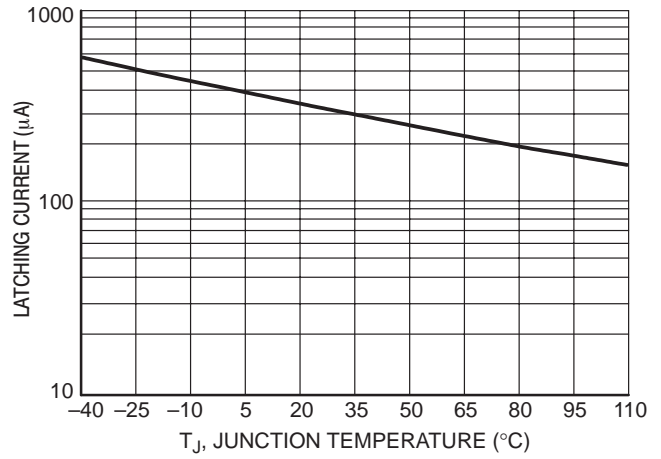


Figure 4. Typical Latching Current versus Junction Temperature

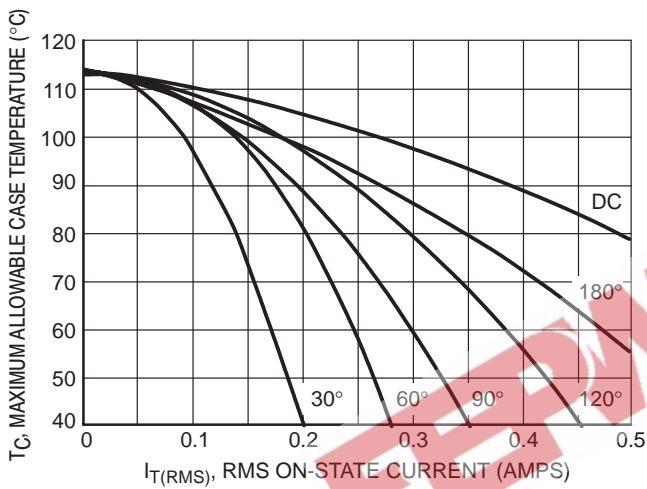


Figure 5. Typical RMS Current Derating

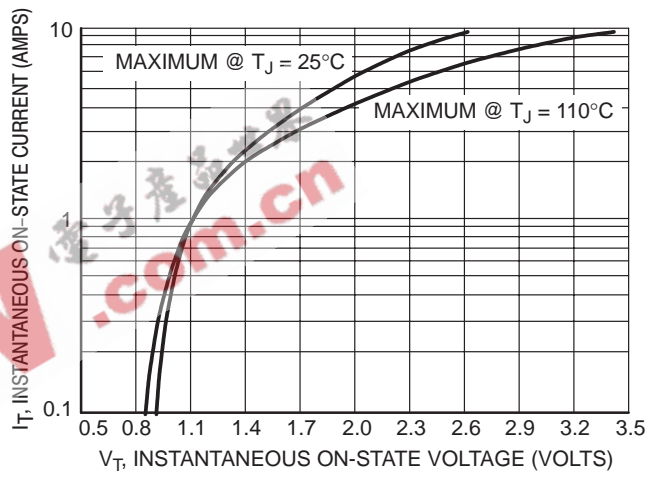


Figure 6. Typical On-State Characteristics