X4003/X4005

CPU Supervisor

FEATURES

- **Selectable watchdog timer**
  - **—Select 200ms, 600ms, 1.4s, off**
- **Low V_{CC} detection and reset assertion**
  - **—Five standard reset threshold voltages nominal 4.62V, 4.38V, 2.92V, 2.68V, 1.75V**
  - **—Adjust low V_{CC} reset threshold voltage using special programming sequence**
  - **—Reset signal valid to V_{CC} = 1V**
- **Low power CMOS**
  - **—12µA typical standby current, watchdog on**
  - **—800nA typical standby current watchdog off**
  - **—3mA active current**
- **400kHz I^2C interface**
- **1.8V to 5.5V power supply operation**
- **Available packages**
  - **—8-lead SOIC**
  - **—8-lead MSOP**

DESCRIPTION

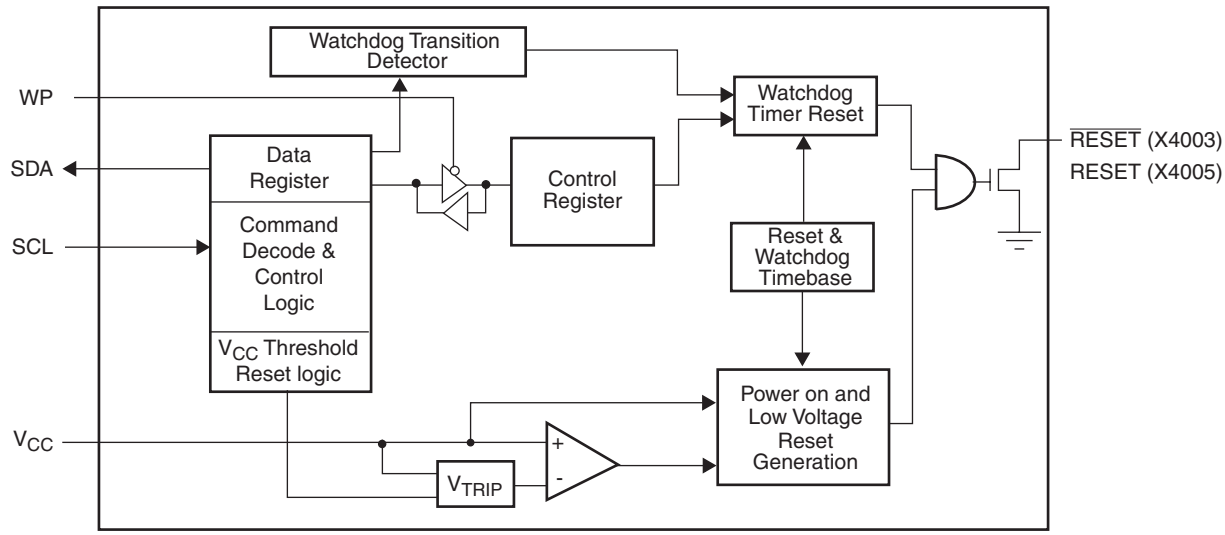
These devices combine three popular functions, Power-on Reset Control, Watchdog Timer, and Supply Voltage Supervision. This combination lowers system cost, reduces board space requirements, and increases reliability.

Applying power to the device activates the power on reset circuit which holds $\overline{\text{RESET}}$/RESET active for a period of time. This allows the power supply and oscillator to stabilize before the processor can execute code.

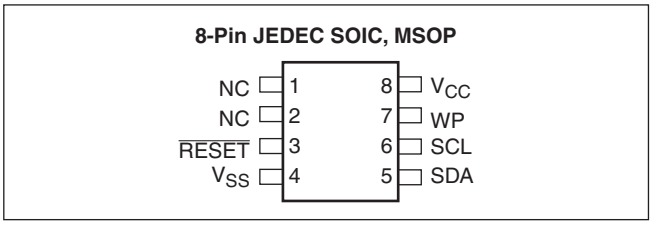
The Watchdog Timer provides an independent protection mechanism for microcontrollers. When the microcontroller fails to restart a timer within a selectable time out interval, the device activates the $\overline{\text{RESET}}$/RESET signal. The user selects the interval from three preset values. Once selected, the interval does not change, even after cycling the power.

The device's low V_{CC} detection circuitry protects the user's system from low voltage conditions, resetting the system when V_{CC} falls below the minimum V_{CC} trip point. $\overline{\text{RESET}}$/RESET is asserted until V_{CC} returns to proper operating level and stabilizes. Five industry standard V_{TRIP} thresholds are available; however, Xicor's unique circuits allow the threshold to be reprogrammed to meet custom requirements, or to fine-tune the threshold for applications requiring higher precision.

BLOCK DIAGRAM



PIN CONFIGURATION



PIN DESCRIPTION

Pin (SOIC/DIP)	Pin TSSOP	Pin (MSOP)	Name	Function
1	3		NC	No internal connections
2	4		NC	No internal connections
3	5	2	$\overline{\text{RESET}}$/ RESET	**Reset Output**. $\overline{\text{RESET}}$/RESET is an active LOW/HIGH, open drain output which goes active whenever V_{CC} falls below the minimum V_{CC} sense level. It will remain active until V_{CC} rises above the minimum V_{CC} sense level for 250ms. $\overline{\text{RESET}}$/ RESET goes active if the watchdog timer is enabled and SDA remains either HIGH or LOW longer than the selectable Watchdog time out period. A falling edge of SDA, while SCL also toggles from HIGH to LOW followed by a stop condition resets the watchdog timer. $\overline{\text{RESET}}$/RESET goes active on power up and remains active for 250ms after the power supply stabilizes.
4	6	3	V_{SS}	Ground
5	7	4	SDA	**Serial Data.** SDA is a bidirectional pin used to transfer data into and out of the device. It has an open drain output and may be wire ORed with other open drain or open collector outputs. This pin requires a pull up resistor and the input buffer is always active (not gated). **Watchdog Input.** A HIGH to LOW transition on the SDA while SCL also toggles from HIGH to LOW follow by a stop condition resets the watchdog timer. The absence of this procedure within the watchdog time out period results in $\overline{\text{RESET}}$/RESET going active.
6	8	5	SCL	**Serial Clock.** The serial clock controls the serial bus timing for data input and output.
7	1	6	WP	**Write Protect.** WP HIGH prevents changes to the watchdog timer setting.
8	2	1	V_{CC}	Supply voltage

PRINCIPLES OF OPERATION

Power On Reset

Application of power to the X4003/X4005 activates a power on reset circuit that pulls the $\overline{\text{RESET}}$/RESET pin active. This signal provides several benefits.

– It prevents the system microprocessor from starting to operate with insufficient voltage.

– It prevents the processor from operating prior to stabilization of the oscillator.

– It allows time for an FPGA to download its configuration prior to initialization of the circuit.

When V_{CC} exceeds the device V_{TRIP} threshold value for 200ms (nominal) the circuit releases $\overline{\text{RESET}}$/RESET, allowing the system to begin operation.

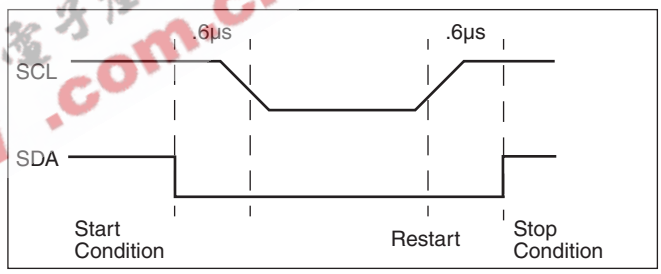
Low Voltage Monitoring

During operation, the X4003/X4005 monitors the V_{CC} level and asserts $\overline{\text{RESET}}$/RESET if supply voltage falls below a preset minimum V_{TRIP}. The $\overline{\text{RESET}}$/RESET signal prevents the microprocessor from operating in a power fail or brownout condition. The $\overline{\text{RESET}}$/RESET signal remains active until the voltage drops below 1V. It also remains active until V_{CC} returns and exceeds V_{TRIP} for 200ms.

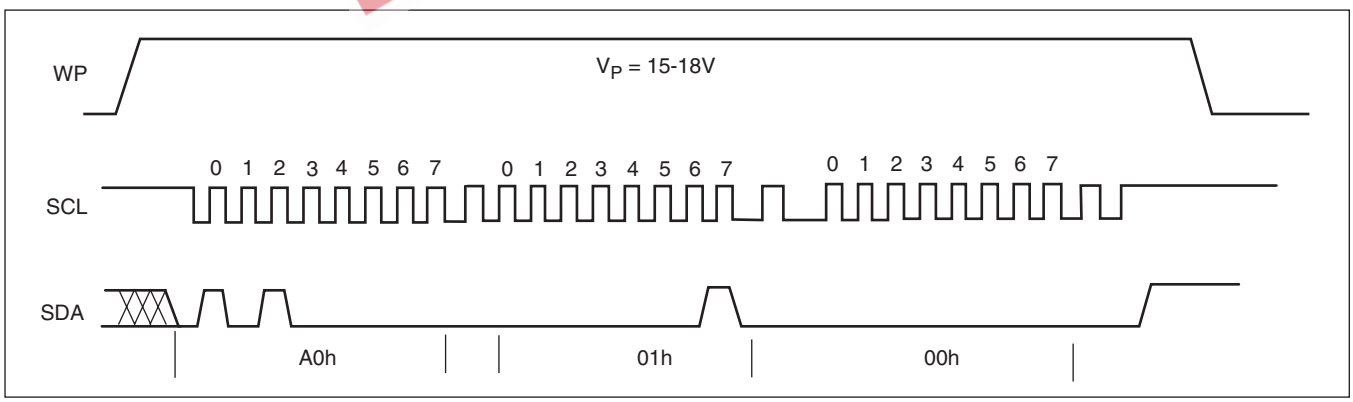
Watchdog Timer

The watchdog timer circuit monitors the microprocessor activity by monitoring the SDA and SCL pins. The microprocessor must toggle the SDA pin HIGH to LOW periodically, while SCL also toggles from HIGH to LOW (this is a start bit) followed by a stop condition prior to the expiration of the watchdog time out period to prevent a $\overline{\text{RESET}}$/RESET signal. The state of two nonvolatile control bits in the control register determine the watchdog timer period. The microprocessor can change these watchdog bits, or they may be "locked" by tying the WP pin HIGH.

Figure 1. Watchdog Restart



Set V_{TRIP} Level Sequence (V_{CC} = desired V_{TRIP} value)



V_{CC} THRESHOLD RESET PROCEDURE

The X4003/X4005 is shipped with a standard V_{CC} threshold (V_{TRIP}) voltage. This value will not change over normal operating and storage conditions. However, in applications where the standard V_{TRIP} is not exactly right, or if higher precision is needed in the V_{TRIP} value, the X4003/X4005 threshold may be adjusted. The procedure is described below, and uses the application of a nonvolatile control signal.

Setting the V_{TRIP} Voltage

This procedure is used to set the V_{TRIP} to a higher voltage value. For example, if the current V_{TRIP} is 4.4V and the new V_{TRIP} is 4.6V, this procedure will directly make the change. If the new setting is to be lower than the current setting, then it is necessary to reset the trip point before setting the new value.

To set the new V_{TRIP} voltage, apply the desired V_{TRIP} threshold voltage to the V_{CC} pin and tie the WP pin to the programming voltage V_P. Then write data 00hto address 01h. The stop bit following a valid write operation initiates the V_{TRIP} programing sequence. Bring WP LOW to complete the operation.

Resetting the V_{TRIP} Voltage

This procedure is used to set the V_{TRIP} to a "native" voltage level. For example, if the current V_{TRIP} is 4.4V and the new V_{TRIP} must be 4.0V, then the V_{TRIP} must be reset. When V_{TRIP} is reset, the new V_{TRIP} is something less than 1.7V. This procedure must be used to set the voltage to a lower value.

To reset the new V_{TRIP} voltage, apply the desired V_{TRIP} threshold voltage to the V_{CC} pin and tie the WP pin to the programming voltage V_P. Then write 00h to address 03h. The stop bit of a valid write operation initiates the V_{TRIP} programming sequence. Bring WP LOW to complete the operation.

Figure 2. Reset V_{TRIP} Level Sequence (V_{CC} > 3V. $\overline{WP}$ = 15-18V)

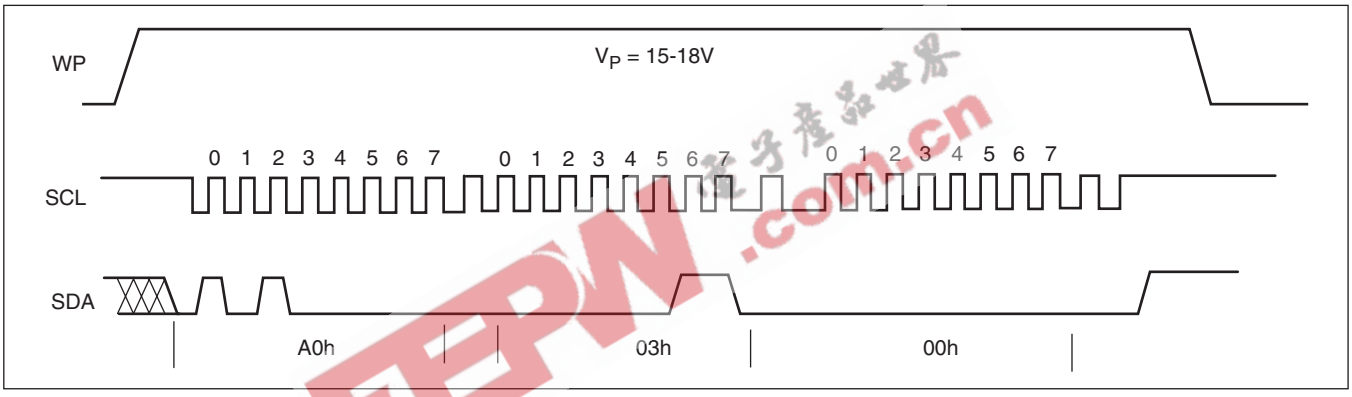


Figure 3. Sample V_{TRIP} Reset Circuit

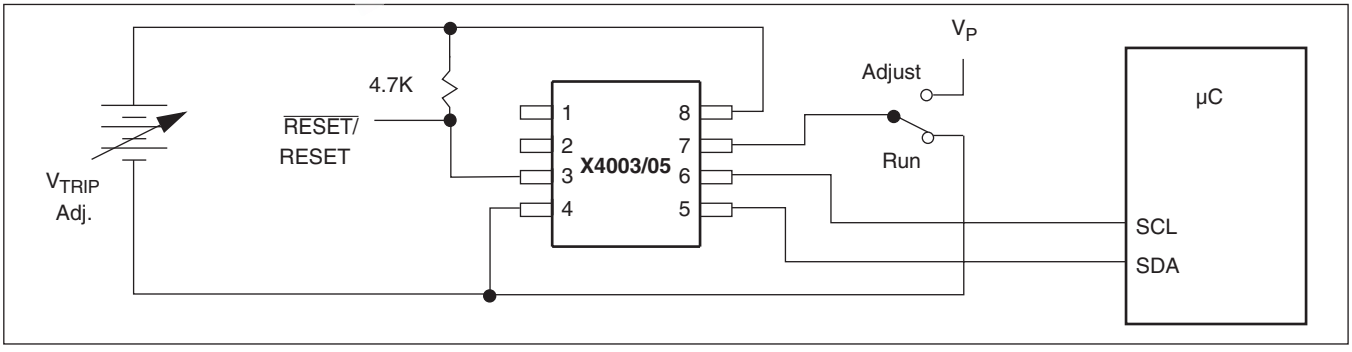
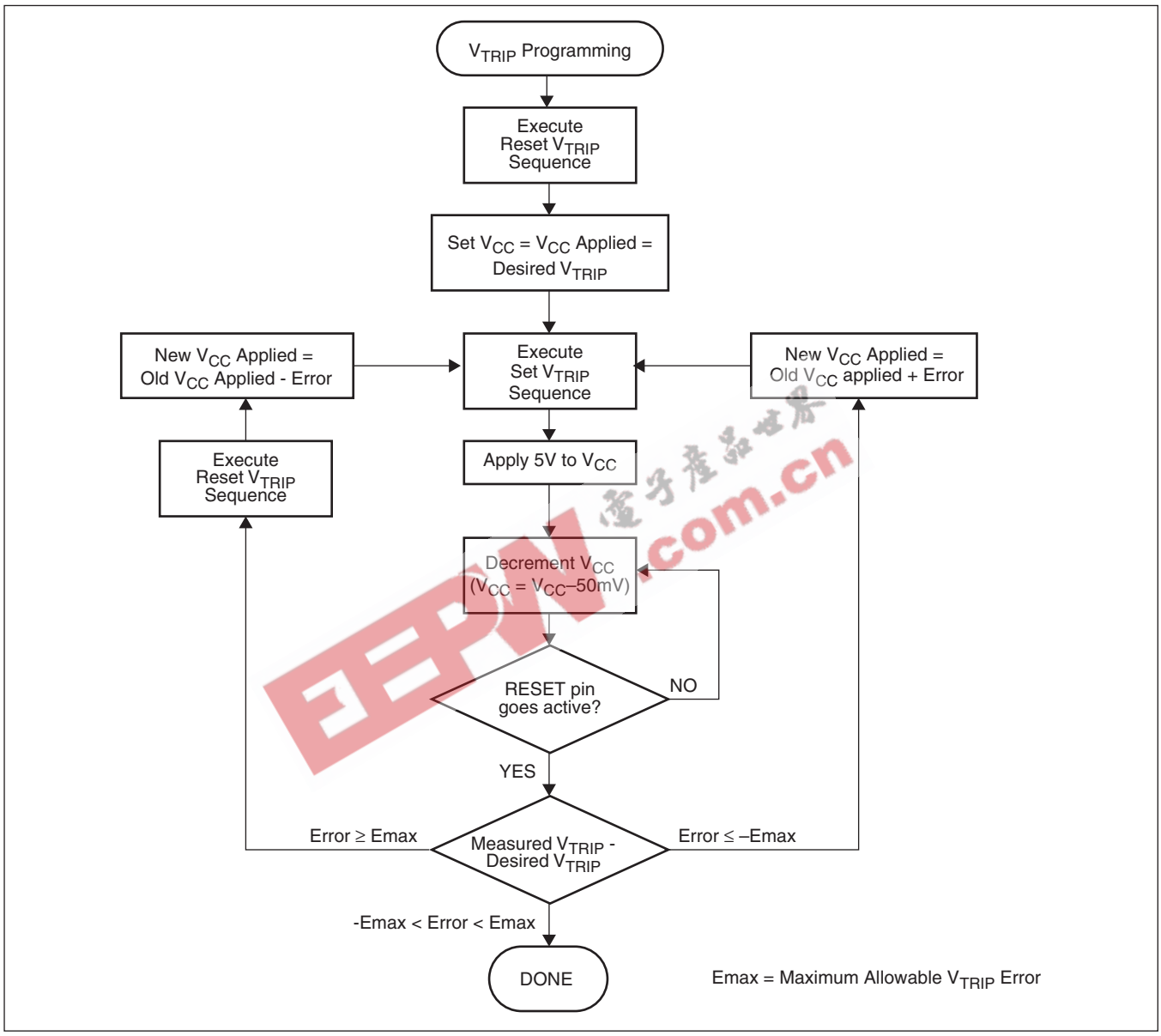


Figure 4. V_{TRIP} Programming Sequence



Control Register

The control register provides the user a mechanism for changing the watchdog timer settings. watchdog timer bits are nonvolatile and do not change when power is removed.

The control register is accessed with a special preamble in the slave byte (1011) and is located at address 1FFh. It can only be modified by performing a control register write operation. Only one data byte is allowed for each register write operation. Prior to writing to the control register, the WEL and RWEL bits must be set using a two step process, with the whole sequence requiring 3 steps. See "Writing to the Control Register" below.

The user must issue a stop after sending the control byte to the register to initiate the nonvolatile cycle that stores WD1 and WD0. The X4003/X4005 will not acknowledge any data bytes written after the first byte is entered.

The state of the control register can be read at any time by performing a serial read operation. Only one byte is read by each register read operation. The X4003/X4005 resets itself after the first byte is read. The master should supply a stop condition to be consistent with the bus protocol, but a stop is not required to end this operation.

7	6	5	4	3	2	1	0
0	WD1	WD0	0	0	RWEL	WEL	0

RWEL: Register Write Enable Latch (Volatile)

The RWEL bit must be set to "1" prior to a write to the control register.

WEL: Write Enable Latch (Volatile)

The WEL bit controls the access to the control register during a write operation. This bit is a volatile latch that powers up in the LOW (disabled) state. While the WEL bit is LOW, writes the control register will be ignored (no acknowledge will be issued after the data byte). The WEL bit is set by writing a "1" to the WEL bit and zeroes to the other bits of the control register. Once set, WEL remains set until either it is reset to 0 (by writing a "0" to the WEL bit and zeroes to the other bits of the control register) or until the part powers up again. Writes to the WEL bit do not cause a nonvolatile write cycle, so the device is ready for the next operation immediately after the stop condition.

WD1, WD0: Watchdog Timer Bits

The bits WD1 and WD0 control the period of the watchdog timer. The options are shown below.

WD1	WD0	Watchdog Time Out Period
0	0	1.4 seconds
0	1	600 milliseconds
1	0	200 milliseconds
1	1	Disabled (factory setting)

Writing to the Control Register

Changing any of the nonvolatile bits of the control register requires the following steps:

– Write a 02H to the control register to set the write enable latch (WEL). This is a volatile operation, so there is no delay after the write. (Operation preceeded by a start and ended with a stop.)

– Write a 06H to the control register to set both the register write enable latch (RWEL) and the WEL bit. This is also a volatile cycle. The zeros in the data byte are required. (Operation preceeded by a start and ended with a stop.)

– Write a value to the control register that has all the control bits set to the desired state. This can be represented as 0*xy*0 0010 in binary, where *xy* are the WD bits. (Operation preceeded by a start and ended with a stop.) Since this is a nonvolatile write cycle it will take up to 10ms to complete. The RWEL bit is reset by this cycle and the sequence must be repeated to change the nonvolatile bits again. If bit 2 is set to '1' in this third step (0*xy*0 0110) then the RWEL bit is set, but the WD1 and WD0 bits remain unchanged. Writing a second byte to the control register is not allowed. Doing so aborts the write operation and returns a NACK.

– A read operation occurring between any of the previous operations will not interrupt the register write operation.

– The RWEL bit cannot be reset without writing to the nonvolatile control bits in the control register, power cycling the device or attempting a write to a write protected block.

To illustrate, a sequence of writes to the device consisting of [02H, 06H, 02H] will reset all of the nonvolatile bits in the control register to 0. A sequence of [02H, 06H, 06H] will leave the nonvolatile bits unchanged and the RWEL bit remains set.

SERIAL INTERFACE

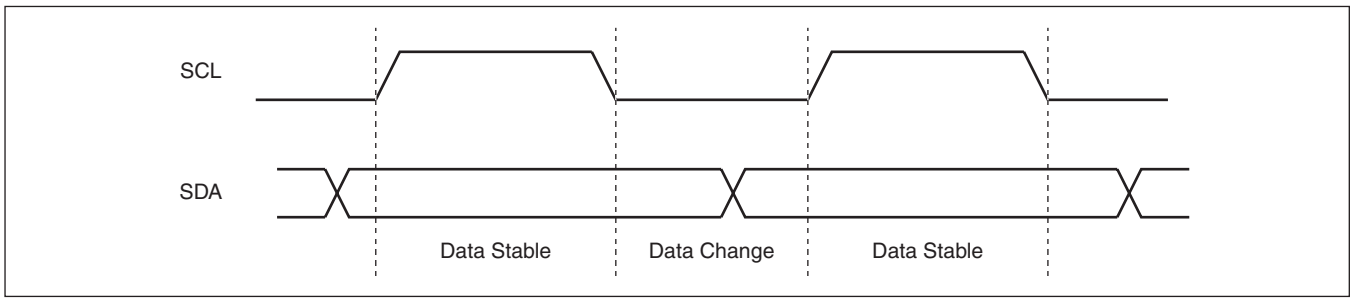
Serial Interface Conventions

The device supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter, and the receiving device as the receiver. The device controlling the transfer is called the master and the device being controlled is called the slave. The master always initiates data transfers, and provides the clock for both transmit and receive operations. Therefore, the devices in this family operate as slaves in all applications.

Serial Clock and Data

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions. See Figure 5.

Figure 5. Valid Data Changes on the SDA Bus



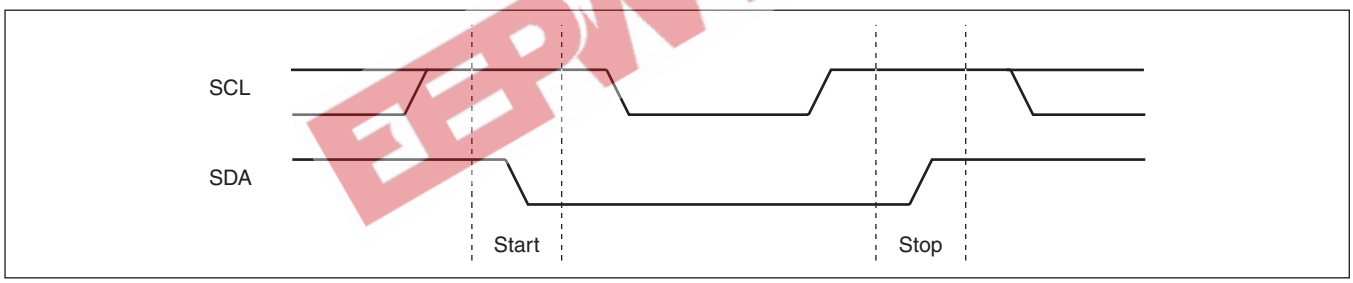
Serial Start Condition

All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The device continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met. See Figure 6.

Serial Stop Condition

All communications must be terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used to place the device into the Standby power mode after a read sequence. A stop condition can only be issued after the transmitting device has released the bus. See Figure 6.

Figure 6. Valid Start and Stop Conditions

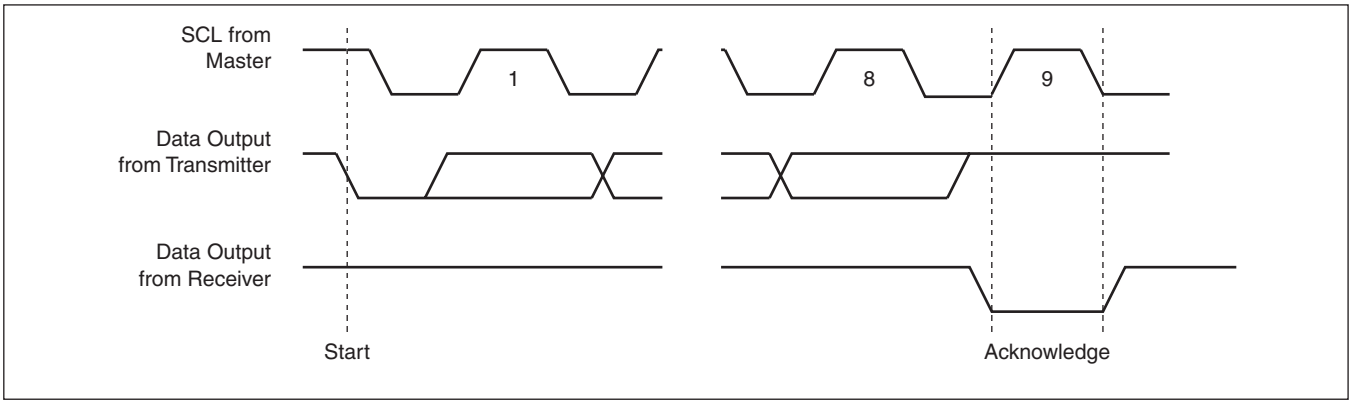


Serial Acknowledge

Acknowledge is a software convention used to indicate successful data transfer. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle, the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data. Refer to Figure 7.

The device will respond with an acknowledge after recognition of a start condition and the correct contents of the slave address byte. Acknowledge bits are also provided by the X4003/4005 after correct reception of the control register address byte, after receiving the byte written to the control register and after the second slave address in a read question (See Figure 8 and See Figure 9.)

Figure 7. Acknowledge Response From Receiver



SERIAL WRITE OPERATIONS

Slave Address Byte

Following a start condition, the master must output a slave address byte. This byte consists of several parts:

– a device type identifier that is always '1011'.

– two bits of '0'.

– one bit of the slave command byte is a R/$\overline{W}$ bit. The R/$\overline{W}$ bit of the slave address byte defines the operation to be performed. When the R/$\overline{W}$ bit is a one, then a read operation is selected. A zero selects a write operation. Refer to Figure 8.

– After loading the entire slave address byte from the SDA bus, the device compares the input slave byte data to the proper slave byte. Upon a correct compare, the device outputs an acknowledge on the SDA line.

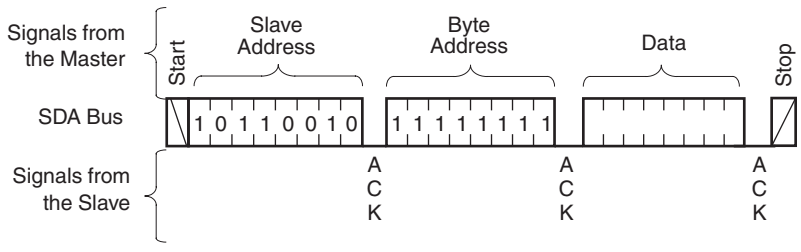
Write Control Register

To write to the control register, the device requires the slave address byte and a byte address. This gives the master access to register. After receipt of the address byte, the device responds with an acknowledge, and awaits the data. After receiving the 8 bits of the data byte, the device again responds with an acknowledge. The master then terminates the transfer by generating a stop condition, at which time the device begins the internal write cycle to the nonvolatile memory. During this internal write cycle, the device inputs are disabled, so the device will not respond to any requests from the master. If WP is HIGH, the control register cannot be changed. A write to the control register will suppress the acknowledge bit and no data in the control register will change. With WP low, a second byte written to the control register terminates the operation and no write occurs.

Stops and Write Modes

Stop conditions that terminate write operations must be sent by the master after sending 1 full data byte plus the subsequent ACK signal. If a stop is issued in the middle of a data byte, or before 1 full data byte plus its associated ACK is sent, then the device will reset itself without performing the write.

Figure 8. Write Control Register Sequence



Serial Read Operations

The read operation allows the master to access the control register. To conform to the I^2C standard, prior to issuing the slave address byte with the R/$\overline{W}$ bit set to one, the master must first perform a "dummy" write operation. The master issues the start condition and the slave address byte, receives an acknowledge, then issues the byte address. After acknowledging receipt of the byte address, the master immediately issues another start condition and the slave address byte with the R/$\overline{W}$ bit set to one. This is followed by an acknowledge from the device and then by the eight bit control register. The master terminates the read operation by not responding with an acknowledge and then issuing a stop condition. Refer to Figure 9 for the address, acknowledge, and data transfer sequences.

Operational Notes

The device powers-up in the following state:

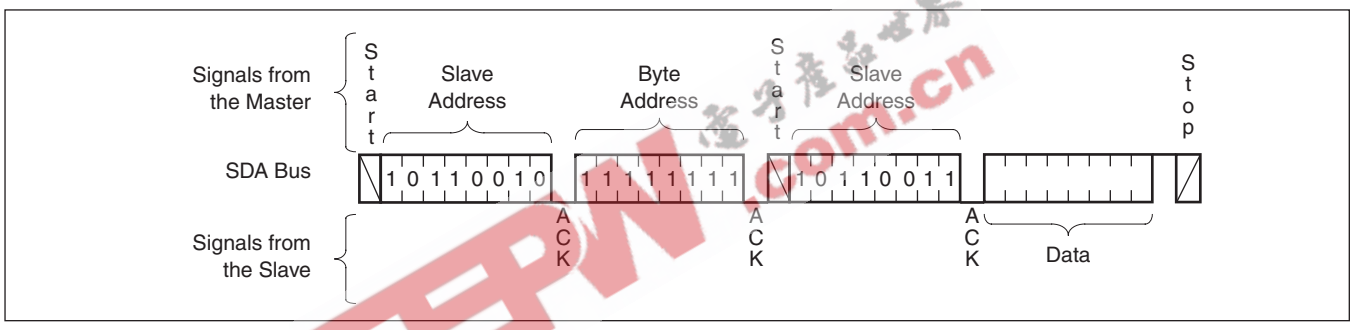
– The device is in the low power standby state.

– The WEL bit is set to '0'. In this state it is not possible to write to the device.

– SDA pin is the input mode.

$\overline{RESET}$/RESET signal is active for t_{PURST}.

Figure 9. Control Register Read Sequence



Data Protection

The following circuitry has been included to prevent inadvertent writes:

– The WEL bit must be set to allow a write operation.

– The proper clock count and bit sequence is required prior to the stop bit in order to start a nonvolatile write cycle.

– A three step sequence is required before writing into the control register to change watchdog timer or block lock settings.

– The WP pin, when held HIGH, prevents all writes to the control register.

– Communication to the device is inhibited below the V_{TRIP} voltage.

– Command to change the control register are terminated if in-progress when $\overline{RESET}$/RESET go active.

Symbol Table

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

ABSOLUTE MAXIMUM RATINGS

Temperature under bias ..... -65°C to +135°C
Storage temperature ..... -65°C to +150°C
Voltage on any pin with
respect to V_{SS} .....-1.0V to +7V
D.C. output current 5mA
Lead temperature (soldering, 10 seconds).....300°C

COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; the functional operation of the device (at these or any other conditions above those listed in the operational sections of this specification) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	70°C
Industrial	-40°C	+85°C

Option	Supply Voltage Limits
–1.8	1.8V to 3.6V
–2.7 and –2.7A	2.7V to 5.5V
Blank and –4.5A	4.5V to 5.5V

D.C. OPERATING CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified.)

Symbol	Parameter	V_{CC} = 1.8 to 3.6V		V_{CC} = 2.7 to 5.5V		Unit	Test Conditions
		Min	Max	Min	Max		
I_{CC}[1]	Active supply current read control register		0.5		1.0	mA	f_{SCL} = 400kHznonvolatile, SDA = Open
I_{CC2}[1]	Active supply current write control register		1.5		3.0	mA	
I_{CC3}[2]	Operating current AC (WDT off)		1		1	µA	
I_{CC4}[2]	Operating current DC (WDT off)		1		1	µA	$V_{SDA} = V_{SCL} = V_{CC}$ Others = GND or V_{SB}
I_{CC5}[2]	Operating current DC (WDT on)		10		20	µA	
I_{LI}	Input leakage current		10		10	µA	V_{IN} = GND to V_{CC}
I_{LO}	Output leakage current		10		10	µA	V_{SDA} = GND to V_{CC} Device is in Standby[2]
V_{IL}[3]	Input LOW voltage	-0.5	V_{CC} x 0.3	-0.5	V_{CC} x 0.3	V	
V_{IH}[3]	Input HIGH voltage	V_{CC} x 0.7	V_{CC} + 0.5	V_{CC} x 0.7	V_{CC} + 0.5	V	
V_{HYS}	Schmitt trigger input hysteresis fixed input level V_{CC} related level	0.2 .05 x V_{CC}		0.2 .05 x V_{CC}		V	
V_{OL}	Output LOW voltage		0.4		0.4	V	I_{OL} = 3.0mA (2.7–5.5V) I_{OL} = 1.8mA (1.8–3.6V)

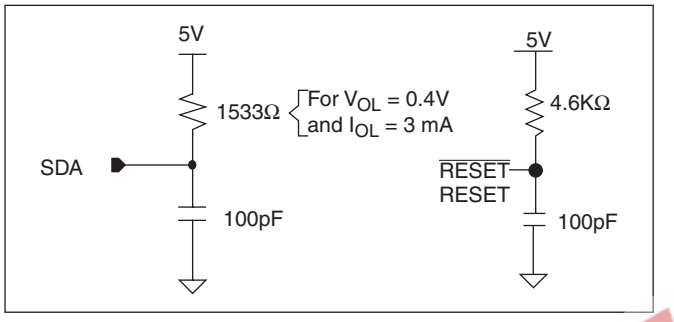
Notes: (1) The device enters the active state after any start, and remains active until: 9 clock cycles later if the device select bits in the slave address byte are incorrect; 200ns after a stop ending a read operation; or t_{WC} after a stop ending a write operation.
(2) The device goes into standby: 200ns after any stop, except those that initiate a nonvolatile write cycle; t_{WC} after a stop that initiates a nonvolatile cycle; or 9 clock cycles after any start that is not followed by the correct device select bits in the slave address byte.
(3) V_{IL} min. and V_{IH} max. are for reference only and are not tested.

CAPACITANCE (T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V)

Symbol	Parameter	Max.	Unit	Test Conditions
C_{OUT}(4)	Output capacitance (SDA, $\overline{RESET}$/RESET)	8	pF	V_{OUT} = 0V
C_{IN}(4)	Input capacitance (SCL, WP)	6	pF	V_{IN} = 0V

Note: (4) This parameter is periodically sampled and not 100% tested.

EQUIVALENT A.C. LOAD CIRCUIT



A.C. TEST CONDITIONS

Input pulse levels	0.1V_{CC} to 0.9V_{CC}
Input rise and fall times	10ns
Input and output timing levels	0.5V_{CC}
Output load	Standard output load

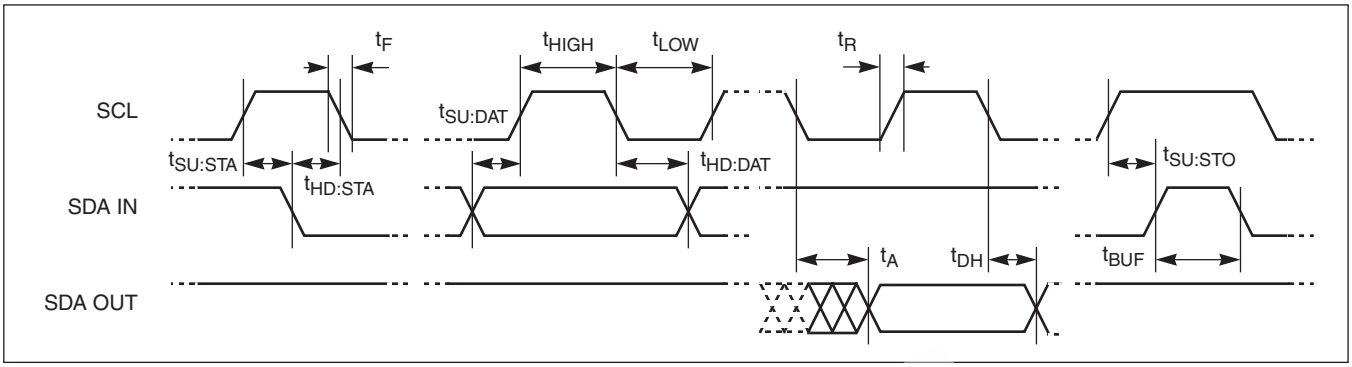
A.C. CHARACTERISTICS (Continued)(Over recommended operating conditions, unless otherwise specified)

Symbol	Parameter	100kHz		400kHz		Unit
		Min.	Max.	Min.	Max.	
f_{SCL}	SCL clock frequency	0	100	0	400	kHz
t_{IN}	Pulse width suppression time at inputs	n/a	n/a	50		ns
t_{AA}	SCL LOW to SDA data out valid	0.1	0.9	0.1	0.9	µs
t_{BUF}	Time the bus free before start of new transmission	4.7		1.3		µs
t_{LOW}	Clock LOW time	4.7		1.3		µs
t_{HIGH}	Clock HIGH time	4.0		0.6		µs
$t_{SU:STA}$	Start condition setup time	4.7		0.6		µs
$t_{HD:STA}$	Start condition hold time	4.0		0.6		µs
$t_{SU:DAT}$	Data in setup time	250		100		ns
$t_{HD:DAT}$	Data in hold time	5.0		0		µs
$t_{SU:STO}$	Stop condition setup time	0.6		0.6		µs
t_{DH}	Data output hold time	50		50		ns
t_R	SDA and SCL rise time		1000	20 +.1Cb(6)	300	ns
t_F	SDA and SCL fall time		300	20 +.1Cb(6)	300	ns
$t_{SU:WP}$	$\overline{WP}$ setup time	0.4		0.6		µs
$t_{HD:WP}$	$\overline{WP}$ hold time	0		0		µs
Cb	Capacitive load for each bus line		400		400	pF

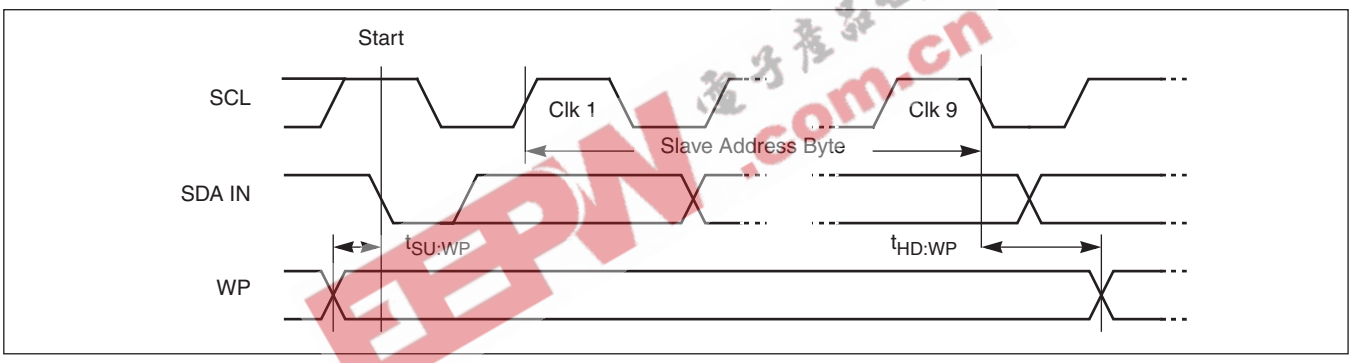
Notes: (5) Typical values are for T_A = 25°C and V_{CC} = 5.0V
(6) Cb = total capacitance of one bus line in pF.

TIMING DIAGRAMS

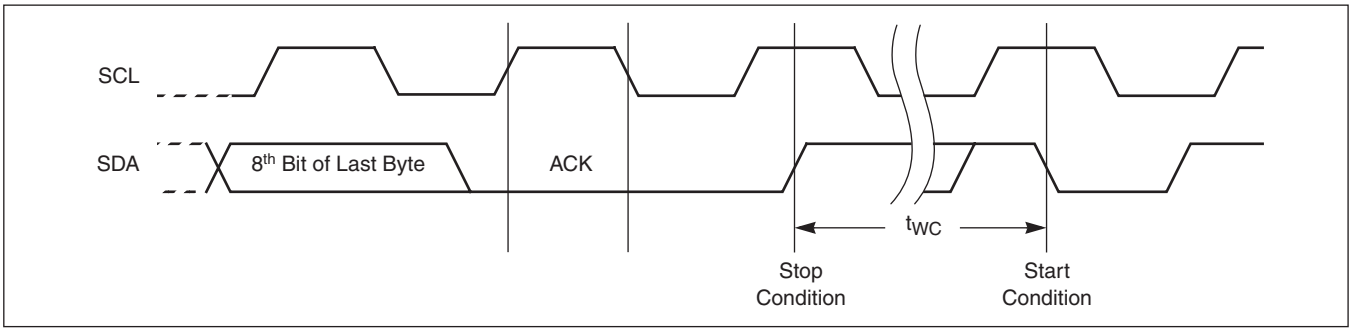
Bus Timing



WP Pin Timing



Write Cycle Timing

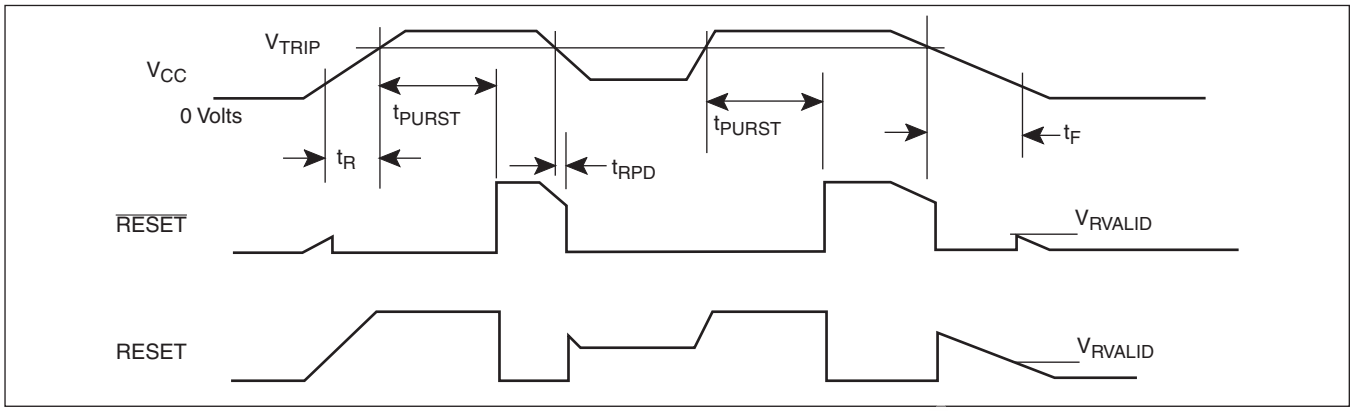


Nonvolatile Write Cycle Timing

Symbol	Parameter	Min.	Typ.(1)	Max.	Unit
t_{WC}(7)	Write cycle time		5	10	ms

Note: (7) t_{WC} is the time from a valid stop condition at the end of a write sequence to the end of the self-timed internal nonvolatile write cycle. It is the minimum cycle time to be allowed for any nonvolatile write by the user, unless Acknowledge Polling is used.

Power-Up and Power-Down Timing

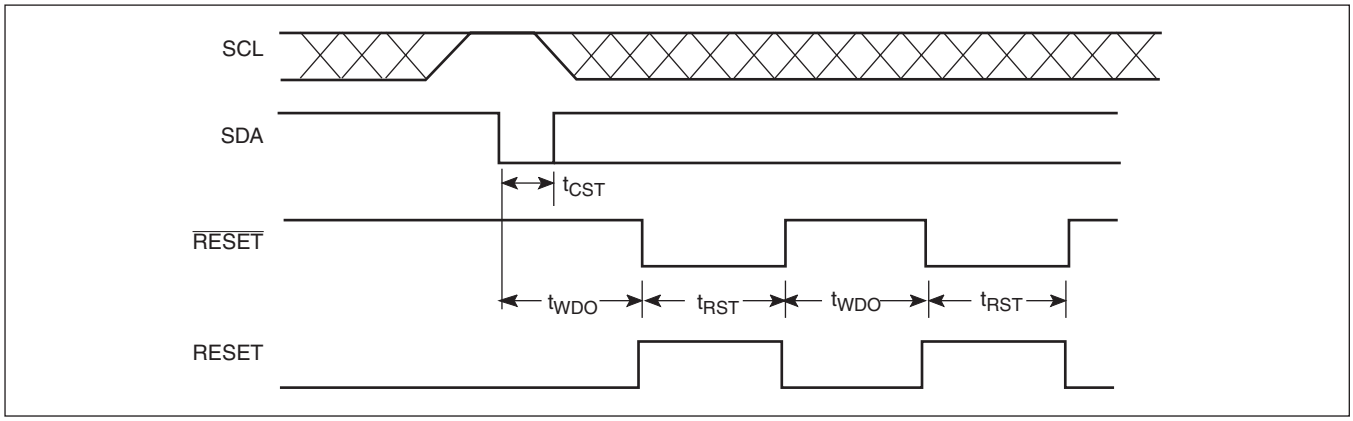


RESET/RESET Output Timing

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{TRIP}	Reset trip point voltage, X4003–4.5A, X4005–4.5A	4.5	4.62	4.75	V
	Reset trip point voltage, X4003, X4005	4.25	4.38	4.5	V
	Reset trip point voltage, X4003–2.7A, X4005–2.7A	2.85	2.92	3.0	V
	Reset trip point voltage, X4003–2.7, X4005–2.7	2.55	2.62	2.7	
	Reset trip point voltage, X4003–1.8, X4005–1.8	1.7	1.75	1.8	
t_{PURST}	Power-up reset time out	100	200	400	ms
t_{RPD}[8]	V_{CC} detect to reset/output			500	ns
t_F[8]	V_{CC} fall time	10			ms
t_R[8]	V_{CC} rise time	0.1			ns
V_{RVALID}	Reset valid V_{CC}	1			V

Note: (8) This parameter is periodically sampled and not 100% tested.

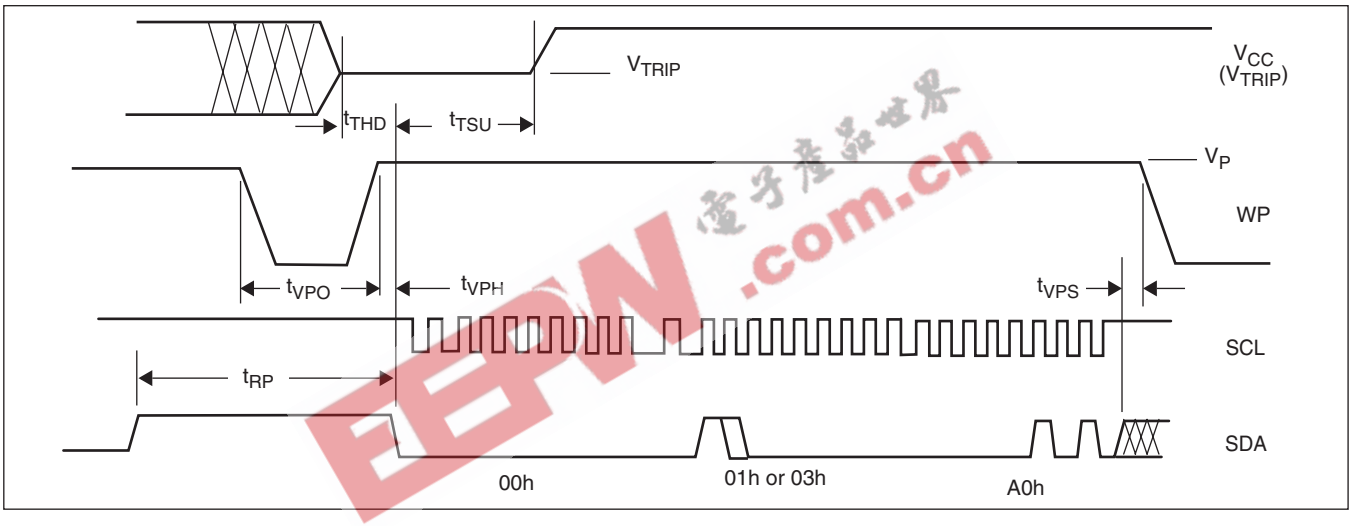
SDA vs. RESET/RESET Timing



RESET/RESET Output Timing

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{WDO}	Watchdog time out period, WD1 = 1, WD0 = 1 (factory setting) WD1 = 1, WD0 = 0 WD1 = 0, WD0 = 1 WD1 = 0, WD0 = 0	 100 450 1	 OFF 200 600 1.4	 300 800 2	 ms ms sec
t_{CST}	$\overline{CS}$ pulse width to reset the watchdog	400			ns
t_{RST}	Reset time out	100	200	400	ms

V_{TRIP} Programming Timing Diagram



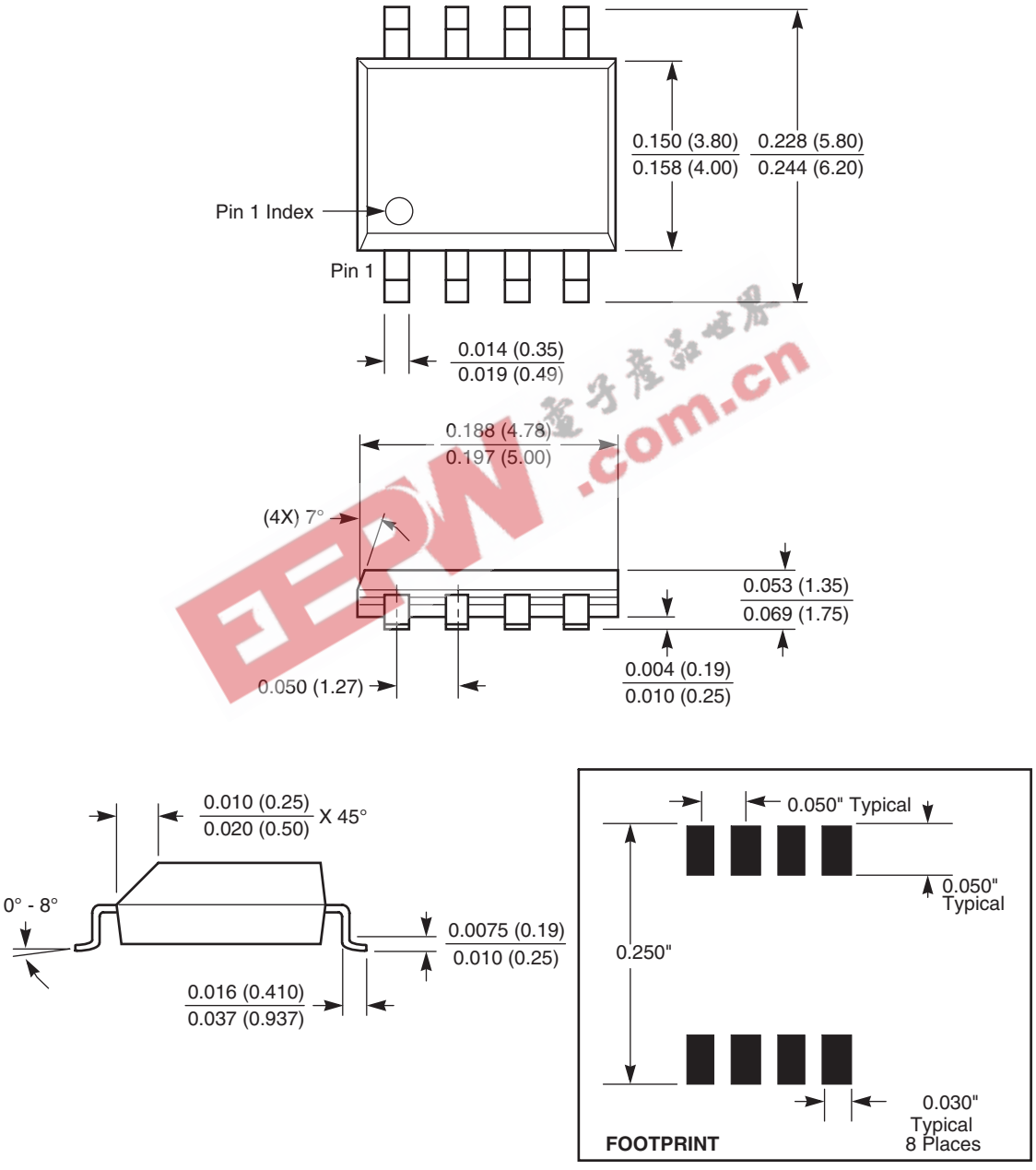
V_{TRIP} Programming Parameters

Parameter	Description	Min.	Max.	Unit
t_{VPS}	V_{TRIP} program enable voltage setup time	1		µs
t_{VPH}	V_{TRIP} program enable voltage hold time	1		µs
t_{TSU}	V_{TRIP} setup time	1		µs
t_{THD}	V_{TRIP} hold (stable) time	10		ms
t_{WC}	V_{TRIP} write cycle time		10	ms
t_{VPO}	V_{TRIP} program enable voltage off time (between successive adjustments)	0		µs
t_{RP}	V_{TRIP} program recovery period (between successive adjustments)	10		ms
V_P	Programming voltage	15	18	V
V_{TRAN}	V_{TRIP} programmed voltage range	1.7	5.0	V
V_{ta1}	Initial V_{TRIP} program voltage accuracy (V_{CC} applied–V_{TRIP}) (Programmed at 25°C.)	-0.1	+0.4	V
V_{ta2}	Subsequent V_{TRIP} program voltage accuracy [(V_{CC} applied–V_{ta1})–V_{TRIP}. Programmed at 25°C.)	-25	+25	mV
V_{tr}	V_{TRIP} program voltage repeatability (Successive program operations. Programmed at 25°C.)	-25	+25	mV
V_{tv}	V_{TRIP} program variation after programming (0-75°C). (programmed at 25°C)	-25	+25	mV

V_{TRIP} programming parameters are periodically sampled and are not 100% tested.

PACKAGING INFORMATION

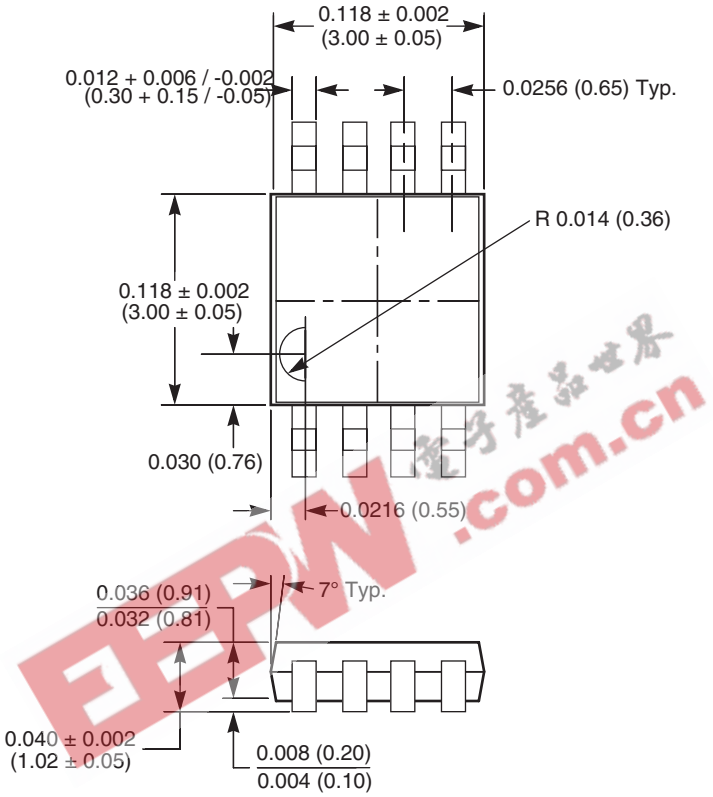
8-Lead Plastic Small Outline Gull Wing Package Type S

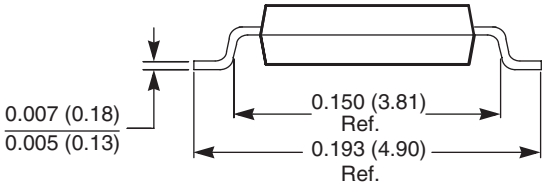


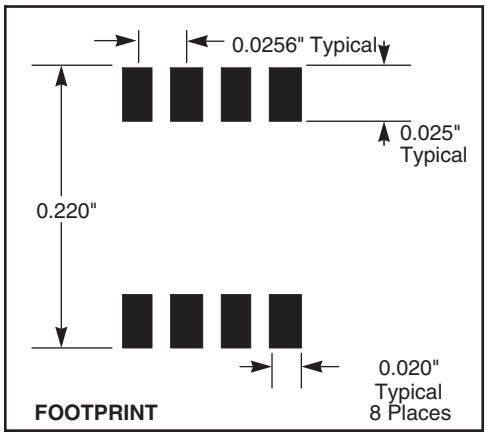
NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

PACKAGING INFORMATION

8-Lead Miniature Small Outline Gull Wing Package Type M







NOTE:
1. ALL DIMENSIONS IN INCHES AND (MILLIMETERS)

Ordering Information

V_{CC} Range	V_{TRIP} Range	Package	Operating Temperature Range	Part Number $\overline{\text{RESET}}$ (Active LOW)	Part Number RESET (Active HIGH)
4.5–5.5V	4.5–4.75	8L SOIC	0–70°C	X4003S8–4.5A	X4005S8–4.5A
			-40–85°C	X4003S8I–4.5A	X4005S8I–4.5A
		8L MSOP	-40–85°C	X4003M8I–4.5A	X4005M8I–4.5A
4.5–5.5V	4.25–4.5	8L SOIC	0–70°C	X4003S8	X4005S8
			-40–85°C	X4003S8I	X4005S8I
		8L MSOP	-40–85°C	X4003M8I	X4005M8I
2.7–5.5V	2.85–3.0	8L SOIC	0–70°C	X4003S8–2.7A	X4005S8–2.7A
			-40–85°C	X4003S8I–2.7A	X4005S8I–2.7A
		8L MSOP	-40–85°C	X4003M8I–2.7A	X4005M8I–2.7A
2.7–5.5V	2.55–2.7	8L SOIC	0–70°C	X4003S8–2.7	X4005S8–2.7
			-40–85°C	X4003S8I–2.7	X4005S8I–2.7
		8L MSOP	-40–85°C	X4003M8I–2.7	X4005M8I–2.7
1.8–3.6V	1.7–1.8	8L SOIC	0–70°C	X4003S8–1.8	X4005S8–1.8
		8L MSOP	0–70°C	X4003M8–1.8	X4005M8–1.8

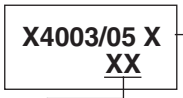
Part Mark Information

8-Lead TSSOP

ACI/ACR = –4.5A (0 to70°C)
ACK/ACT = No Suffix (0 to 70°C)
ACM/ACV = –2.7A (0 to 70°C)
ACO/ACX = –2.7 (0 to 70°C)
ACP/ACY = –1.8 (0 to 70°C)

4003/4005

8-Lead SOIC



AL = –4.5A (0 to +70°C)
AM = –4.5A (-171740 to +85°C)
Blank = No Suffix (0 to +70°C)
I = No Suffix (-40 to +85°C)
AN = –2.7A (0 to +70°C)
AP = –2.7A (-40 to +85°C)
F = –2.7 (0 to +70°C)
G = –2.7 (-40 to +85°C)
AG = –1.8 (0 to +70°C)

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.