

This X25330 device has been acquired by  
IC MICROSYSTEMS from Xicor, Inc.



32K

X25330

4K x 8 Bit

5MHz SPI Serial E<sup>2</sup>PROM with Block Lock™ Protection

FEATURES

- 5MHz Clock Rate
- Low Power CMOS
  - <1µA Standby Current
  - <5mA Active Current
- 2.5V To 5.5V Power Supply
- SPI Modes (0,0 & 1,1)
- 4K X 8 Bits
  - 32 Byte Page Mode
- Block Lock™ Protection
  - Protect 1/4, 1/2 or all of E<sup>2</sup>PROM Array
- Programmable Hardware Write Protection
  - In-Circuit Programmable ROM Mode
- Built-in Inadvertent Write Protection
  - Power-Up/Down protection circuitry
  - Write Enable Latch
  - Write Protect Pin
- Self-Timed Write Cycle
  - 5ms Write Cycle Time (Typical)
- High Reliability
  - Endurance: 100,000 cycles
  - Data Retention: 100 Years
  - ESD protection: 2000V on all pins
- Packages
  - 8-Lead SOIC
  - 14-Lead TSSOP

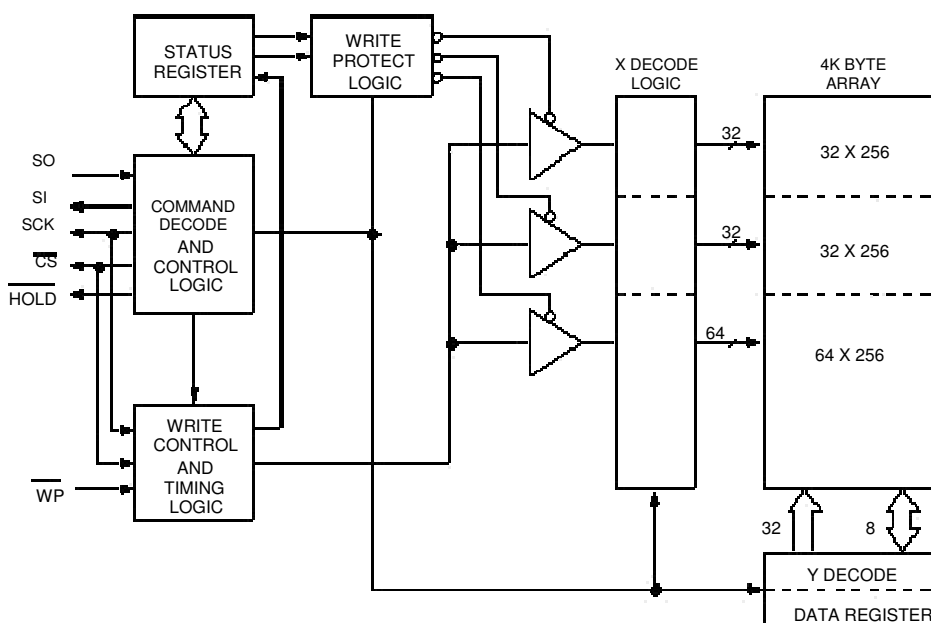
DESCRIPTION

The X25330 is a CMOS 32K-bit serial E<sup>2</sup>PROM, internally organized as 4K x 8. The X25330 features a Serial Peripheral Interface (SPI) and software protocol allowing operation on a simple three-wire bus. The bus signals are a clock input (SCK) plus separate data in (SI) and data out (SO) lines. Access to the device is controlled through a chip select ( $\overline{CS}$ ) input, allowing any number of devices to share the same bus.

The X25330 also features two additional inputs that provide the end user with added flexibility. By asserting the HOLD input, the X25330 will ignore transitions on its inputs, thus allowing the host to service higher priority interrupts. The WP input can be used as a hardware input to the X25330 disabling all write attempts to the status register, thus providing a mechanism for limiting end user capability of altering 0, 1/4, 1/2 or all of the memory.

The X25330 utilizes Xicor's proprietary Direct Write™ cell, providing a minimum endurance of 100,000 cycles and a minimum data retention of 100 years.

FUNCTIONAL DIAGRAM



Direct Write™ and Block Lock™ Protection is a trademark of Xicor, Inc.

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# X25330

## PIN DESCRIPTIONS

### Serial Output (SO)

SO is a push/pull serial data output pin. During a read cycle, data is shifted out on this pin. Data is clocked out by the falling edge of the serial clock.

### Serial Input (SI)

SI is the serial data input pin. All opcodes, byte addresses, and data to be written to the memory are input on this pin. Data is latched by the rising edge of the serial clock.

### Serial Clock (SCK)

The Serial Clock controls the serial bus timing for data input and output. Opcodes, addresses, or data present on the SI pin are latched on the rising edge of the clock input, while data on the SO pin change after the falling edge of the clock input.

### Chip Select ( $\overline{CS}$ )

When  $\overline{CS}$  is HIGH, the X25330 is deselected and the SO output pin is at high impedance and unless an internal write operation is underway, the X25330 will be in the standby power mode.  $\overline{CS}$  LOW enables the X25330, placing it in the active power mode. It should be noted that after power-up, a HIGH to LOW transition on  $\overline{CS}$  is required prior to the start of any operation.

### Write Protect ( $\overline{WP}$ )

When  $\overline{WP}$  is LOW and the nonvolatile bit WPEN is "1", nonvolatile writes to the X25330 status register are disabled, but the part otherwise functions normally. When  $\overline{WP}$  is held HIGH, all functions, including nonvolatile writes operate normally.  $\overline{WP}$  going LOW while  $\overline{CS}$  is still LOW will interrupt a write to the

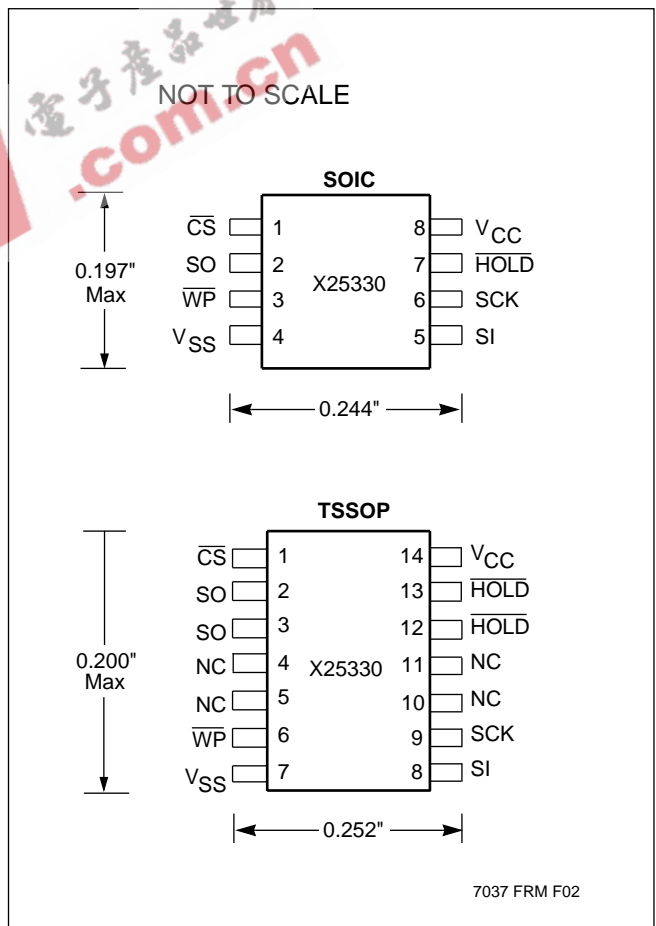
X25330 status register. If the internal write cycle has already been initiated,  $\overline{WP}$  going LOW will have no effect on a write.

The  $\overline{WP}$  pin function is blocked when the WPEN bit in the status register is "0". This allows the user to install the X25330 in a system with  $\overline{WP}$  pin grounded and still be able to write to the status register. The  $\overline{WP}$  pin functions will be enabled when the WPEN bit is set "1".

### Hold (HOLD)

HOLD is used in conjunction with the  $\overline{CS}$  pin to pause the device. Once the part is selected and a serial sequence is underway, HOLD may be used to pause

## PIN CONFIGURATION



## PIN NAMES

Symbol	Description
$\overline{CS}$	Chip Select Input
SO	Serial Output
SI	Serial Input
SCK	Serial Clock Input
$\overline{WP}$	Write Protect Input
V <sub>SS</sub>	Ground
V <sub>CC</sub>	Supply Voltage
HOLD	Hold Input
NC	No Connect

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\* Pin 2 and Pin 3 are internally connected. Only one  $\overline{CS}$  needs to be connected externally.

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the serial communication with the controller without resetting the serial sequence. To pause,  $\overline{\text{HOLD}}$  must be brought LOW while SCK is LOW. To resume communication,  $\overline{\text{HOLD}}$  is brought HIGH, again while SCK is LOW. If the pause feature is not used,  $\overline{\text{HOLD}}$  should be held HIGH at all times.

### PRINCIPLES OF OPERATION

The X25330 is a 4K x 8 E<sup>2</sup>PROM designed to interface directly with the synchronous serial peripheral interface (SPI) of many popular microcontroller families.

The X25330 contains an 8-bit instruction register. It is accessed via the SI input, with data being clocked in on the rising SCK.  $\overline{\text{CS}}$  must be LOW and the  $\overline{\text{HOLD}}$  and  $\overline{\text{WP}}$  inputs must be HIGH during the entire operation.

Table 1 contains a list of the instructions and their opcodes. All instructions, addresses and data are transferred MSB first.

Data input is sampled on the first rising edge of SCK after  $\overline{\text{CS}}$  goes LOW. SCK is static, allowing the user to stop the clock and then resume operations. If the clock line is shared with other peripheral devices on the SPI bus, the user can assert the  $\overline{\text{HOLD}}$  input to place the X25330 into a "PAUSE" condition. After releasing  $\overline{\text{HOLD}}$ , the X25330 will resume operation from the point when  $\overline{\text{HOLD}}$  was first asserted.

#### Write Enable Latch

The X25330 contains a "write enable" latch. This latch must be SET before a write operation will be completed internally. The WREN instruction will set the latch and the WRDI instruction will reset the latch. This latch is automatically reset upon a power-up condition and after the completion of a byte, page, or status register write cycle.

### Status Register

The RDSR instruction provides access to the status register. The status register may be read at any time, even during a write cycle. The status register is formatted as follows:

7	6	5	4	3	2	1	0
WPEN	X	X	X	BL1	BL0	WEL	WIP

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WPEN, BL0 and BL1 are set by the WRSR instruction. WEL and WIP are read-only and automatically set by other operations.

The Write-In-Process (WIP) bit indicates whether the X25330 is busy with a write operation. When set to a "1", a write is in progress, when set to a "0", no write is in progress. During a write, all other bits are set to "1".

The Write Enable Latch (WEL) bit indicates the status of the "write enable" latch. When set to a "1", the latch is set, when set to a "0", the latch is reset.

The Block Lock (BL0 and BL1) bits are nonvolatile and allow the user to select one of four levels of protection. The X25330 is divided into four 8K bit segments. One, two, or all four of the segments may be protected. That is, the user may read the segments but will be unable to alter (write) data within the selected segments. The partitioning is controlled as illustrated below.

Status Register Bits		Array Addresses Protected
BL1	BL0	
0	0	None
0	1	\$0C00-\$0FFF
1	0	\$0800-\$0FFF
1	1	\$0000-\$0FFF

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**Table 1. Instruction Set**

Instruction Name	Instruction Format*	Operation
WREN	0000 0110	Set the Write Enable Latch (Enable Write Operations)
WRDI	0000 0100	Reset the Write Enable Latch (Disable Write Operations)
RDSR	0000 0101	Read Status Register
WRSR	0000 0001	Write Status Register
READ	0000 0011	Read Data from Memory Array beginning at selected address
WRITE	0000 0010	Write Data to Memory Array beginning at Selected Address (1 to 32 Bytes)

\*Instructions are shown MSB in leftmost position. Instructions are transferred MSB first.

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The Write-Protect-Enable (WPEN) bit is available for the X25330 as a nonvolatile enable bit for the  $\overline{WP}$  pin.

WPEN	$\overline{WP}$	WEL	Protected Blocks	Unprotected Blocks	Status Register
0	X	0	Protected	Protected	Protected
0	X	1	Protected	Writable	Writable
1	LOW	0	Protected	Protected	Protected
1	LOW	1	Protected	Writable	Protected
X	HIGH	0	Protected	Protected	Protected
X	HIGH	1	Protected	Writable	Writable

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### Programmable Hardware Write Protection

The Write Protect ( $\overline{WP}$ ) pin and the nonvolatile Write Protect Enable (WPEN) bit in the Status Register control the Programmable Hardware Write Protect feature. Hardware Write Protection is enabled when  $\overline{WP}$  pin is LOW, and the WPEN bit is “1”. Hardware Write Protection is disabled when either the  $\overline{WP}$  pin is HIGH or the WPEN bit is “0”. When the chip is hardware write protected, nonvolatile writes are disabled to the Status Register, including the Block Lock bits and the WPEN bit itself, as well as the block-protected sections in the memory array. Only the sections of the memory array that are not block-protected can be written.

### In Circuit Programmable ROM Mode

Note that since the WPEN bit is write protected, it cannot be changed back to a LOW state; so write protection is enabled as long as the WP pin is held LOW. Thus an In Circuit Programmable ROM function can be implemented by hardwiring the WP pin to Vss, writing to and Block Locking the desired portion of the array to be ROM, and then programming the WPEN bit HIGH. The table above defines the program protect status for each combination of WPEN and  $\overline{WP}$ .

### Clock and Data Timing

Data input on the SI line is latched on the rising edge of SCK. Data is output on the SO line by the falling edge of SCK.

### Read Sequence

When reading from the E<sup>2</sup>PROM memory array,  $\overline{CS}$  is first pulled LOW to select the device. The 8-bit READ instruction is transmitted to the X25330, followed by the 16-bit address of which the last 12 are used. After the READ opcode and address are sent, the data stored in the memory at the selected address is shifted out on the SO line. The data stored in memory

at the next address can be read sequentially by continuing to provide clock pulses. The address is automatically incremented to the next higher address after each byte of data is shifted out. When the highest address is reached (\$0FFF) the address counter rolls over to address \$0000 allowing the read cycle to be continued indefinitely. The read operation is terminated by taking  $\overline{CS}$  HIGH. Refer to the read E<sup>2</sup>PROM array operation sequence illustrated in Figure 1.

To read the status register the  $\overline{CS}$  line is first pulled LOW to select the device followed by the 8-bit RDSR instruction. After the RDSR opcode is sent, the contents of the status register are shifted out on the SO line. Figure 2 illustrates the read status register sequence.

### Write Sequence

Prior to any attempt to write data into the X25330, the “Write Enable” latch must first be set by issuing the WREN instruction (See Figure 3).  $\overline{CS}$  is first taken LOW, then the WREN instruction is clocked into the X25330. After all eight bits of the instruction are transmitted,  $\overline{CS}$  must then be taken HIGH. If the user continues the write operation without taking  $\overline{CS}$  HIGH after issuing the WREN instruction, the write operation will be ignored.

To write data to the E<sup>2</sup>PROM memory array, the user issues the WRITE instruction, followed by the address and then the data to be written. This is minimally a thirty-two clock operation.  $\overline{CS}$  must go LOW and remain LOW for the duration of the operation. The host may continue to write up to 32 bytes of data to the X25330. The only restriction is the 32 bytes must reside on the same page. If the address counter reaches the end of the page and the clock continues, the counter will “roll over” to the first address of the page and overwrite any data that may have been written.

For the write operation (byte or page write) to be completed,  $\overline{CS}$  can only be brought HIGH after bit 0 of data byte N is clocked in. If it is brought HIGH at any other time the write operation will not be completed. Refer to Figures 4 and 5 below for a detailed illustration of the write sequences and time frames in which  $\overline{CS}$  going HIGH are valid.

To write to the status register, the WRSR instruction is followed by the data to be written. Data bits 0, 1, 4, 5 and 6 must be “0”. Figure 6 illustrates this sequence.

While the write is in progress following a status register or E<sup>2</sup>PROM write sequence, the status register may be read to check the WIP bit. During this time the WIP bit will be HIGH.

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## Hold Operation

The  $\overline{\text{HOLD}}$  input should be HIGH (at  $V_{IH}$ ) under normal operation. If a data transfer is to be interrupted  $\overline{\text{HOLD}}$  can be pulled LOW to suspend the transfer until it can be resumed. The only restriction is the SCK input must be LOW when  $\overline{\text{HOLD}}$  is first pulled LOW and SCK must also be LOW when  $\overline{\text{HOLD}}$  is released.

The  $\overline{\text{HOLD}}$  input may be tied HIGH either directly to  $V_{CC}$  or tied to  $V_{CC}$  through a resistor.

## Operational Notes

The X25330 powers-up in the following state:

- The device is in the low power standby state.
- A HIGH to LOW transition on  $\overline{\text{CS}}$  is required to enter an active state and receive an instruction.
- SO pin is high impedance.
- The “write enable” latch is reset.

## Data Protection

The following circuitry has been included to prevent inadvertent writes:

- The “write enable” latch is reset upon power-up.
- A WREN instruction must be issued to set the “write enable” latch.
- $\overline{\text{CS}}$  must come HIGH at the proper clock count in order to start a write cycle.

Figure 1. Read E<sup>2</sup>PROM Array Operation Sequence

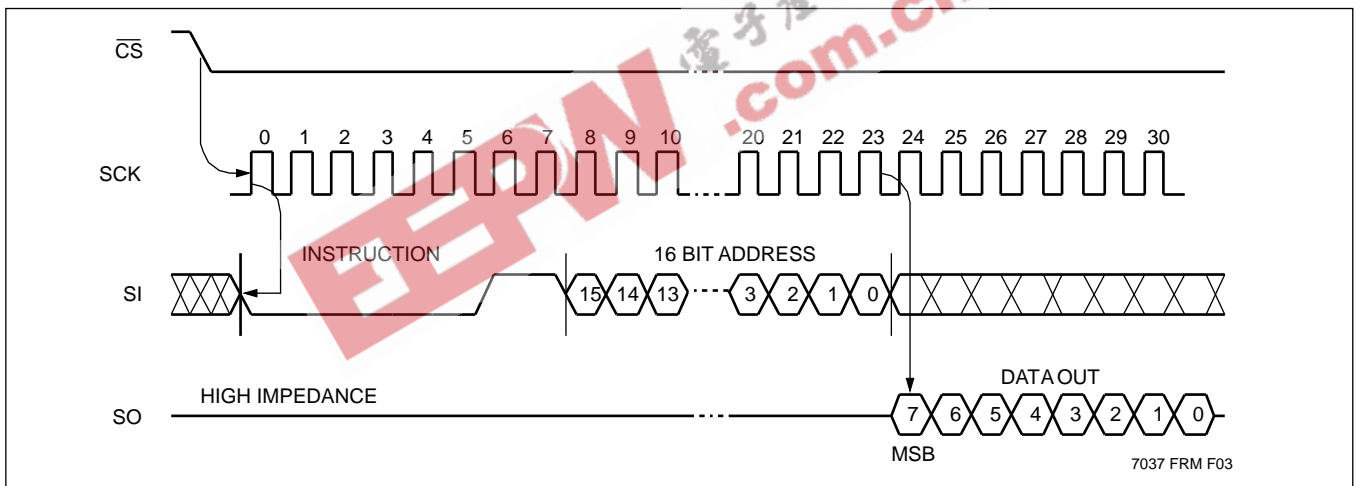
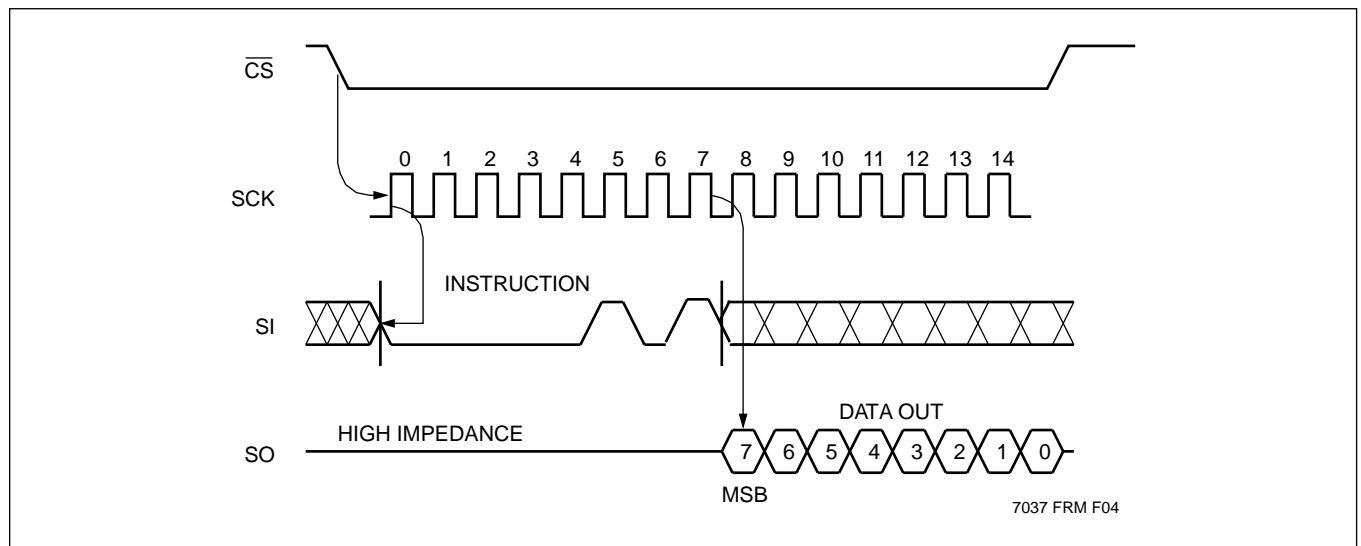


Figure 2. Read Status Register Operation Sequence



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Figure 3. Write Enable Latch Sequence

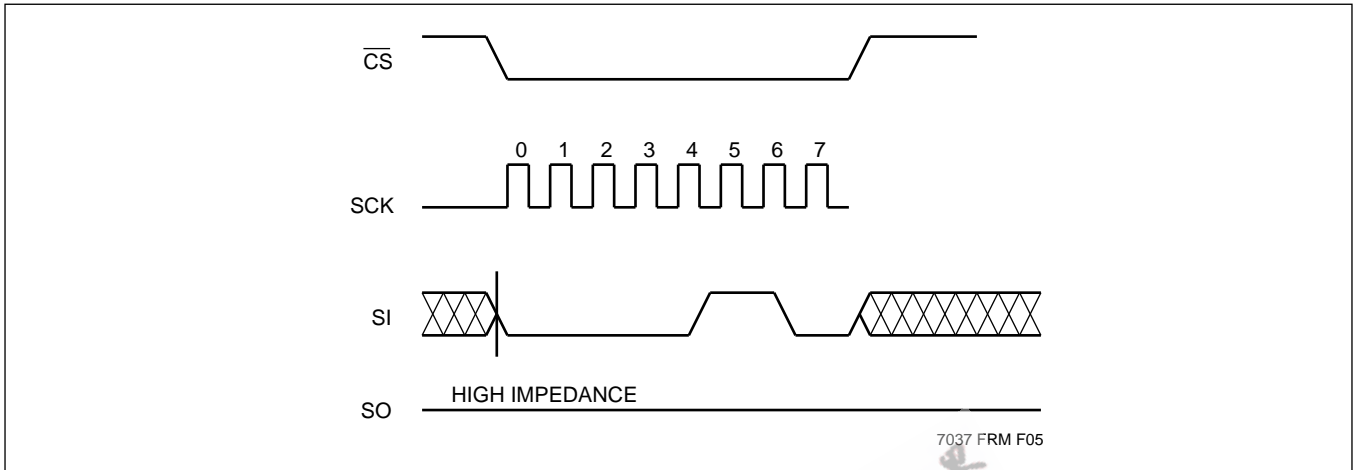
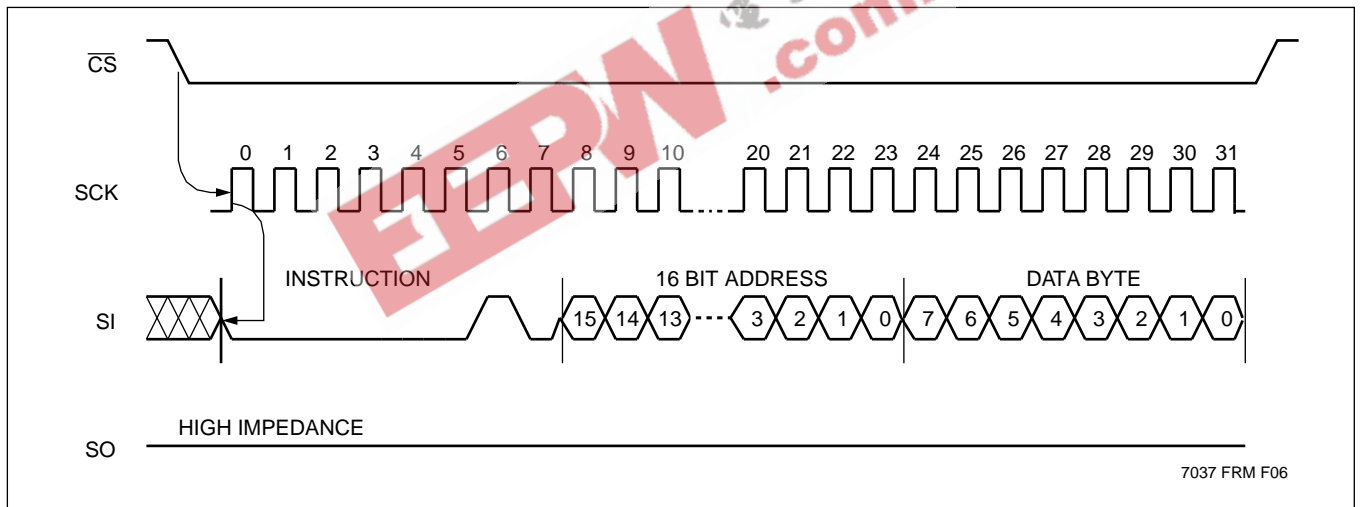


Figure 4. Byte Write Operation Sequence



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Figure 5. Page Write Operation Sequence

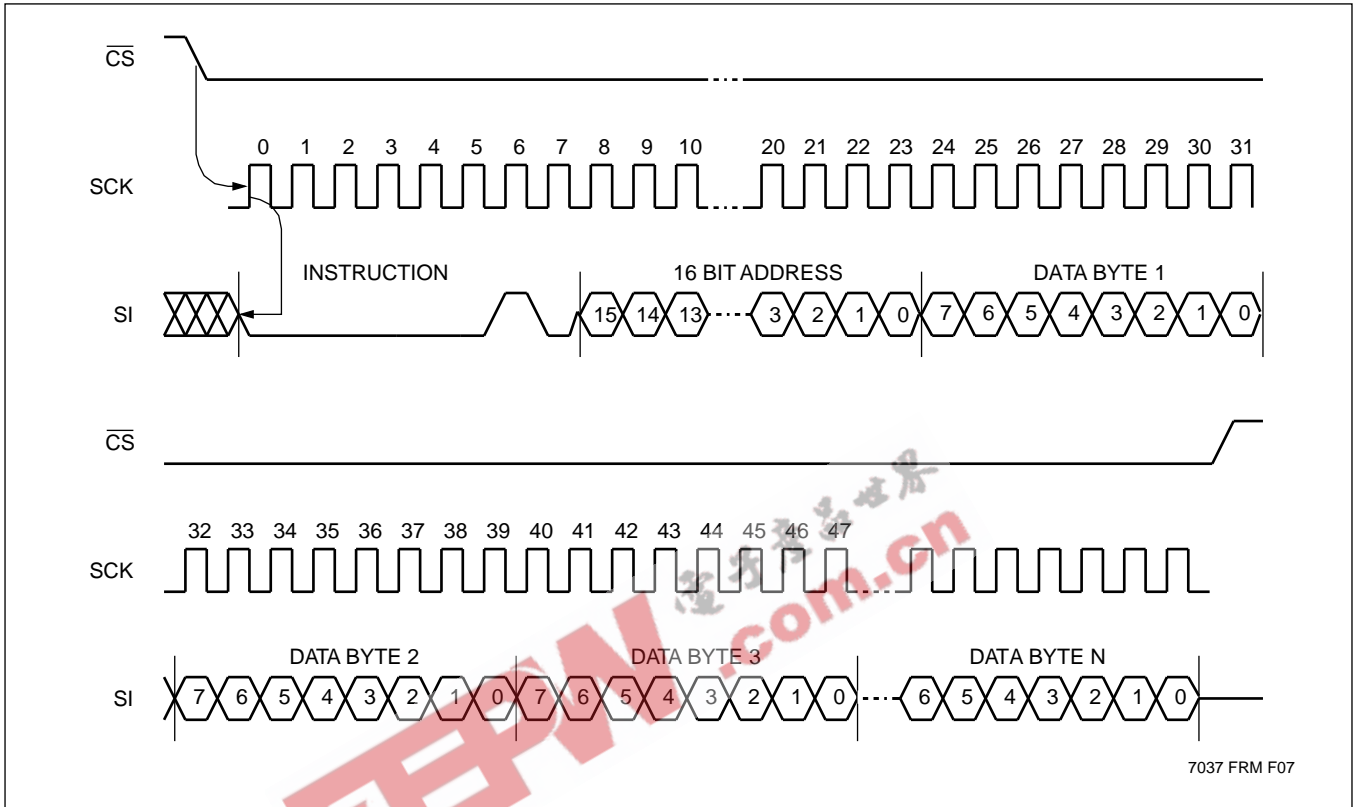
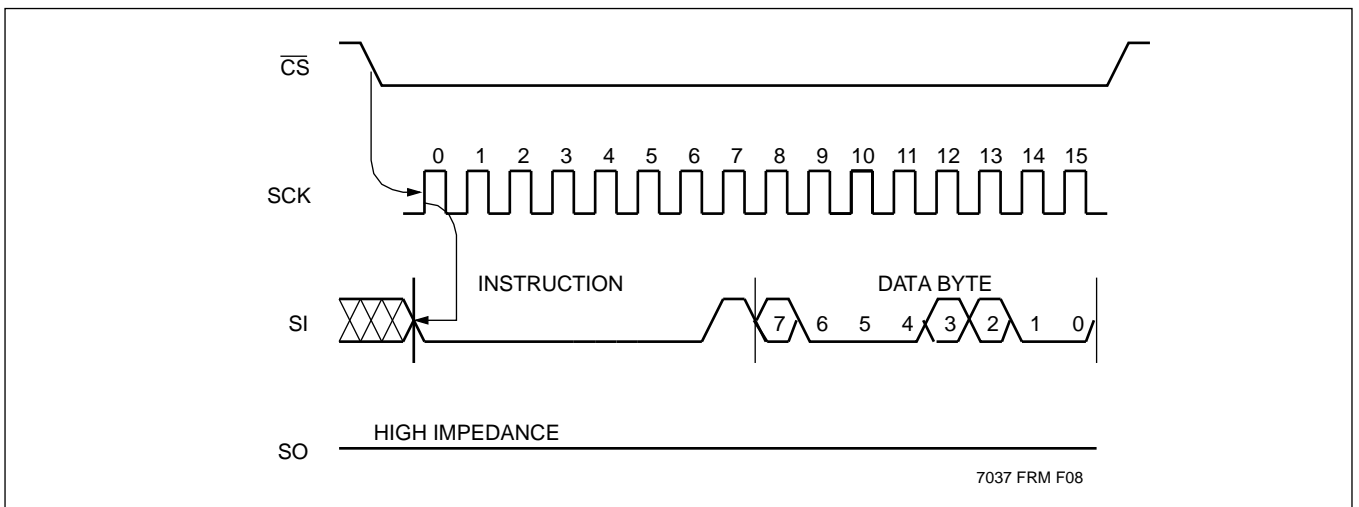


Figure 6. Write Status Register Operation Sequence





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## ABSOLUTE MAXIMUM RATINGS\*

Temperature under Bias.....-65°C to +135°C  
 Storage Temperature .....-65°C to +150°C  
 Voltage on any Pin with Respect to  $V_{SS}$  .....-1V to +7V  
 D.C. Output Current ..... 5mA  
 (Soldering, 10 seconds) .....300°C

## \*COMMENT

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	+70°C
Industrial	-40°C	+85°C

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Supply Voltage	Limits
X25330	5V ±10%
X25330-2.5	2.5V to 5.5V

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## D.C. OPERATING CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
$I_{CC}$	$V_{CC}$ Supply Current (Active)		5	mA	$SCK = V_{CC} \times 0.1 / V_{CC} \times 0.9 @ 5MHz,$
$I_{SB}$	$V_{CC}$ Supply Current (Standby)		1	$\mu A$	$\overline{CS} = V_{CC}, V_{IN} = V_{SS} \text{ or } V_{CC} - 0.3V$
$I_{LI}$	Input Leakage Current		10	$\mu A$	$V_{IN} = V_{SS} \text{ to } V_{CC}$
$I_{LO}$	Output Leakage Current		10	$\mu A$	$V_{OUT} = V_{SS} \text{ to } V_{CC}$
$V_{IL}^{(1)}$	Input LOW Voltage	-1	$V_{CC} \times 0.3$	V	
$V_{IH}^{(1)}$	Input HIGH Voltage	$V_{CC} \times 0.7$	$V_{CC} + 0.5$	V	
$V_{OL1}$	Output LOW Voltage		0.4	V	$I_{OL} = 3mA, V_{CC} = 5V$
$V_{OH1}$	Output HIGH Voltage	$V_{CC} - 0.8$		V	$I_{OH} = -1.6mA, V_{CC} = 5V$
$V_{OL2}$	Output LOW Voltage		0.4	V	$I_{OL} = 1.5mA, V_{CC} = 3V$
$V_{OH2}$	Output HIGH Voltage	$V_{CC} - 0.3$		V	$I_{OH} = -0.4mA, V_{CC} = 3V$

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## POWER-UP TIMING

Symbol	Parameter	Min.	Max.	Units
$T_{PUR}^{(3)}$	Power-up to Read Operation		1	ms
$T_{PUW}^{(3)}$	Power-up to Write Operation		1	ms

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## CAPACITANCE $T_A = +25^\circ C, f = 1MHz, V_{CC} = 5V$

Symbol	Parameter	Max.	Units	Test Conditions
$C_{I/O}^{(3)}$	Output Capacitance (SO)	8	pF	$V_{I/O} = 0V$
$C_{IN}^{(3)}$	Input Capacitance (SCK, SI, $\overline{CS}$ , WP, HOLD)	6	pF	$V_{IN} = 0V$

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Notes: (1)  $V_{IL}$  min. and  $V_{IH}$  max. are for reference only and are not tested.

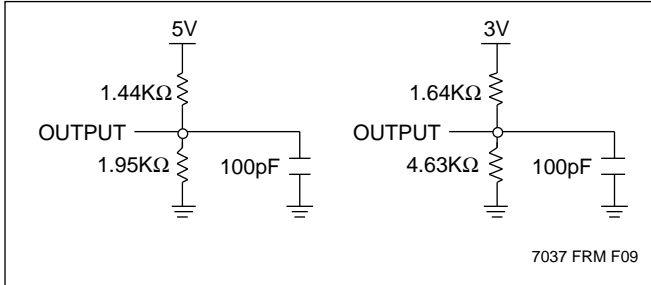
(2) This parameter is periodically sampled and not 100% tested.

(3)  $t_{PUR}$  and  $t_{PUW}$  are the delays required from the time  $V_{CC}$  is stable until the specified operation can be initiated. These parameters are periodically sampled and not 100% tested.



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## EQUIVALENT A.C. LOAD CIRCUIT



## A.C. CONDITIONS OF TEST

Input Pulse Levels	$V_{CC} \times 0.1$ to $V_{CC} \times 0.9$
Input Rise and Fall Times	10ns
Input and Output Timing Levels	$V_{CC} \times 0.5$

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## A.C. OPERATING CHARACTERISTICS

### Data Input Timing

Symbol	Parameter	Min.	Max.	Units
$f_{SCK}$	Clock Frequency	0	5	MHz
$t_{CYC}$	Cycle Time	200		ns
$t_{LEAD}$	$\overline{CS}$ Lead Time	100		ns
$t_{LAG}$	$\overline{CS}$ Lag Time	100		ns
$t_{WH}$	Clock HIGH Time	80		ns
$t_{WL}$	Clock LOW Time	80		ns
$t_{SU}$	Data Setup Time	20		ns
$t_H$	Data Hold Time	20		ns
$t_{RI}^{(4)}$	Data In Rise Time		2	$\mu s$
$t_{FI}^{(4)}$	Data In Fall Time		2	$\mu s$
$t_{HD}$	HOLD Setup Time	40		ns
$t_{CD}$	$\overline{HOLD}$ Hold Time	40		ns
$t_{CS}$	$\overline{CS}$ Deselect Time	100		ns
$t_{WC}^{(5)}$	Write Cycle Time		10	ms

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### Data Output Timing

Symbol	Parameter	Min.	Max.	Units
$f_{SCK}$	Clock Frequency	0	5	MHz
$t_{DIS}$	Output Disable Time		100	ns
$t_V$	Output Valid from Clock LOW		80	ns
$t_{HO}$	Output Hold Time	0		ns
$t_{RO}^{(4)}$	Output Rise Time		50	ns
$t_{FO}^{(4)}$	Output Fall Time		50	ns
$t_{LZ}^{(4)}$	$\overline{HOLD}$ HIGH to Output in Low Z	50		ns
$t_{HZ}^{(4)}$	$\overline{HOLD}$ LOW to Output in High Z	50		ns

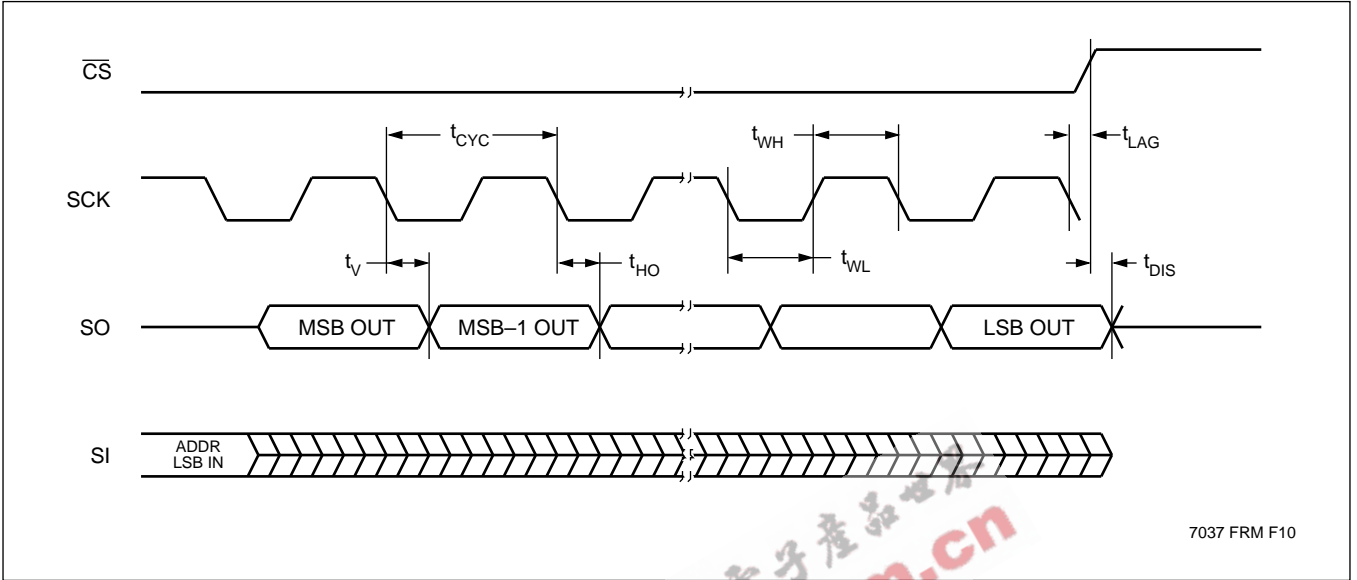
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**Notes:** (4) This parameter is periodically sampled and not 100% tested.

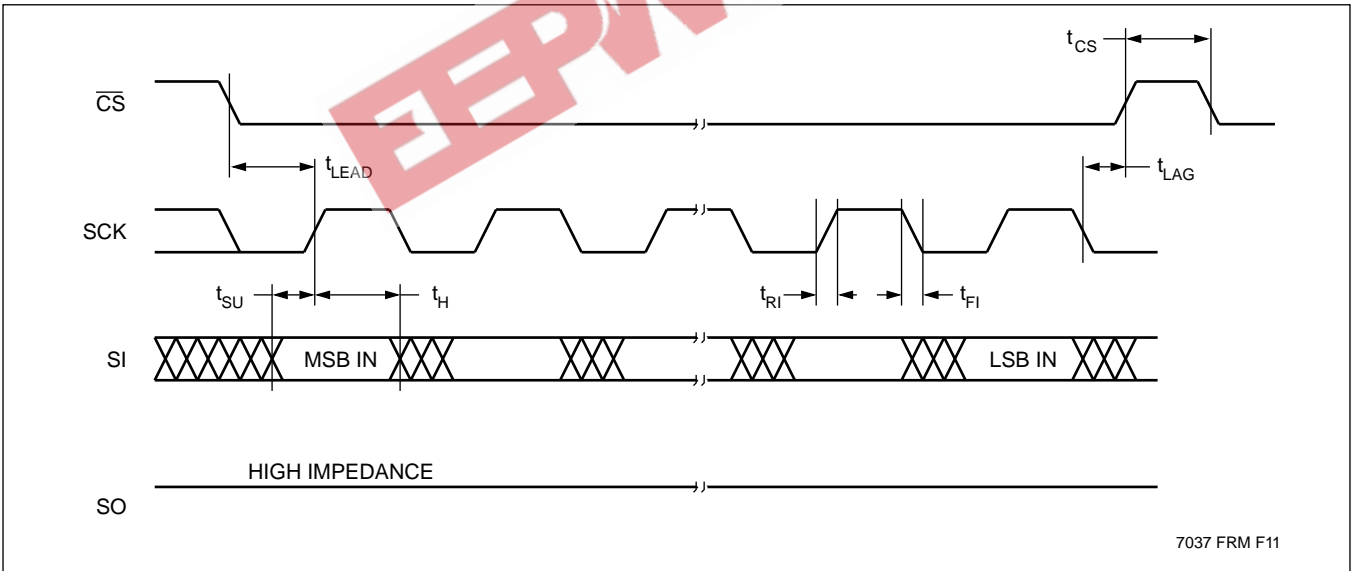
(5)  $t_{WC}$  is the time from the rising edge of  $\overline{CS}$  after a valid write sequence has been sent to the end of the self-timed internal nonvolatile write cycle.

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## Serial Output Timing

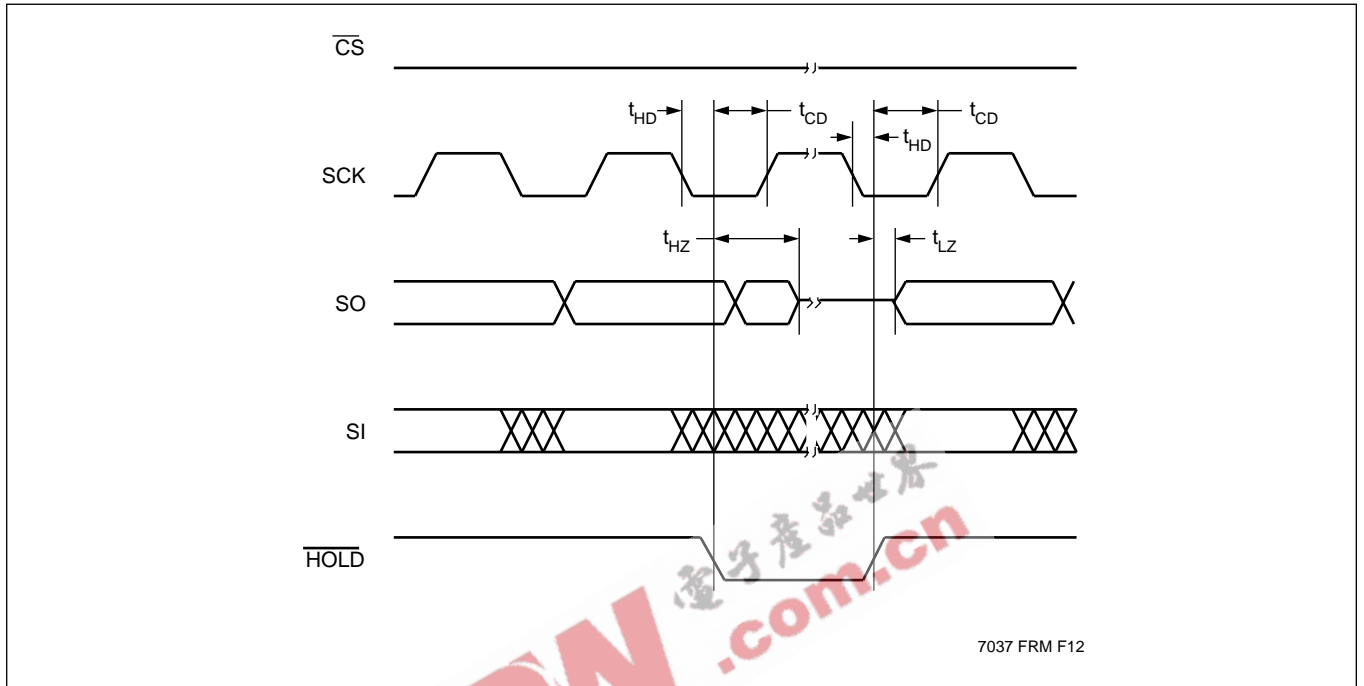


## Serial Input Timing



# X25330

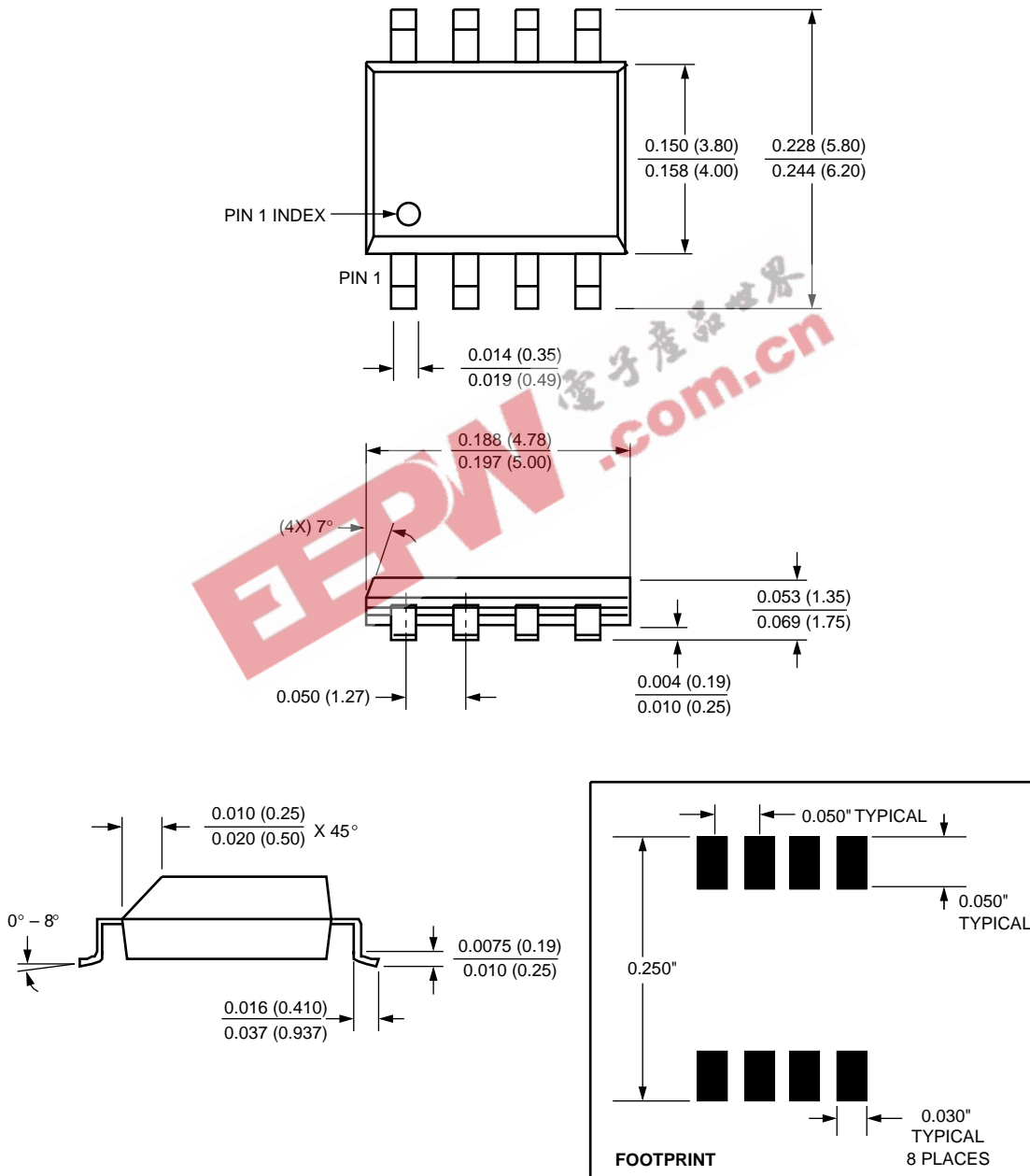
## Hold Timing



# X25330

## PACKAGING INFORMATION

### 8-LEAD PLASTIC SMALL OUTLINE GULL WING PACKAGE TYPE S



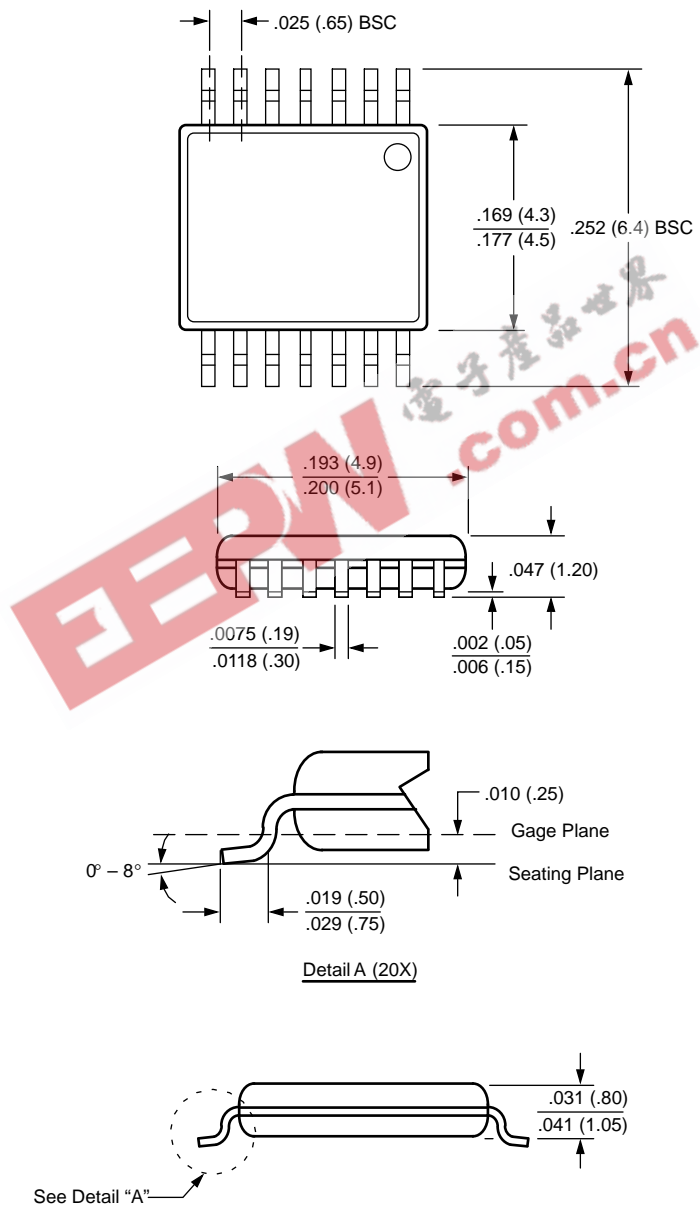
NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

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## PACKAGING INFORMATION

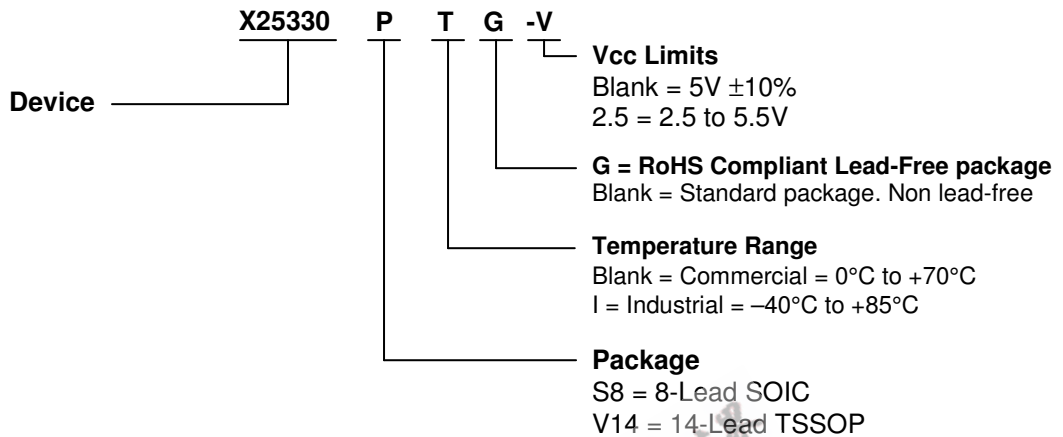
### 14-LEAD PLASTIC, TSSOP, PACKAGE TYPE V



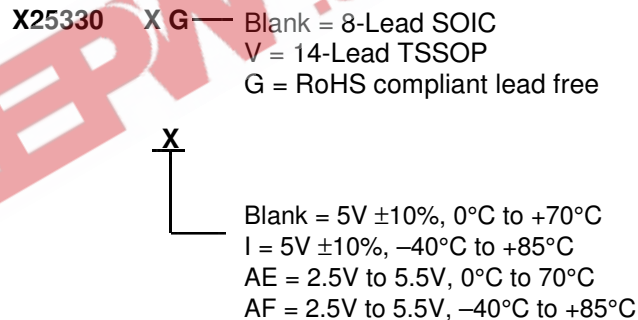
NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

# X25330

## ORDERING INFORMATION



## PART MARK CONVENTION



## LIMITED WARRANTY

Devices sold by Xicor, Inc. are covered by the warranty and patent indemnification provisions appearing in its Terms of Sale only. Xicor, Inc. makes no warranty, express, statutory, implied, or by description regarding the information set forth herein or regarding the freedom of the described devices from patent infringement. Xicor, Inc. makes no warranty of merchantability or fitness for any purpose. Xicor, Inc. reserves the right to discontinue production and change specifications and prices at any time and without notice.

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## U.S. PATENTS

Xicor products are covered by one or more of the following U.S. Patents: 4,263,664; 4,274,012; 4,300,212; 4,314,265; 4,326,134; 4,393,481; 4,404,475; 4,450,402; 4,486,769; 4,488,060; 4,520,461; 4,533,846; 4,599,706; 4,617,652; 4,668,932; 4,752,912; 4,829, 482; 4,874, 967; 4,883, 976. Foreign patents and additional patents pending.

## LIFE RELATED POLICY

In situations where semiconductor component failure may endanger life, system designers using this product should design the system with appropriate error detection and correction, redundancy and back-up features to prevent such an occurrence.

Xicor's products are not authorized for use in critical components in life support devices or systems.

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.

2.A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.