APPLICATION NOTES
AVAILABLE
AN11 • AN21

4K X25043/45 512 x 8 Bit

Programmable Watchdog Supervisory E²PROM

FEATURES

- Programmable Watchdog Timer
- Low V_{CC} Detection
- Reset Signal Valid to V_{CC} = 1V
- 1MHz Clock Rate
- 512 X 8 Bits Serial E²PROM
  - —4 Byte Page Mode
- Low Power CMOS
  - —50µA Standby Current
  - —3mA Active Current
- 2.7V To 5.5V Power Supply
- Block Lock™
  - —Protect 1/4, 1/2 or all of E²PROM Array
- Built-in Inadvertent Write Protection
  - —Power-Up/Power-Down protection circuitry
  - —Write Latch
  - —Write Protect Pin
- High Reliability
  - —Endurance: 100,000 cycles per byte
  - —Data Retention: 100 Years
  - —ESD protection: 2000V on all pins
- Available Packages
  - —8-Lead PDIP
  - —8-Lead SOIC
  - —14-Lead TSSOP
- X25043 = Active LOW $\overline{\text{RESET}}$
- X25045 = Active HIGH RESET

DESCRIPTION

The X25043/45 combines three popular functions, Watchdog Timer, Voltage Supervision, and E²PROM in a single package. This combination lowers the system cost and reduces the board space requirements.

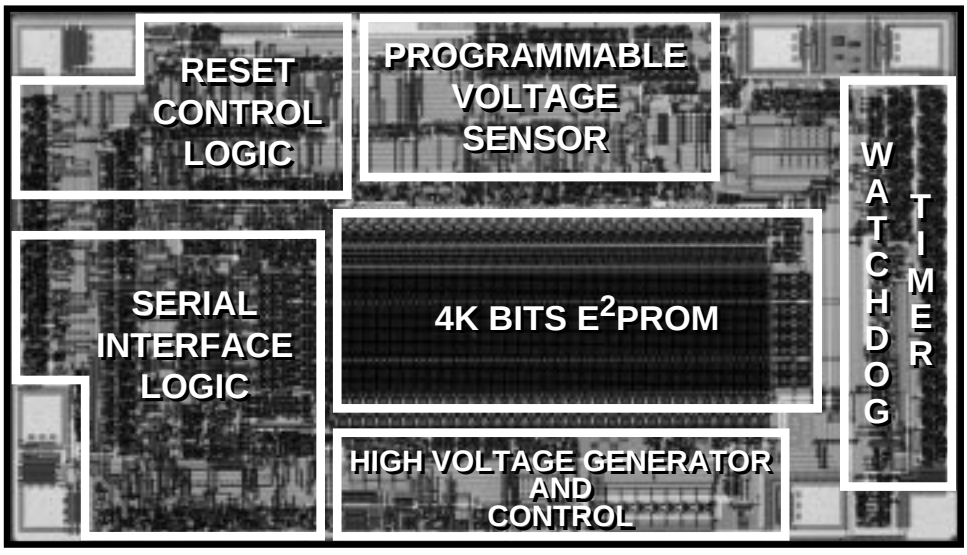
The Watchdog Timer provides an independent protection system for microcontrollers. During a system failure, the X25043/45 watchdog will respond with a $\overline{\text{RESET}}$/RESET signal after a selectable time-out interval. The user selects the interval from three preset values. Once selected, the interval does not change, even after cycling the power.

The system is protected from low voltage conditions by the X25043/45 low V_{CC} detection circuits. When V_{CC} drops below the minimum V_{CC} trip point, the system is reset. Reset is asserted until V_{CC} returns and stabilizes.

The memory portion of the X25043/45 is a CMOS 4096-bit serial E²PROM, internally organized as 512 X 8. The X25043/45 features a Serial Peripheral Interface (SPI) and software protocol allowing operation on a simple three-wire bus.

The X25043/45 utilizes Xicor's proprietary Direct Write™ cell, providing a minimum endurance of 100,000 cycles per byte and a minimum data retention of 100 years.

DIE PHOTOGRAPH



3844 ILL F01

Direct Write™ is a trademark of Xicor, Inc.

PIN DESCRIPTIONS

Serial Output (SO)

SO is a push/pull serial data output pin. During a read cycle, data is shifted out on this pin. Data is clocked out by the falling edge of the serial clock.

Serial Input (SI)

SI is the serial data input pin. All opcodes, byte addresses, and data to be written to the memory are input on this pin. Data is latched by the rising edge of the serial clock.

Serial Clock (SCK)

The Serial Clock controls the serial bus timing for data input and output. Opcodes, addresses, or data present on the SI pin is latched on the rising edge of the clock input, while data on the SO pin changes after the falling edge of the clock input.

Chip Select ($\overline{CS}$)

When $\overline{CS}$ is HIGH, the X25043/45 is deselected and the SO output pin is at high impedance and, unless an internal write operation is underway, the X25043/45 will be in the standby power mode. $\overline{CS}$ LOW enables the X25043/45, placing it in the active power mode. It should be noted that after power-up, a HIGH to LOW transition on $\overline{CS}$ is required prior to the start of any operation.

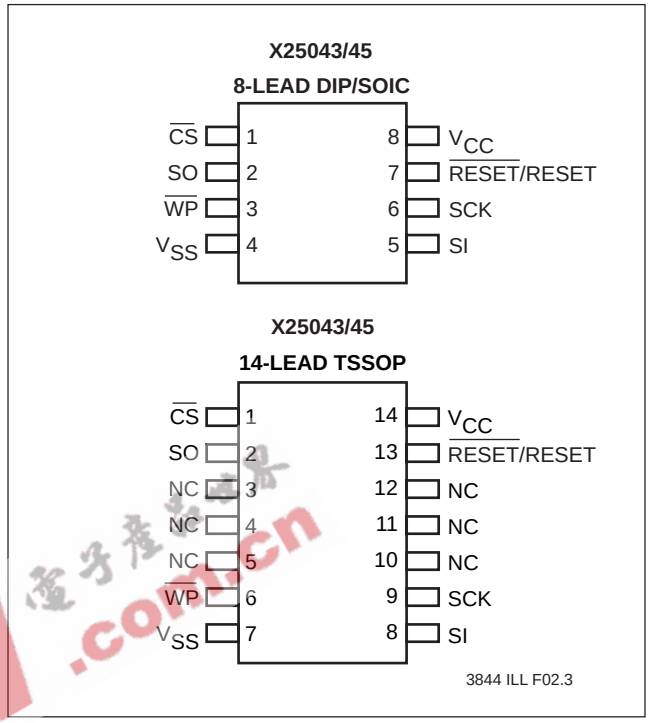
Write Protect ($\overline{WP}$)

When $\overline{WP}$ is LOW, nonvolatile writes to the X25043/45 are disabled, but the part otherwise functions normally. When $\overline{WP}$ is held HIGH, all functions, including nonvolatile writes operate normally. $\overline{WP}$ going LOW while $\overline{CS}$ is still LOW will interrupt a write to the X25043/45. If the internal write cycle has already been initiated, $\overline{WP}$ going LOW will have no affect on a write.

Reset ($\overline{RESET}$, RESET)

X25043/45, $\overline{RESET}$/RESET is an active LOW/HIGH, open drain output which goes active whenever V_{CC} falls below the mimimum V_{CC} sense level. It will remain active until V_{CC} rises above the minimum V_{CC} sense level for 200ms. $\overline{RESET}$/RESET also goes active if the Watchdog timer is enabled and $\overline{CS}$ remains either HIGH or LOW longer than the Watchdog time-out period. A falling edge of $\overline{CS}$ will reset the watchdog timer.

PIN CONFIGURATION



PIN NAMES

Symbol	Description
$\overline{CS}$	Chip Select Input
SO	Serial Output
SI	Serial Input
SCK	Serial Clock Input
$\overline{WP}$	Write Protect Input
V_{SS}	Ground
V_{CC}	Supply Voltage
$\overline{RESET}$/RESET	Reset Output

3844 PGM T01.1

PRINCIPLES OF OPERATION

The X25043/45 is a 512 x 8 E^2PROM designed to interface directly with the synchronous serial peripheral interface (SPI) of many popular microcontroller families.

The X25043/45 contains an 8-bit instruction register. It is accessed via the SI input, with data being clocked in on the rising SCK. $\overline{CS}$ must be LOW and $\overline{WP}$ input must be HIGH during the entire operation. The X25043/45 monitors the bus and provides a $\overline{RESET}$/RESET output if there is no bus activity within the preset time period.

Table 1 contains a list of the instructions and their operation codes. All instructions, addresses and data are transferred MSB first. Bit 3 of the Read and Write instructions contain the higher order address bit, A_8.

Data input is sampled on the first rising edge of SCK after $\overline{CS}$ goes LOW. SCK is static, allowing the user to stop the clock and then resume operations.

Write Enable Latch

The X25043/45 contains a "write enable" latch. This latch must be SET before a write operation will be completed internally. The WREN instruction will set the latch and the WRDI instruction will reset the latch. This latch is automatically reset upon a power-up condition and after the completion of a byte, page, or status register write cycle. The latch is also reset if $\overline{WP}$ is brought LOW.

Status Register

The RDSR instruction provides access to the status register. The status register may be read at any time, even during a write cycle. The status register is formatted as follows:

7	6	5	4	3	2	1	0
X	X	WD1	WD0	BL1	BL0	WEL	WIP

3844 PGM T02

When issuing, WREN, WRDI and RDSR commands, it is not necessary to send a byte address or data.

The Write-In-Process (WIP) bit indicates whether the X25043/45 is busy with a write operation. When set to a "1", a write is in progress, when set to a "0", no write is in progress. During a write, all other bits are set to "1". The WIP bit is read-only.

The Write Enable Latch (WEL) bit indicates the status of the "write enable" latch. When set to a "1", the latch is set, when set to a "0", the latch is reset. The WEL bit is read-only and is set by the WREN instruction and reset by WRDI instruction or successful completion of a write cycle.

The Block Protect (BL0 and BL1) bits indicate the extent of protection employed. These nonvolatile bits are set by issuing the WRSR instruction and allows the user to select one of four levels of protection and program the watchdog timer. The X25043/45 is divided into four 1024-bit segments. One, two, or all four of the segments may be locked. That is, the user may read the segments but will be unable to alter (write) data within the selected segments. The partitioning is controlled as illustrated below with the state of BL1 and BL0.

Status Register Bits		Array Addresses Protected
BL1	BL0	
0	0	None
0	1	$180–$1FF
1	0	$100–$1FF
1	1	$000–$1FF

3844 PGM T04

The Watchdog Timer (WD0 and WD1) bits allow setting of the watchdog time-out function as shown in the table below. These nonvolatile bits are set by issuing the WRSR instruction.

Status Register Bits		Watchdog Time-out (Typical)
WD1	WD0	
0	0	1.4 Seconds
0	1	600 Milliseconds
1	0	200 Milliseconds
1	1	Disabled

3844 PGM T03

Clock and Data Timing

Data input on the SI line is latched on the rising edge of SCK. Data is output on the SO line by the falling edge of SCK.

Read Sequence

When reading from the E^{2}PROM memory array, $\overline{CS}$ is first pulled LOW to select the device. The 8-bit READ instruction is transmitted to the X25043/45, followed by the 8-bit byte address. Bit 3 of the Read instruction contains address A_8. This bit is used to select the upper or lower half of the device. After the read opcode and byte address are sent, the data stored in the memory at the selected address is shifted out on the SO line. The data stored in memory at the next address can be read sequentially by continuing to provide clock pulses. The byte address is automatically incremented to the next higher address after each byte of data is shifted out. When the highest address is reached ($1FF) the address counter rolls over to address $000, allowing the read cycle to be continued indefinitely. The read operation is terminated by taking $\overline{CS}$ HIGH. Refer to the read E^{2}PROM Array operation sequence illustrated in Figure 1.

To read the status register the $\overline{CS}$ line is first pulled LOW to select the device followed by the 8-bit RDSR instruction. After the read status register opcode is sent, the contents of the status register is shifted out on the SO line as shown in Figure 2.

Write Sequence

Prior to any attempt to write data into the X25043/45 the "write enable" latch must first be set by issuing the WREN instruction (See Figure 3). $\overline{CS}$ is first taken LOW, then the WREN instruction is clocked into the X25043/45. After all eight bits of the instruction are transmitted, $\overline{CS}$ must then be taken HIGH. If the user continues the write operation without taking $\overline{CS}$ HIGH after issuing the WREN instruction the write operation will be ignored.

To write data to the E^{2}PROM memory array, the user issues the WRITE instruction, followed by the address and then the data to be written. Bit 3 of the Write instruction contains address A_8. This bit is used to select the upper or lower half of the device. This is minimally a twenty-four clock operation. $\overline{CS}$ must go LOW and remain LOW for the duration of the operation. The host may continue to write up to four bytes of data to the X25043/45. The only restriction is the four bytes must reside on the same page. A page address begins with address X XXXX XX00 and ends with X XXXX XX11. If the byte address counter reaches X XXXX XX11 and the clock continues the counter will roll back to the first address of the page and overwrite any data that may have been written.

For the write operation (byte or page write) to be completed, $\overline{CS}$ can only be brought HIGH after the twenty-fourth, thirty-second, fortieth, or forty-eighth clock. If it is brought HIGH at any other time, the write operation will not be completed. Refer to Figure 4 and 5 below for a detailed illustration of the write sequences.

While the write is in progress, following a status register or E^{2}PROM write sequence the status register may be read to check the WIP bit. During this time the WIP bit will be HIGH and all other bits in the status register will be undefined.

$\overline{RESET}$/RESET Operation

The $\overline{RESET}$ (X25043) output is designed to go LOW whenever V_{CC} has dropped below the minimum trip point and/or the Watchdog timer has reached its programmable time-out limit.

Table 1. Instruction Set

Instruction Name	Instruction Format*	Operation
WREN	0000 0110	Set the Write Enable Latch (Enable Write Operations)
WRDI	0000 0100	Reset the Write Enable Latch (Disable Write Operations)
RDSR	0000 0101	Read Status Register
WRSR	0000 0001	Write Status Register (Block Lock Bits)
READ	0000 $A_8$011	Read Data from Memory Array beginning at selected address
WRITE	0000 $A_8$010	Write Data to Memory Array beginning at Selected Address (1 to 4 Bytes)

3844 PGM T05.1

*Instructions are shown MSB in leftmost position. Instructions are transferred MSB first.

The RESET (X25045) output is designed to go HIGH whenever V_{CC} has dropped below the minimum trip point and/or the watchdog timer has reached its programmable time-out limit.

Operational Notes

The X25043/45 powers-up in the following state:

- The device is in the low power standby state.
- A HIGH to LOW transition on $\overline{CS}$ is required to enter an active state and receive an instruction.
- SO pin is high impedance.
- The “write enable” latch is reset.

Data Protection

The following circuitry has been included to prevent inadvertent writes:

- The “write enable” latch is reset upon power-up.
- A WREN instruction must be issued to set the “write enable” latch.
- $\overline{CS}$ must come HIGH at the proper clock count in order to start a write cycle.

The “write enable” latch is reset when $\overline{WP}$ is brought LOW.

Figure 1. Read E²PROM Array Operation Sequence

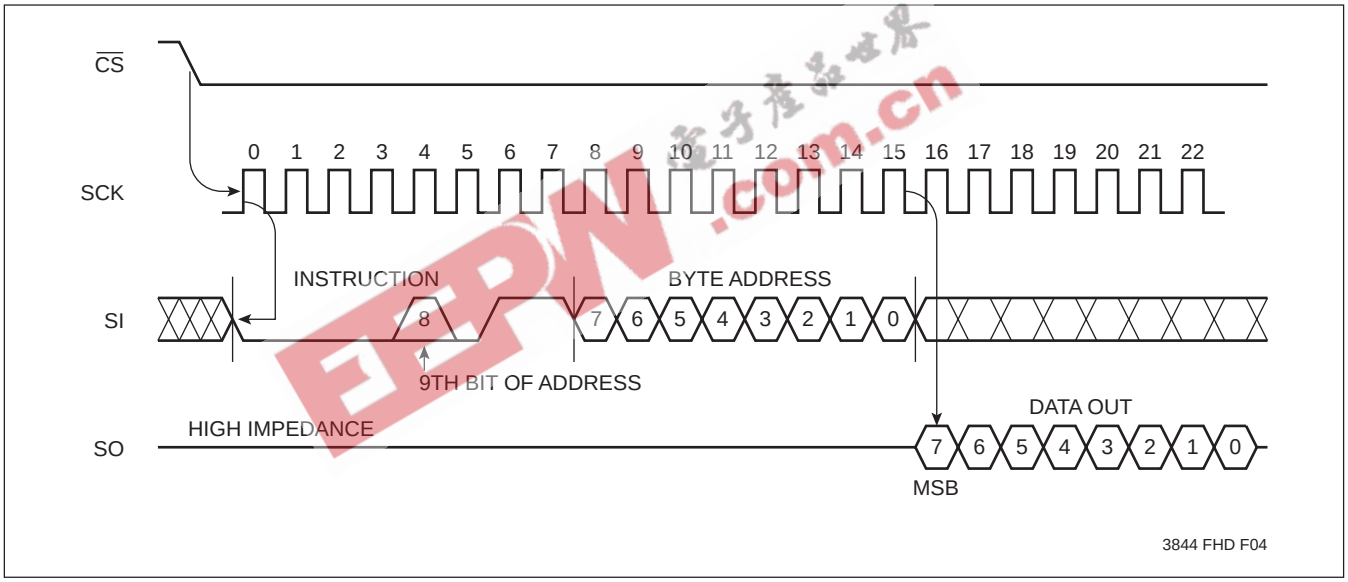


Figure 2. Read Status Register Operation Sequence

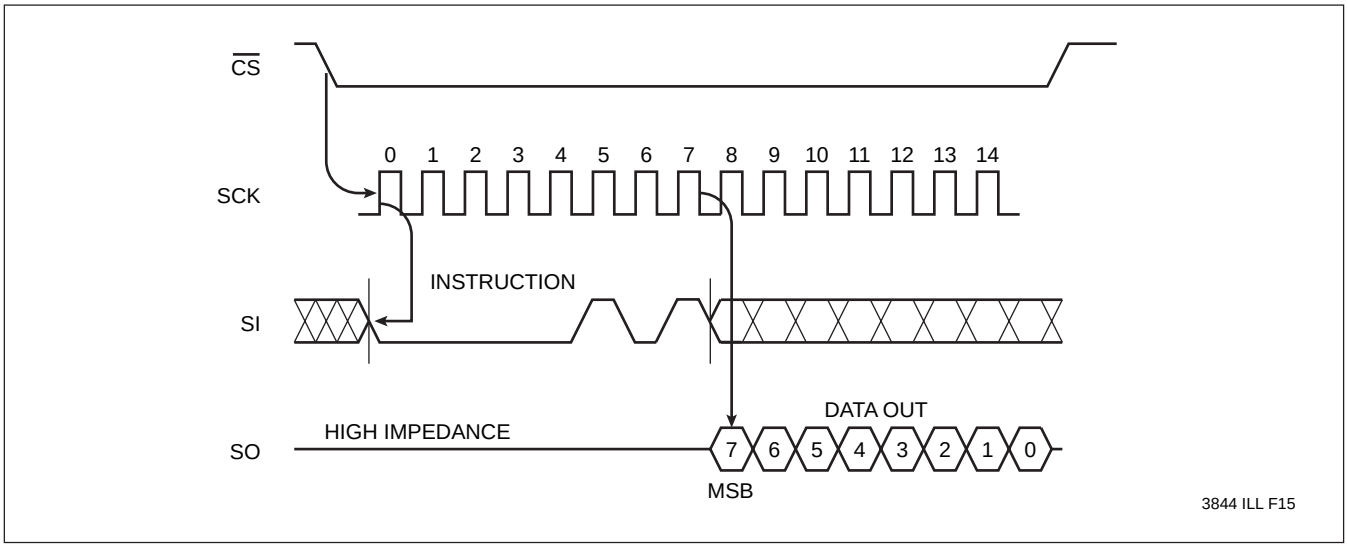


Figure 3. Write Enable Latch Sequence

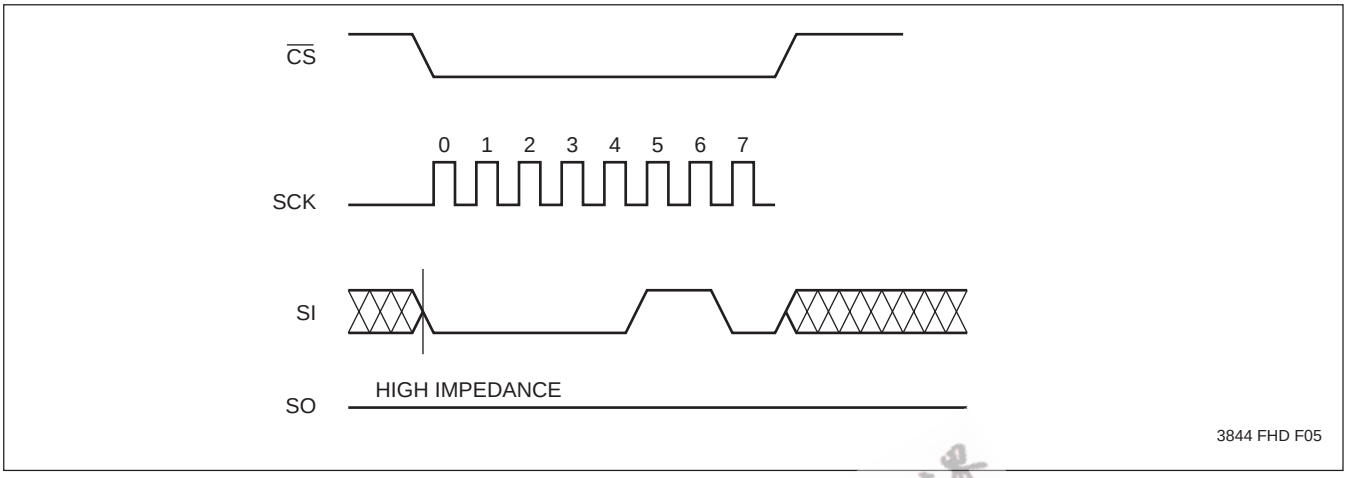
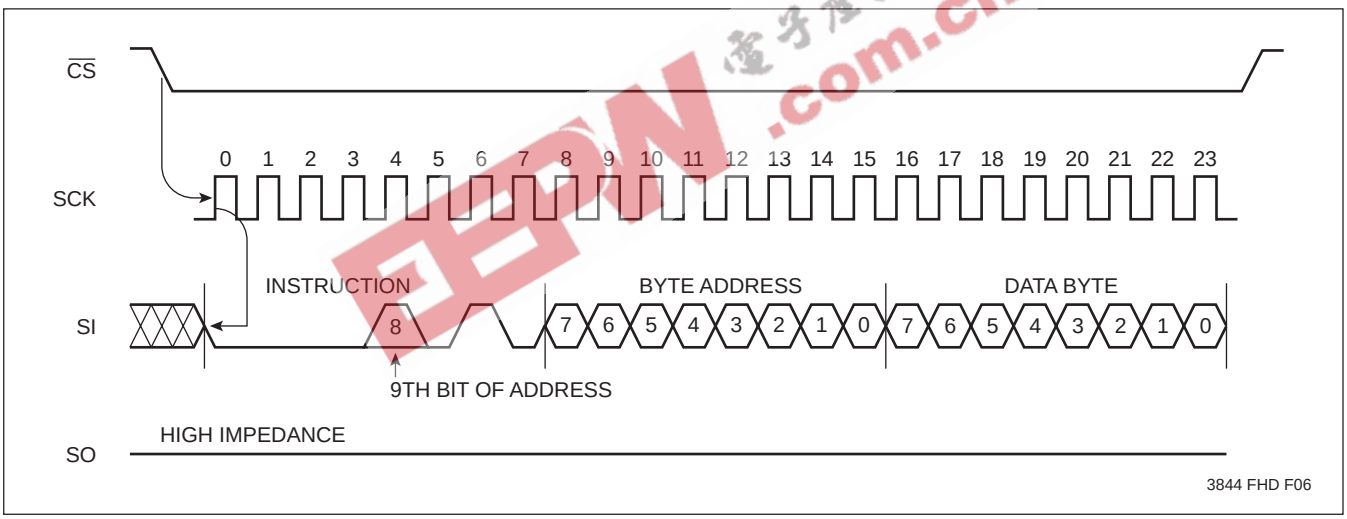


Figure 4. Byte Write Operation Sequence



SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

Figure 5. Page Write Operation Sequence

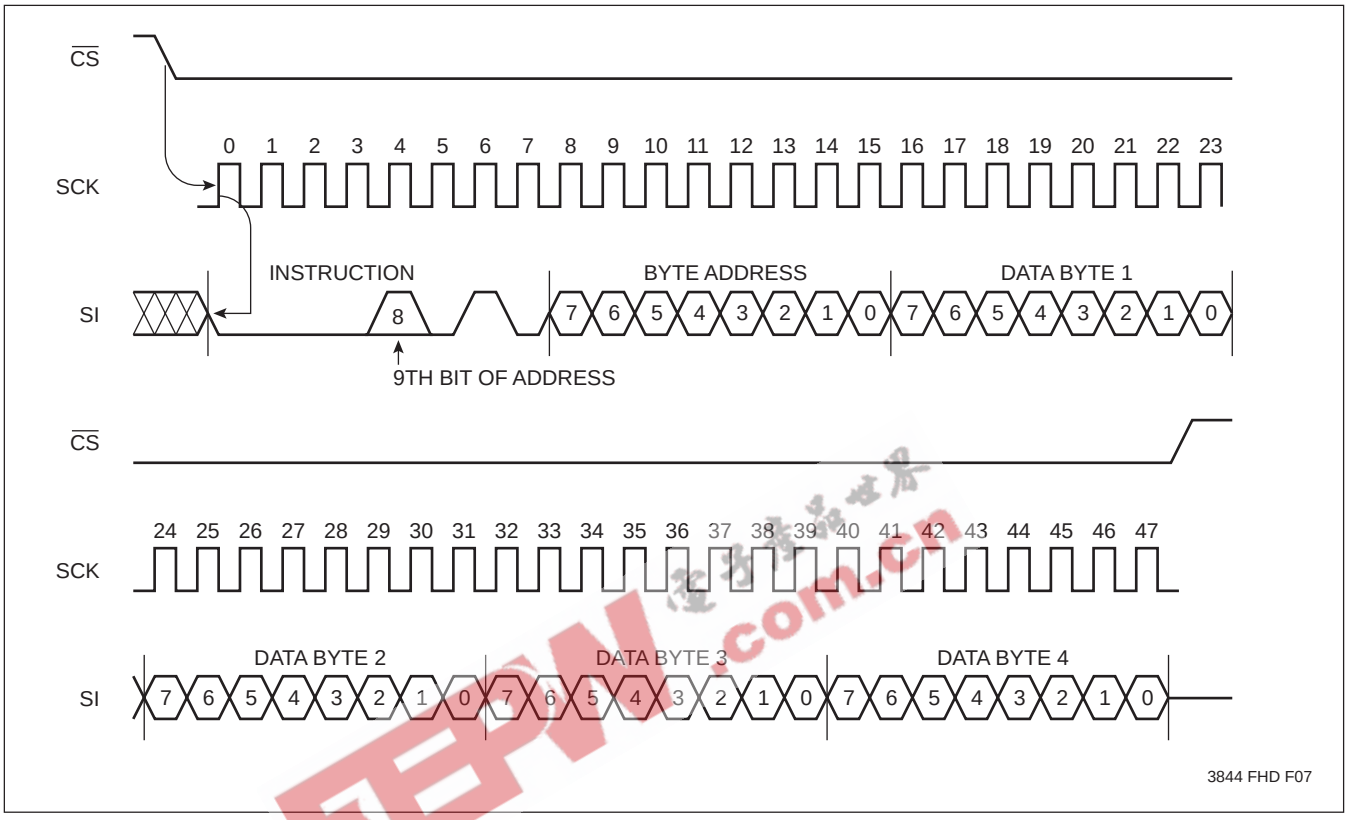
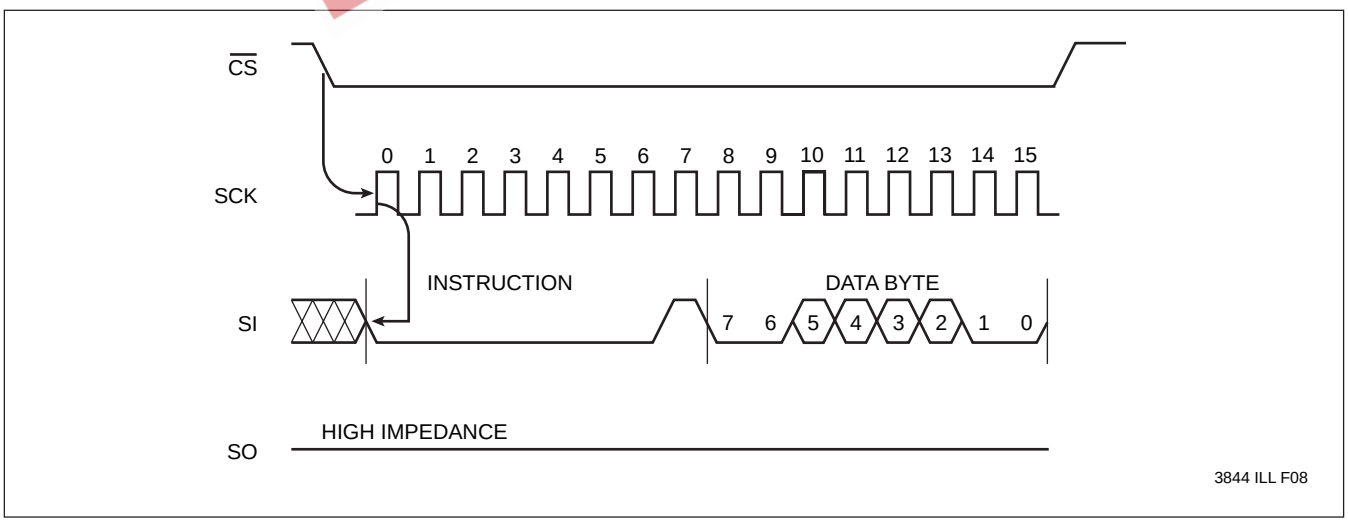


Figure 6. Write Status Register Operation Sequence



ABSOLUTE MAXIMUM RATINGS*

Temperature under Bias ..... –65°C to +135°C
Storage Temperature ..... –65°C to +150°C
Voltage on any Pin with Respect to V_{SS} ..... –1.0V to +7V
D.C. Output Current 5mA
Lead Temperature
(Soldering, 10 seconds) ..... 300°C

***COMMENT**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temp	Min.	Max.
Commercial	0°C	70°C
Industrial	–40°C	+85°C

3844 PGM T06.1

Supply Voltage	Limits
X25043/45	5V ±10%
X25043/45-2.7	2.7 to 5.5V

3844 PGM T07.3

D.C. OPERATING CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I_{CC}	V_{CC} Supply Current (Active)		3	mA	SCK = V_{CC} x 0.1/V_{CC} x 0.9 @ 1MHz, SO = Open
I_{SB1}	V_{CC} Standby Current		50	µA	$\overline{CS}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}, V_{CC} = 5.5
I_{SB2}	V_{CC} Standby Current		20	µA	$\overline{CS}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}, V_{CC} = 2.7V
I_{LI}	Input Leakage Current		10	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output Leakage Current		10	µA	V_{OUT} = V_{SS} to V_{CC}
V_{IL}(1)	Input LOW Voltage	–0.5	V_{CC} x 0.3	V	
V_{IH}(1)	Input HIGH Voltage	V_{CC} x 0.7	V_{CC} + 0.5	V	
V_{OL}	Output LOW Voltage		0.4	V	I_{OL} = 2mA
V_{OH1}	Output HIGH Voltage	V_{CC}–0.8		V	I_{OH} = –1.6mA, V_{CC} = 4.5V
V_{OH2}	Output HIGH Voltage	V_{CC}–0.4		V	I_{OH} = –.4mA, V_{CC} = 2.7V
VOLRS	Reset Output LOW Voltage		0.4	V	I_{OL} = 1mA

3844 PGM T08.3

POWER-UP TIMING

Symbol	Parameter	Min.	Max.	Units
t_{PUR}(2)	Power-up to Read Operation		1	ms
t_{PUW}(2)	Power-up to Write Operation		5	ms

3844 PGM T09

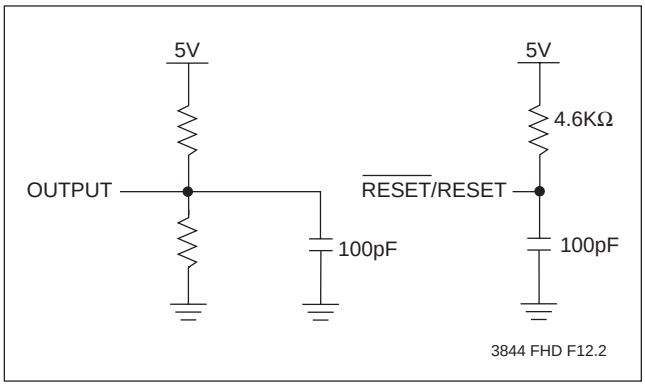
CAPACITANCE T_A = +25°C, f = 1MHz, V_{CC} = 5V.

Symbol	Test	Max.	Units	Conditions
C_{OUT}(2)	Output Capacitance (SO, $\overline{RESET}$, RESET)	8	pF	V_{OUT} = 0V
C_{IN}(2)	Input Capacitance (SCK, SI, $\overline{CS}$, $\overline{WP}$)	6	pF	V_{IN} = 0V

3844 PGM T10.2

Notes: (1) V_{IL} min. and V_{IH} max. are for reference only and are not tested.
(2) This parameter is periodically sampled and not 100% tested.

EQUIVALENT A.C. LOAD CIRCUIT AT 5V VCC



A.C. TEST CONDITIONS

Input Pulse Levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input Rise and Fall Times	10ns
Input and Output Timing Level	V_{CC} x 0.5

3844 PGM T11

A.C. CHARACTERISTICS (Over recommended operating conditions, unless otherwise specified)

Data Input Timing

Symbol	Parameter	Min.	Max.	Units
f_{SCK}	Clock Frequency	0	1	MHz
t_{CYC}	Cycle Time	1000		ns
t_{LEAD}	$\overline{CS}$ Lead Time	500		ns
t_{LAG}	$\overline{CS}$ Lag Time	500		ns
t_{WH}	Clock HIGH Time	500		ns
t_{WL}	Clock LOW Time	400		ns
t_{SU}	Data Setup Time	100		ns
t_H	Data Hold Time	100		ns
t_{RI}(3)	Input Rise Time		2	µs
t_{FI}(3)	Input Fall Time		2	µs
t_{CS}	$\overline{CS}$ Deselect Time	500		ns
t_{WC}(4)	Write Cycle Time		10	ms

3844 PGM T12.2

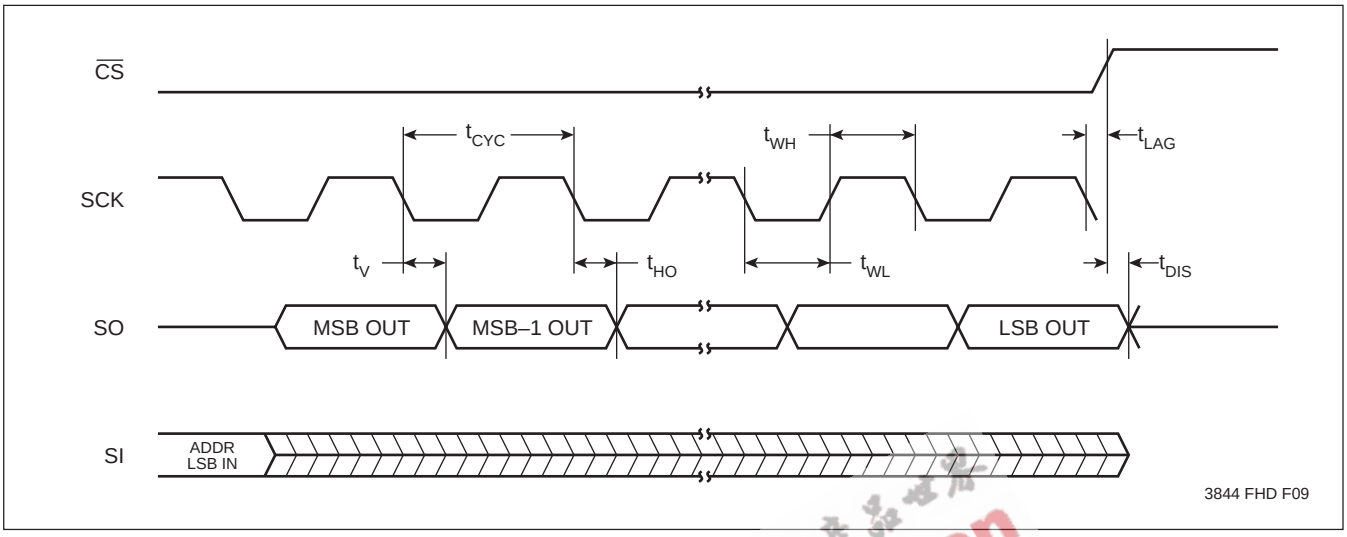
Data Output Timing

Symbol	Parameter	Min.	Max.	Units
f_{SCK}	Clock Frequency	0	1	MHz
t_{DIS}	Output Disable Time		500	ns
t_V	Output Valid from Clock LOW		400	ns
t_{HO}	Output Hold Time	0		ns
t_{RO}(3)	Output Rise Time		300	ns
t_{FO}(3)	Output Fall Time		300	ns

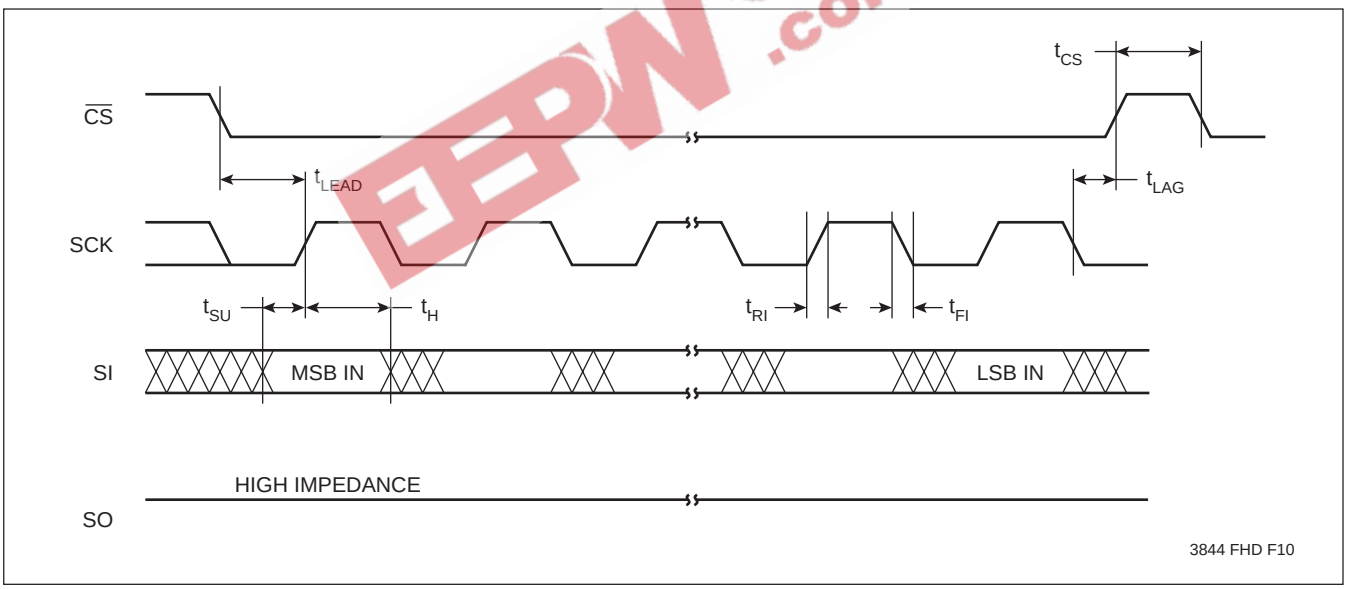
3844 PGM T13.1

Notes: (3) This parameter is periodically sampled and not 100% tested.
(4) t_{WC} is the time from the rising edge of $\overline{CS}$ after a valid write sequence has been sent to the end of the self-timed internal nonvolatile write cycle.

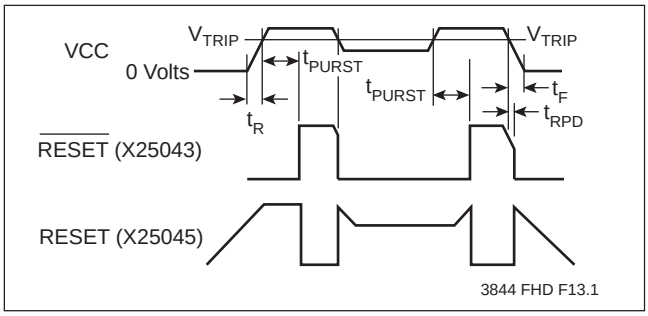
Serial Output Timing



Serial Input Timing



Power-Up and Power-Down Timing



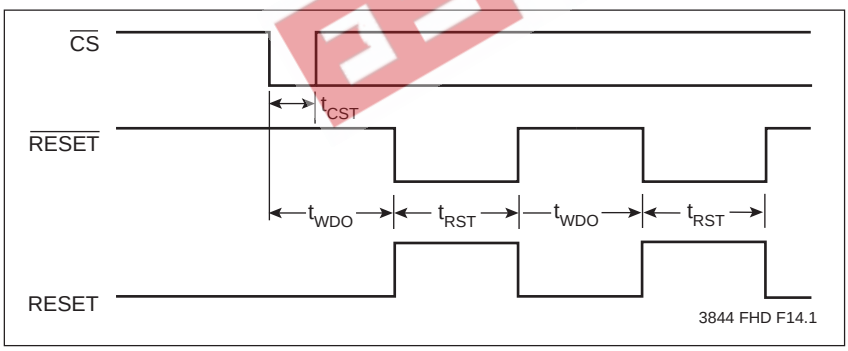
$\overline{\text{RESET}}$ Output Timing

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{TRIP}	Reset Trip Point Voltage, 5V Device Reset Trip Point Voltage, 2.7V Device	4.25 2.55		4.5 2.7	V V
t_{PURST}	Power-up Reset Timeout	100		400	ms
t_{RPD}(5)	V_{CC} Detect to Reset/Output			500	ns
t_F(5)	V_{CC} Fall Time	10			µs
t_R(5)	V_{CC} Rise Time	0			ns
V_{RVALID}	Reset Valid V_{CC}	1			V

3844 PGM T14.3

Notes: (5) This parameter is periodically sampled and not 100% tested.

$\overline{\text{CS}}$ vs $\overline{\text{RESET}}$/RESET Timing



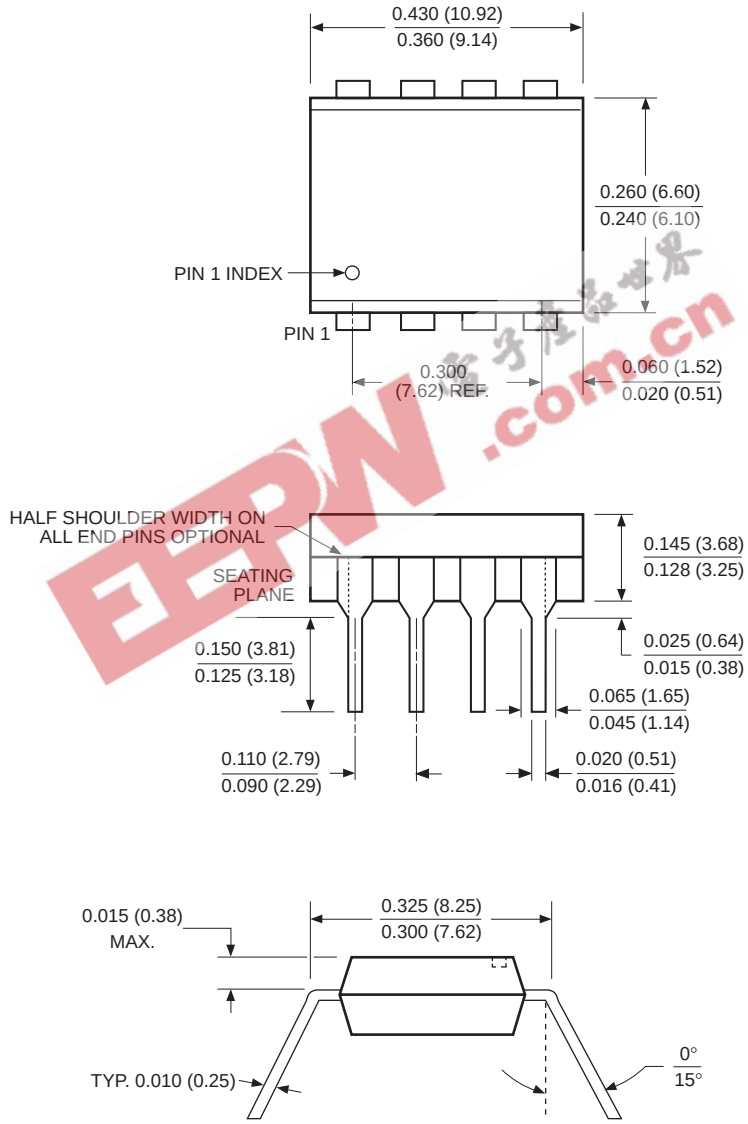
$\overline{\text{RESET}}$/RESET Output Timing

Symbol	Parameter	Min.	Typ.	Max.	Units
t_{WDO}	Watchdog Timeout Period, WD1=1,WD0=0 WD1=0,WD0=1 WD1=0,WD0=0	 100 450 1	 200 600 1.4	 300 800 2	 ms ms sec
t_{CST}	$\overline{\text{CS}}$ Pulse Width to Reset the Watchdog	400			ns
t_{RST}	Reset Timeout	100		400	ms

3844 PGM T15.3

PACKAGING INFORMATION

8-LEAD PLASTIC DUAL IN-LINE PACKAGE TYPE P

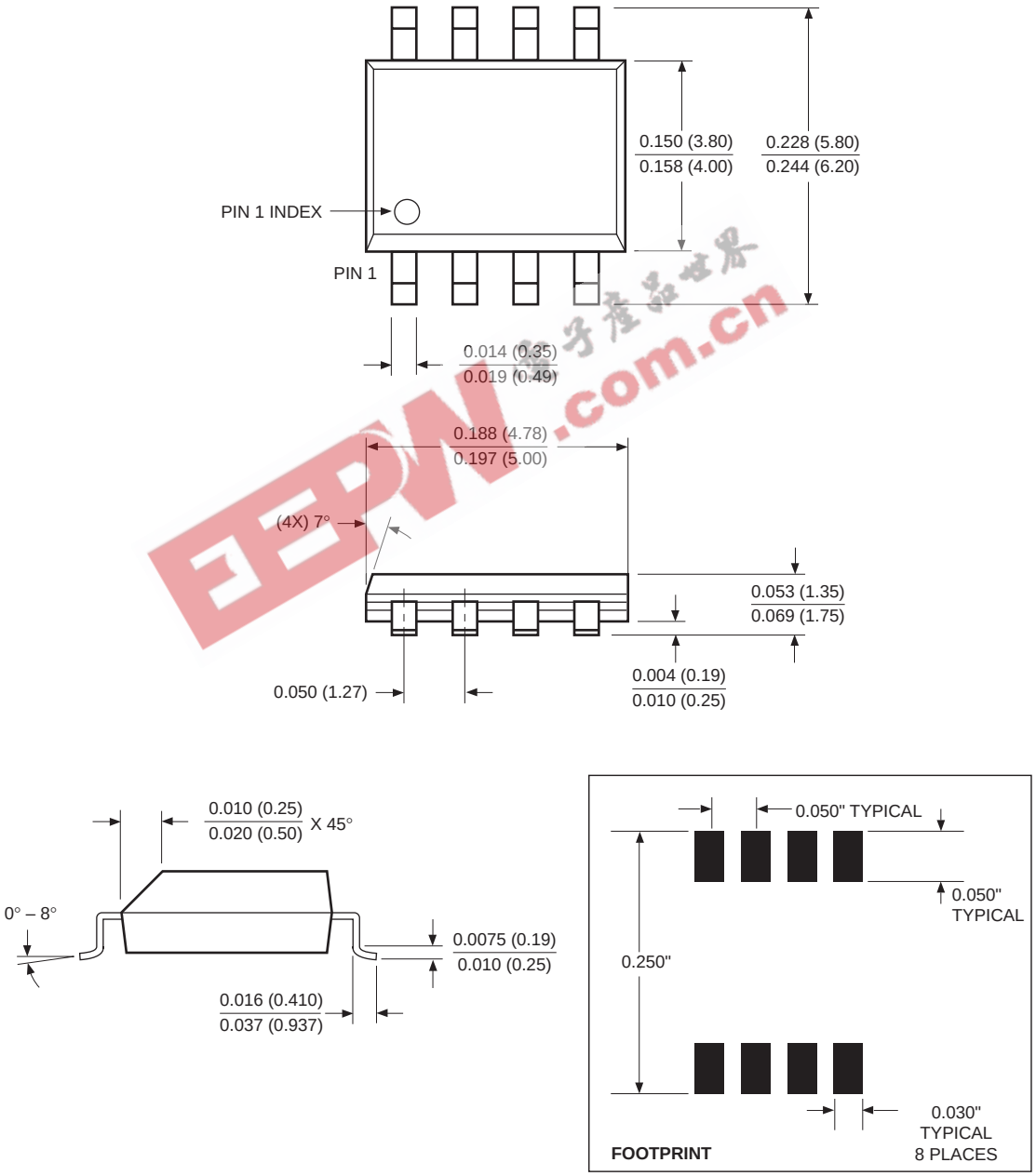


NOTE:

1. **ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)**
2. **PACKAGE DIMENSIONS EXCLUDE MOLDING FLASH**

PACKAGING INFORMATION

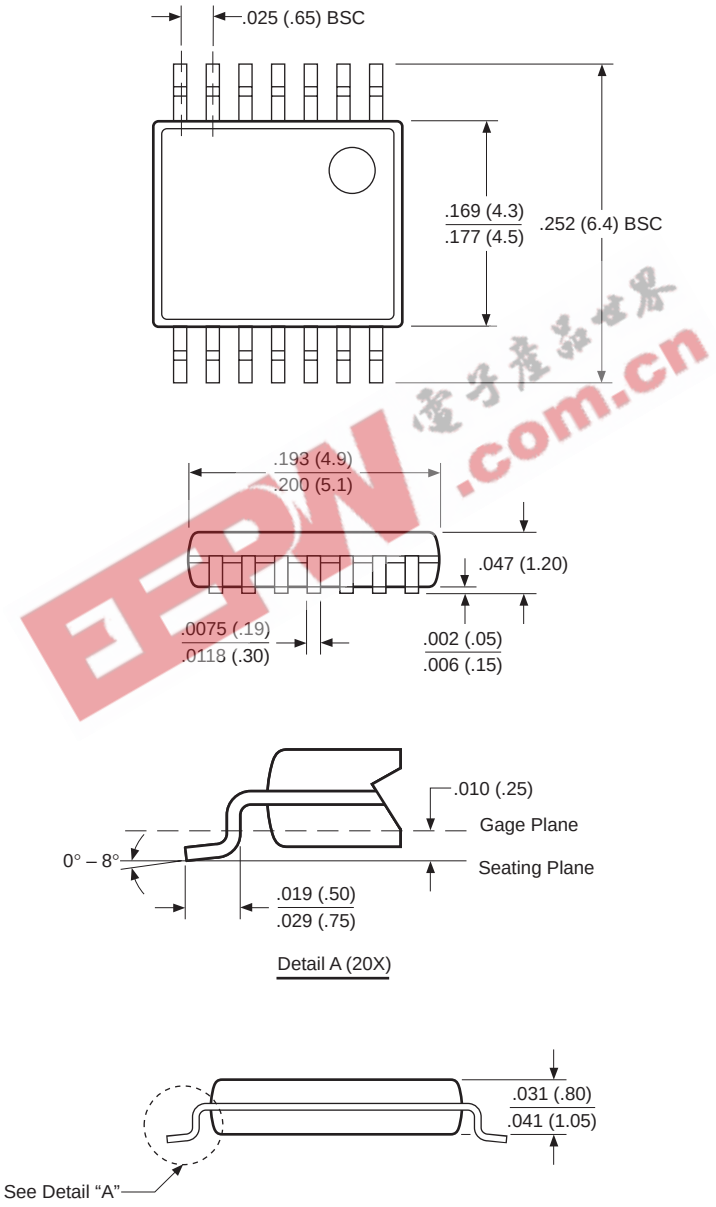
8-LEAD PLASTIC SMALL OUTLINE GULL WING PACKAGE TYPE S



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

PACKAGING INFORMATION

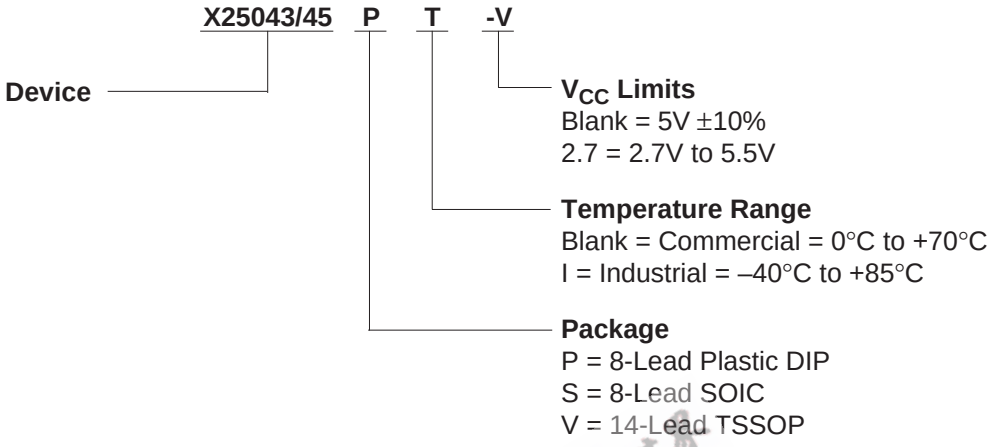
14-LEAD PLASTIC, TSSOP PACKAGE TYPE V



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

3926 FHD F32

ORDERING INFORMATION



Part Mark Convention