APPLICATION NOTES
A V A I L A B L E
AN4 • AN12 • AN22 • AN26 • AN32

128 Bit X24C00 16 x 8 Bit

Serial E²PROM

FEATURES

- 2.7V to 5.5V Power Supply
- 128 Bit Serial E²PROM
- Low Power CMOS
  - —Active Current Less Than 3mA
  - —Standby Current Less Than 50µA
- Internally Organized 16 x 8
- 2 Wire Serial Interface
  - —Bidirectional Data Transfer Protocol
- Byte Mode Write
- Self Timed Write Cycle
  - —Typical Write Cycle Time of 5ms
- Push/Pull Output
- High Reliability
  - —Endurance: 100,000 Cycles
  - —Data Retention: 100 Years
- Available Packages
  - —8-Lead MSOP
  - —8-Lead PDIP
  - —8-Lead SOIC

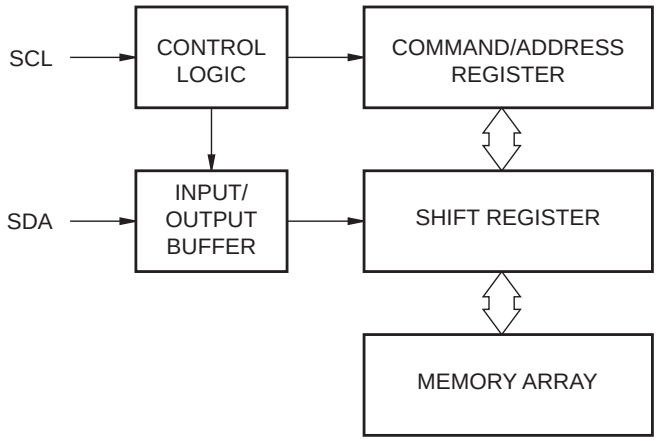
DESCRIPTION

The X24C00 is a CMOS 128 bit serial E²PROM, internally organized as 16 x 8. The X24C00 features a serial interface and software protocol allowing operation on a simple two wire bus.

Xicor E²PROMs are designed and tested for applications requiring extended endurance. Inherent data retention is greater than 100 years.

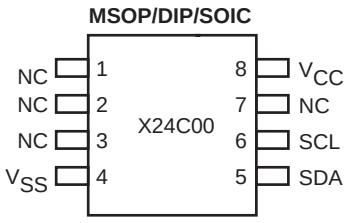
The X24C00 is fabricated with Xicor's Advanced CMOS Floating Gate technology.

FUNCTIONAL DIAGRAM



3836 FHD F01

PIN CONFIGURATION



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PIN DESCRIPTIONS

Serial Clock (SCL)

The SCL input is used to clock all data into and out of the device.

Serial Data (SDA)

SDA is a bidirectional pin used to transfer data into and out of the device. It is a push/pull output and does not require the use of a pull-up resistor.

PIN NAMES

Symbol	Description
NC	No Connect
V_{SS}	Ground
V_{CC}	Supply Voltage
SDA	Serial Data
SCL	Serial Clock

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DEVICE OPERATION

The X24C00 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master will always initiate data transfers and provide the clock for both transmit and receive operations. Therefore, the X24C00 will be considered a slave in all applications.

Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions. Refer to Figures 1 and 2.

Start Condition

All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The X24C00 continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

A start may be issued to terminate the input of a control word or the input of data to be written. This will reset the device and leave it ready to begin a new read or write command. Because of the push/pull output, a start cannot be generated while the part is outputting data. Starts are also inhibited while a write is in progress.

Stop Condition

The stop condition is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is used to reset the device during a command or data input sequence and will leave the device in the standby mode. As with starts, stops are inhibited when outputting data and while a write is in progress.

Write Operation

The byte write operation is initiated with a start condition. The start condition is followed by an eight bit control byte which consists of a two bit write command (0,1), four address bits, and two “don’t care” bits (Figure 3).

Figure 1. Data Validity

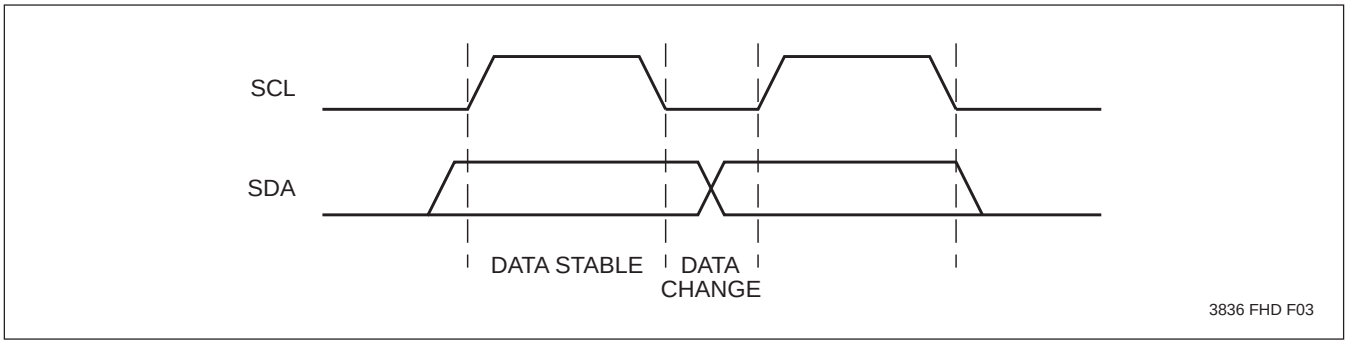


Figure 2. Definition of Start and Stop Conditions

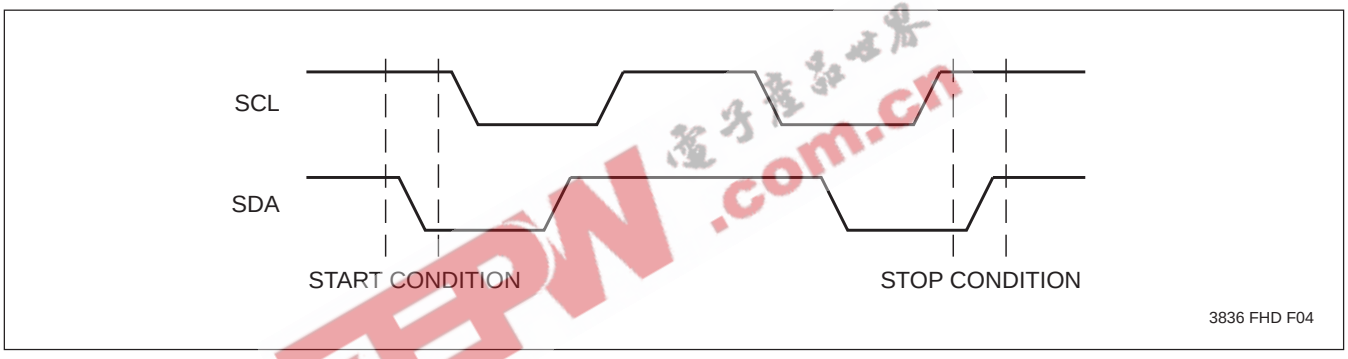
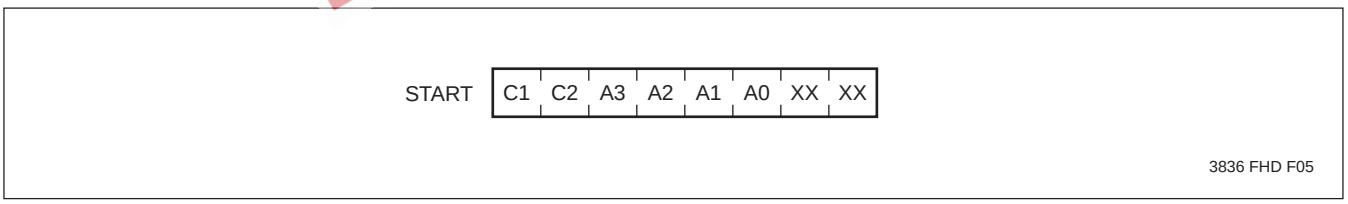


Figure 3. Control Byte



After receipt of the control byte, the X24C00 will enter the write mode and await the data to be written. This data is shifted into the device on the next eight SCL clocks. Once eight clocks have been received, the data in the shift register will be written into the memory array. While the write is in progress the X24C00 will not respond to any inputs. At any time prior to clocking in the last data bit, a stop command or a new start command will terminate the operation. If a start command is given, the X24C00 will reset all counters and will prepare to clock in the next control byte. If a stop command is given, the X24C00 will reset all counters and await the next start command.

At the end of the write the X24C00 will automatically reset all counters and enter the standby mode. (Figure 4).

Read Operation

The byte read operation is initiated with a start condition. The start condition is followed by an eight-bit control byte which consists of a two-bit read command (1,0), four address bits, and two “don’t care” bits. After receipt of the control byte the X24C00 will enter the read mode and transfer data into the shift register from the array. This data is shifted out of the device on the next eight SCL clocks. At the end of the read, all counters are reset and the X24C00 will enter the standby mode. As with a write, the read operation can be interrupted by a start or stop condition while the command or address is being clocked in. While clocking data out, starts or stops cannot be generated.

During the second don’t care clock cycle, starts and stops are ignored. The master must free the bus prior to the end of this clock cycle to allow the X24C00 to begin outputting data (Figures 5 and 6).

Figure 4. Write Sequence

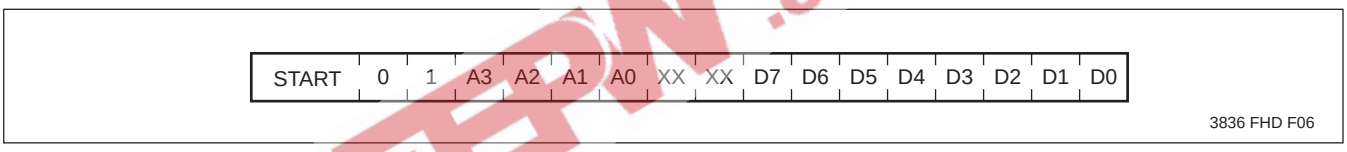


Figure 5. Read Sequence

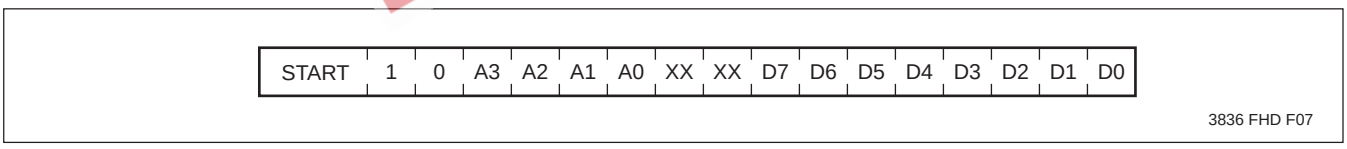
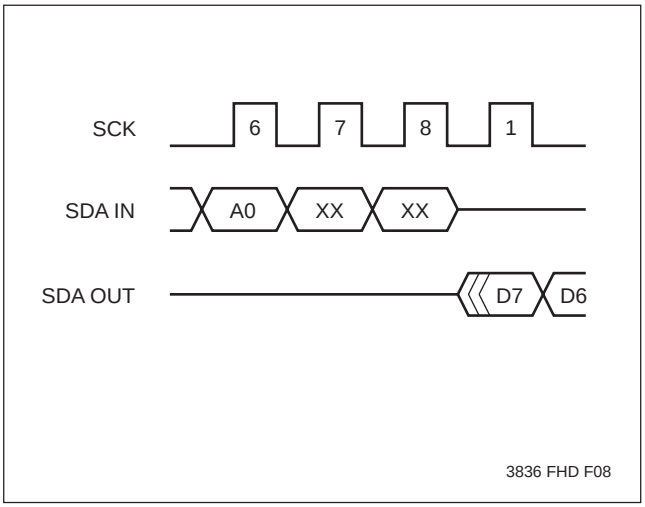


Figure 6. Read Cycle Timing



SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don’t Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

ABSOLUTE MAXIMUM RATINGS*

Temperature under Bias
X24C00 ..... –65°C to +135°C
Storage Temperature ..... –65°C to +150°C
Voltage on any Pin with
Respect to V_{SS} ..... –1V to +7V
D.C. Output Current 5mA
Lead Temperature
(Soldering, 10 seconds) ..... 300°C

***COMMENT**

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	+70°C
Industrial	–40°C	+85°C
Military	–55°C	+125°C

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Supply Voltage	Limits
X24C00	5V ±10%
X24C00-3	3V to 5.5V
X24C00-2.7	2.7V to 5.5V

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D.C. OPERATING CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I_{CC1}	V_{CC} Supply Current Read		1	mA	SCL = VCC x 0.1/VCC x 0.9
I_{CC2}	V_{CC} Supply Current Write		3		Levels @ 1MHz, SDA = Open
I_{SB1}	V_{CC} Standby Current		100	µA	SCL = SDA = V_{CC} V_{CC} = 5V ±10%
I_{SB2}	V_{CC} Standby Current		50	µA	SCL = SDA = V_{CC} V_{CC} = 2.7V
I_{LI}	Input Leakage Current		10	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output Leakage Current		10	µA	V_{OUT} = V_{SS} to V_{CC}
V_{IL}(1)	Input LOW Voltage	–1	V_{CC} x 0.3	V	
V_{IH}(1)	Input HIGH Voltage	V_{CC} x 0.7	V_{CC} + 0.5	V	
V_{OL}	Output LOW Voltage		0.4	V	I_{OL} = 2.1mA
V_{OH}	Output HIGH Voltage	V_{CC} – 0.8		V	I_{OH} = 1mA

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CAPACITANCE T_A = +25°C, f = 1MHz, V_{CC} = 5V

Symbol	Parameter	Max.	Units	Test Conditions
$C_{I/O}$(2)	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}(2)	Input Capacitance (SCL)	6	pF	V_{IN} = 0V

3836 PGM T05.1

Notes: (1) V_{IL} min. and V_{IH} max. are for reference only and are not tested.
(2) This parameter is periodically sampled and not 100% tested.

POWER-UP TIMING

Symbol	Parameter	Max.	Units
t_{PUR}(3)	Power-up to Read Operation	2	ms
t_{PUW}(3)	Power-up to Write Operation	5	ms

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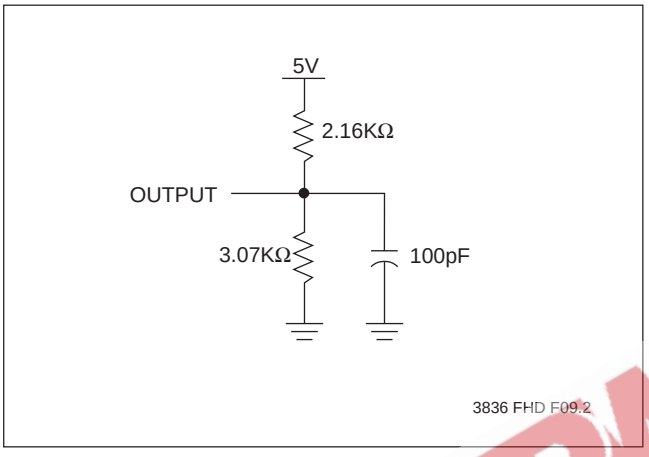
EQUIVALENT A.C. LOAD CIRCUIT



A.C. CONDITIONS OF TEST

Input Pulse Levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input Rise and Fall Times	10ns
Input and Output Timing Levels	V_{CC} x 0.5

3836 PGM T06.1

A.C. CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified.)

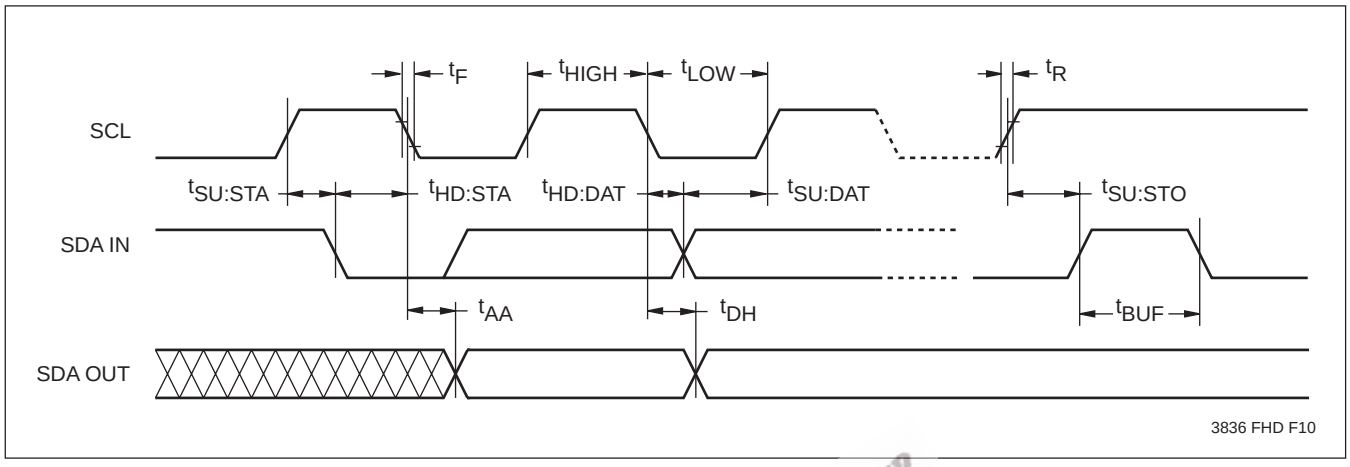
Read & Write Cycle Limits

Symbol	Parameter	Min.	Max.	Units
f_{SCL}	SCL Clock Frequency	0	1	MHz
t_{AA}	SCL LOW to SDA Data Out Valid		350	ns
t_{BUF}	Time the Bus Must Be Free Before a New Transmission Can Start	500		ns
$t_{HD:STA}$	Start Condition Hold Time	250		ns
t_{LOW}	Clock LOW Period	500		ns
t_{HIGH}	Clock HIGH Period	500		ns
$t_{SU:STA}$	Start Condition Setup Time	250		ns
$t_{HD:DAT}$	Data In Hold Time	0		µs
$t_{SU:DAT}$	Data in Setup Time	250		ns
t_R	SDA and SCL Rise Time		1	µs
t_F	SDA and SCL Fall Time		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	250		ns
t_{DH}	Data Out Hold Time	50		ns

3836 PGM T07.1

Note: (3) t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated. These parameters are periodically sampled and not 100% tested.

Bus Timing



WRITE CYCLE LIMITS

Symbol	Parameter	Min.	Max.	Units
t_{WR}(4)	Write Cycle Time		5	ms

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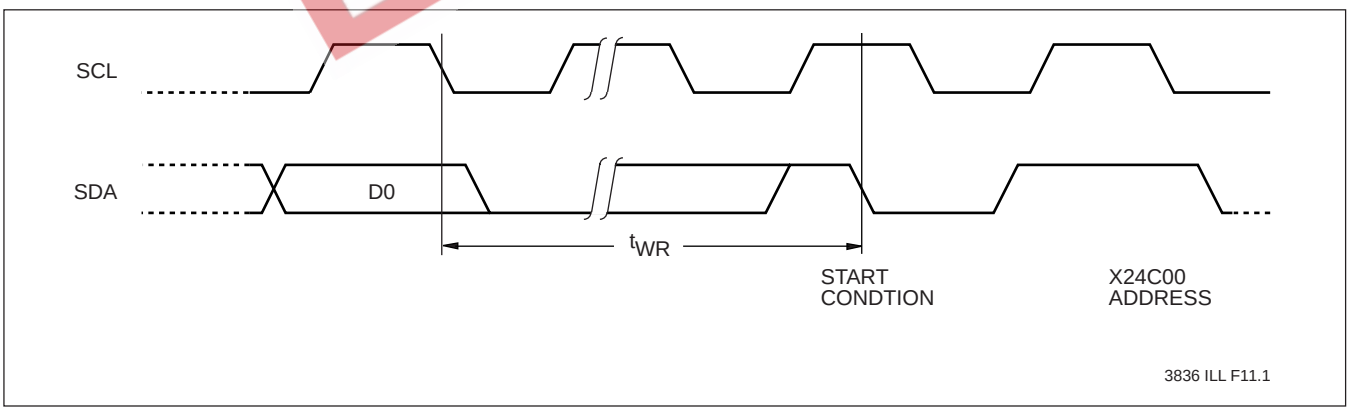
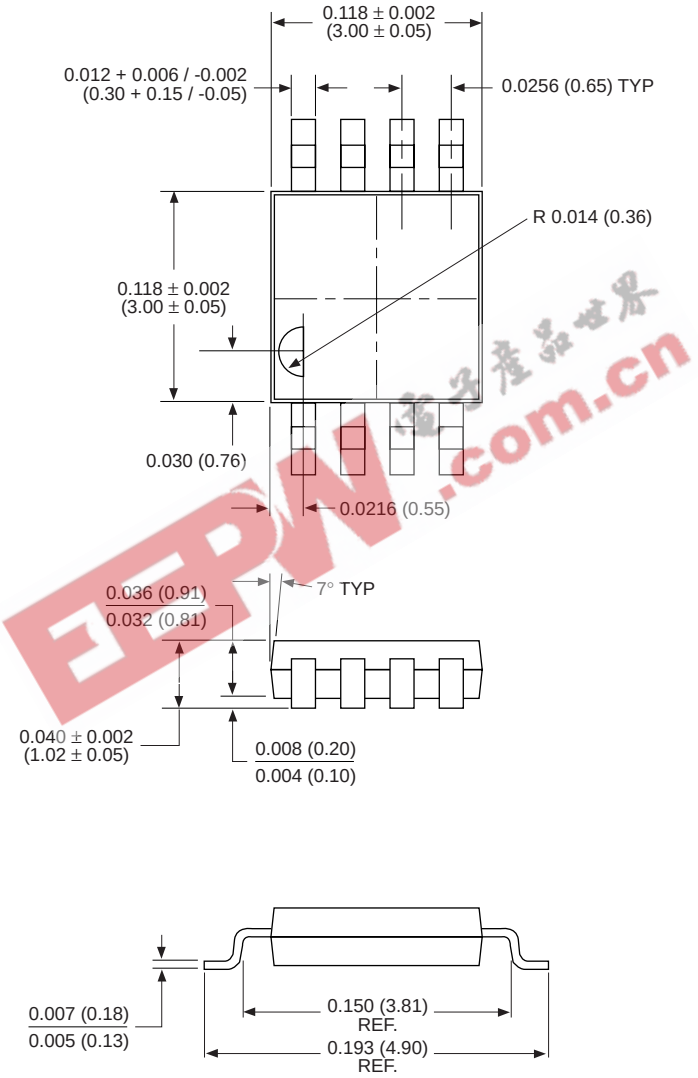
Write Cycle Timing



Note: (4) The write cycle time is the time from the initiation of a write sequence to the end of the internal erase/program cycle. During the write cycle, the X24C00 bus interface circuits are disabled, SDA is high impedance, and the device does not respond to start conditions.

PACKAGING INFORMATION

8-LEAD MINIATURE SMALL OUTLINE GULL WING PACKAGE TYPE M



NOTE:

1. ALL DIMENSIONS IN INCHES AND (MILLIMETERS)

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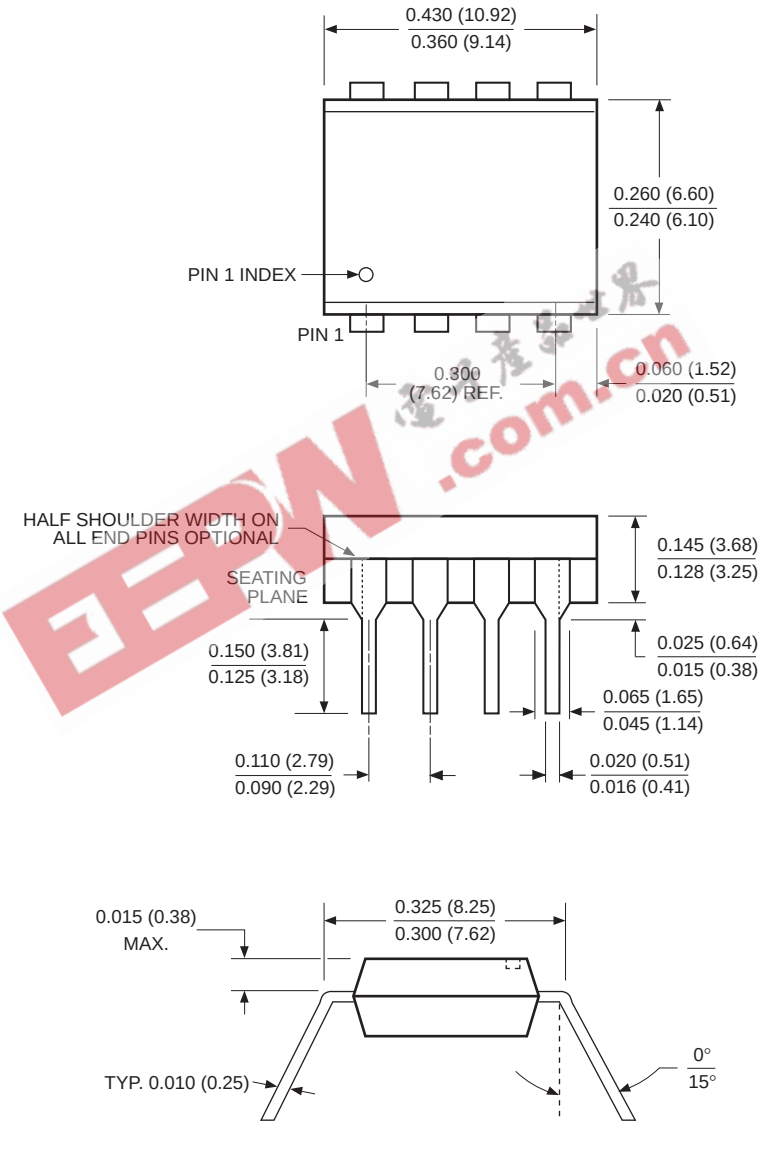
PACKAGING INFORMATION

8-LEAD PLASTIC DUAL IN-LINE PACKAGE TYPE P



NOTE:

1. **ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)**
2. **PACKAGE DIMENSIONS EXCLUDE MOLDING FLASH**

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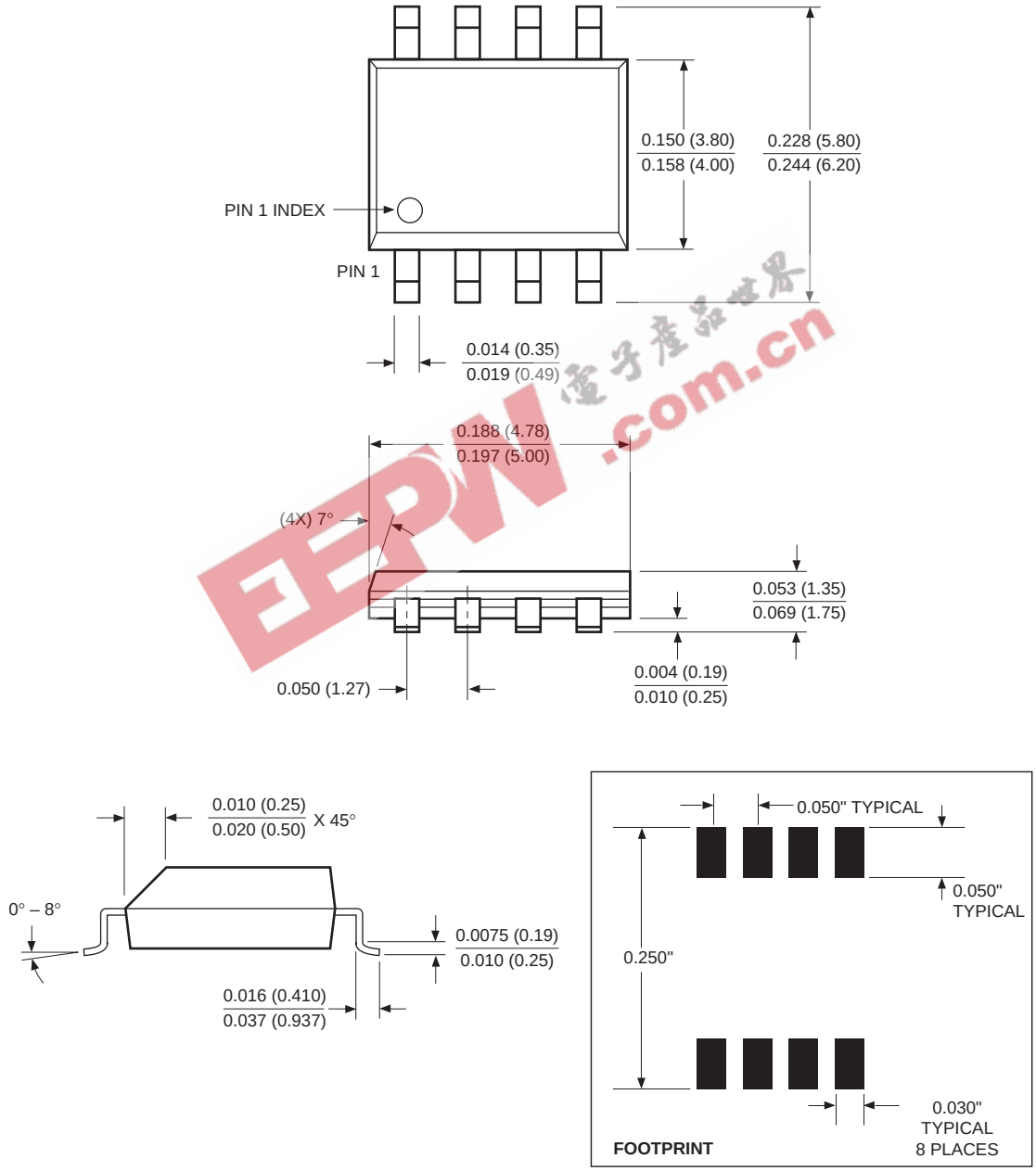
PACKAGING INFORMATION

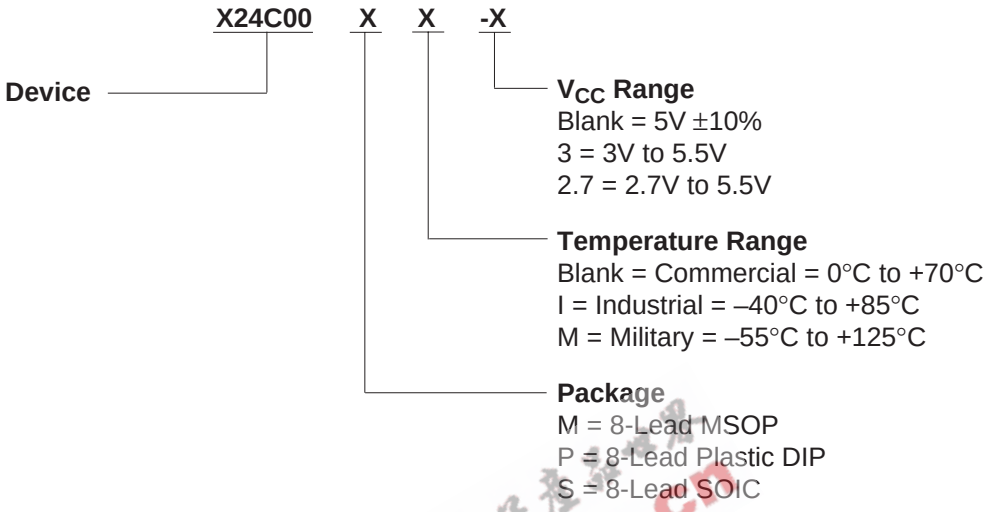
8-LEAD PLASTIC SMALL OUTLINE GULL WING PACKAGE TYPE S



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

3926 FHD F22.1

ORDERING INFORMATION



Part Mark Convention