4K X25F047 512 x 8 Bit

SPI SerialFlash with Block Lock™ Protection

FEATURES

- **1MHz Clock Rate**
- **SPI Modes (0,0 & 1,1)**
- **512 x 8 Bits**
  - **—16 Byte Small Sector Program Mode**
- **Low Power CMOS**
  - **—<1μA Standby Current**
  - **—<3mA Active Current during Program**
  - **—<400μA Active Current during Read**
- **1.8V to 3.6V or 5V "Univolt" Read and Program Power Supply Versions**
- **Block Lock Protection**
  - **—Block Lock Protect 0, any 1/4, 1st 1/2, First or Last Sector of SerialFlash Array**
- **Built-in Inadvertent Program Protection**
  - **—Power-Up/Power-Down Protection Circuitry**
  - **—Program Enable Latch**
  - **—Program Protect Pin**
- **Self-Timed Program Cycle**
  - **—5ms Program Cycle Time (Typical)**
- **High Reliability**
  - **—Endurance: 100,000 Cycles/Byte**
  - **—Data Retention: 100 Years**
  - **—ESD: 2000V on all pins**
- **8-Lead SOIC Package**
- **8-Lead MSOP Package**
- **8-Lead TSSOP Package**
- **8-Pin Mini-DIP Package**

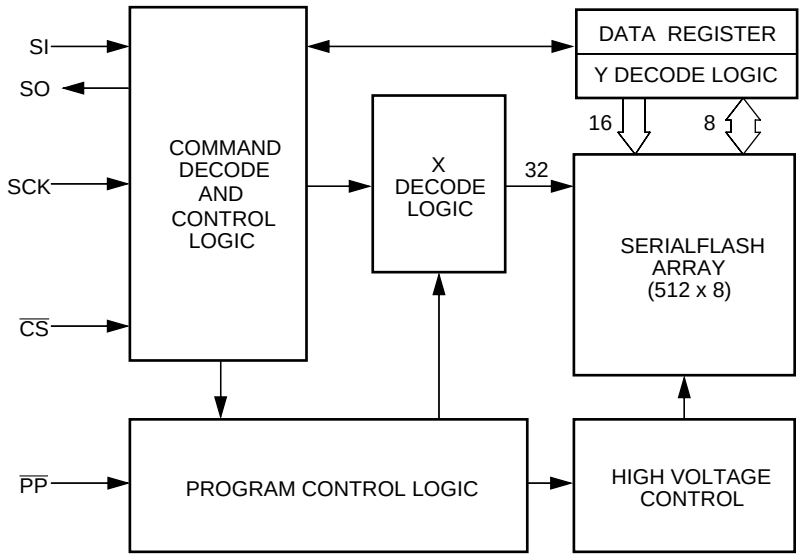
DESCRIPTION

The X25F047 is a CMOS 4K-bit SerialFlash, internally organized as 512 x 8. The X25F047 features a Serial Peripheral Interface (SPI) and software protocol allowing operation on a simple four-wire bus. The bus signals are a clock input (SCK) plus separate data in (SI) and data out (SO) lines. Access to the device is controlled through a chip select ($\overline{CS}$) input, allowing any number of devices to share the same bus.

There are eight options for programmable, nonvolatile, Block Lock Protection available to the end user. These options are implemented via special instructions programmed to the part. The X25F047 also features a $\overline{PP}$ pin that can be used for hardwire protection of the part, disabling all programming attempts, as well as a Program Enable Latch that must be set before a program operation can be initiated.

The X25F047 utilizes Xicor's proprietary Direct Write™ cell, providing a minimum endurance of 100,000 cycles per sector and a minimum data retention of 100 years.

FUNCTIONAL DIAGRAM



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PIN DESCRIPTIONS

Serial Output (SO)

SO is a push/pull serial data output pin. During a read cycle, data is shifted out on this pin. Data is clocked out by the falling edge of the serial clock.

Serial Input (SI)

SI is a serial data input pin. All opcodes, byte addresses, and data to be programmed to the memory are input on this pin. Data is latched by the rising edge of the serial clock.

Serial Clock (SCK)

The Serial Clock controls the serial bus timing for data input and output. Opcodes, addresses, or data present on the SI pin are latched on the rising edge of the clock input, while data on the SO pin change after the falling edge of the clock input.

Chip Select ($\overline{CS}$)

When $\overline{CS}$ is HIGH, the X25F047 is deselected and the SO output pin is at high impedance and unless a nonvolatile write cycle is underway, the X25F047 will be in the standby power mode. $\overline{CS}$ LOW enables the X25F047, placing it in the active power mode. It should be noted that after power-up, a HIGH to LOW transition on $\overline{CS}$ is required prior to the start of any operation.

Program Protect ($\overline{PP}$)

When $\overline{PP}$ is LOW, nonvolatile writes to the X25F047 are disabled, but the part otherwise functions normally. When $\overline{PP}$ is held HIGH, all functions, including nonvolatile writes, operate normally. $\overline{PP}$ going LOW while $\overline{CS}$ is still LOW will interrupt a programming cycle to the X25F047. If the nonvolatile write cycle has already been initiated, $\overline{PP}$ going low will have no affect on this cycle.

PIN NAMES

Symbol	Description
$\overline{CS}$	Chip Select Input
SO	Serial Output
SI	Serial Input
SCK	Serial Clock Input
$\overline{PP}$	Program Protect Input
V_{SS}	Ground
V_{CC}	Supply Voltage
NC	No Connect

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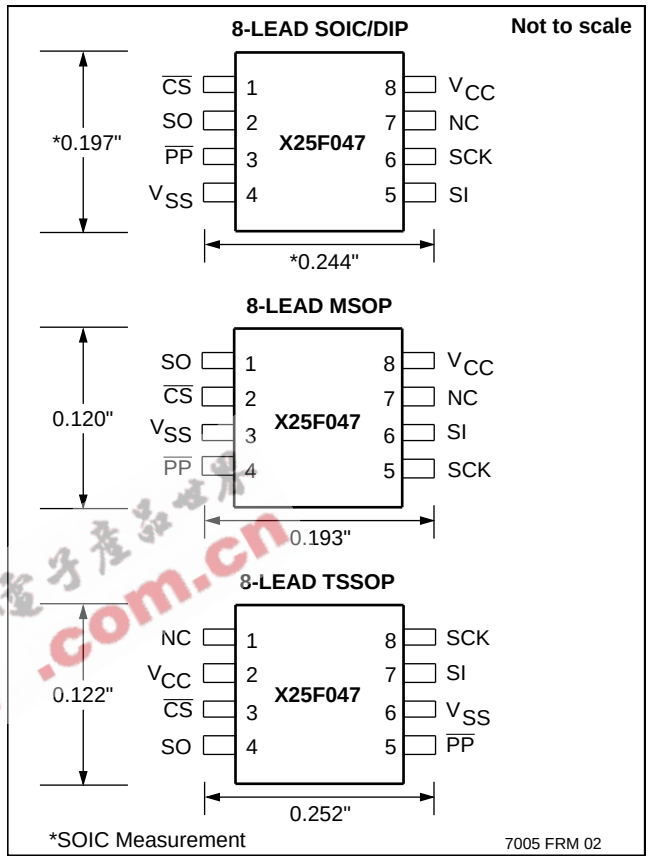
PIN CONFIGURATION



PRINCIPLES OF OPERATION

The X25F047 is a 512 x 8 SerialFlash designed to interface directly with the synchronous Serial Peripheral Interface (SPI) of many popular microcontroller families.

The X25F047 contains an 8-bit instruction register. It is accessed via the SI input, with data being clocked in on the rising edge of SCK. $\overline{CS}$ must be LOW and the $\overline{PP}$ input must be HIGH during the entire operation. Table 1 contains a list of the instructions and their opcodes. All instructions, addresses and data are transferred MSB first.

Data input is sampled on the first rising edge of SCK after $\overline{CS}$ goes LOW. SCK is static, allowing the user to stop the clock and then start it again to resume operations where left off.

Program Enable Latch

The X25F047 contains a “Program Enable” latch. This latch must be SET before a program operation is initiated. The PREN instruction will set the latch and the PRDI instruction will reset the latch (Figure 4). This latch is automatically reset upon a power-up condition and after the completion of a sector program cycle.

Block Lock Protection

There are eight Block Lock Protection options. The predefined blocks and associated address ranges are protected by programming the appropriate two byte Program Status instruction to the device (Table 1 and Figure 6). Once a Block Lock protect instruction has been completed, that Block Lock Protection setup is held in a nonvolatile Status Register (Figure 1) until the next Program Status instruction is issued. The sections of the memory array that are Block Lock protected can be read but not programmed until Block Lock Protection is removed or changed.

Figure 1. Status Register/Block Lock Protection Byte

7	6	5	4	3	2	1	0
0	0	0	0	0	BL2	BL1	BL0

Note: Bits [7:3] specified to be “0’s”

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Read Sequence

When reading from the SerialFlash memory array, $\overline{CS}$ is first pulled LOW to select the device. The 8-bit READ instruction is transmitted to the X25F047, followed by the 16-bit address, of which the last 9 bits are used (bits [15:9] specified to be "0’s"). After the READ opcode and address are sent, the data stored in the memory at the selected address is shifted out on the SO line. The data stored in memory at the next address can be read sequentially by continuing to provide clock pulses. The address is automatically incremented to the next higher address after each byte of data is shifted out. When the highest address is reached (01FFh), the address counter rolls over to address 0000h, allowing the read cycle to be continued indefinitely. The read operation is terminated by taking $\overline{CS}$ HIGH (Figure 2).

Sector Program Sequence

Prior to any attempt to program data into the X25F047, the “Program Enable” latch must first be set by issuing the PREN instruction (Table 1 and Figure 4). $\overline{CS}$ is first taken LOW. Then the PREN instruction is clocked into the X25F047. After all eight bits of the instruction are transmitted, $\overline{CS}$ must then be taken HIGH. If the user continues the program operation without taking $\overline{CS}$ HIGH after issuing the PREN instruction, the program operation will be ignored.

To program data to the SerialFlash memory array, the user then issues the PROGRAM instruction, followed by the 16 bit address of the first location in the sector and then the 16 bytes of data to be programmed. Only the last 9 bits of the address are used and bits [15:9] are specified to be "0’s". The entire write operation takes 152 clocks. $\overline{CS}$ must go LOW and remain LOW for the duration of the operation. The host must program 16 bytes in each write with the restriction that these bytes reside on one sector. If the address counter reaches the end of the sector and the clock continues, or if fewer than 16 bytes are clocked in, the contents of the sector cannot be guaranteed.

For a sector program operation to be completed, $\overline{CS}$ can only be brought HIGH after bit 0 of the last data byte to be programmed is clocked in. If it is brought HIGH at any other time, the program operation will not be completed. (Figure 5)

Read Status Operation

If there is not a nonvolatile write in progress, the Read Status instruction returns the Block Lock Protection byte from the Status Register which contains the Block Lock Protection bits BL2-BL0 (Figure 1). The Block Lock Protection bits define the Block Lock Protection condition (Figure 1 and Table1). The other bits are reserved and will return "0’s" when read (Figure 3).

If a nonvolatile write is in progress, the Read Status instruction returns the status of the internal write operation on SO. When the nonvolatile write cycle is completed, the status register data is again read out.

During a nonvolatile write in progress, the SO pin will be set HIGH. At the end of the nonvolatile write cycle, SO is set to output the current bit from the status register. Clocking SCK is valid during a nonvolatile write in progress, but is not necessary. If the SCK line is clocked, the pointer to the status register is also clocked, even though the SO pin shows the status of the nonvolatile write operation (Figure 3). When the pointer reaches the end of the eight bit status register, it “rolls over” to the first bit of the register.

Program Status Operation

Prior to any attempt to perform a Program Status Operation, the PREN instruction must first be issued. This instruction sets the “Program Enable” latch and allows the part to respond to a Program Status sequence (Figure 6). The Program Status instruction follows and consists of one command byte followed by one Block Lock Protection byte (Figure 1). This byte contains the Block Lock Protection bits BL2-BL0. The rest of the bits [7:3] are unused and must be programmed as “0’s”. Bringing $\overline{CS}$ HIGH after the two byte Program Status instruction initiates a nonvolatile write to the Status Register. Programming more than one byte to the Status Register will overwrite the previously programmed Block Lock Protection byte (Table 1).

Data Protection

The following circuitry has been included to prevent inadvertant programming of data:

- The “Program Enable” latch is reset upon power-up.
- A PREN instruction must be issued to set the “Program Enable” latch.
- $\overline{CS}$ must come HIGH at the proper clock count in order to start a program cycle.

Operational Notes

The X25F047 powers up in the following state:

- The device is in the low power, standby state.
- A HIGH to LOW transition on $\overline{CS}$ is required to enter an active state and receive an instruction.
- SO pin is at high impedance.
- The “Program Enable” latch is reset.

Table 1. Instruction Set and Block Lock Protection Byte Definition

Instruction Format*	Instruction Name and Operation
0000 0110	PREN: Set the Program Enable Latch (Program Enable Operation)
0000 0100	PRDI: Reset the Program Enable Latch (Program Disable Operation)
0000 0001	**PROGRAM STATUS Instruction - followed by:** **Block Lock Protection Byte: (Figure 1)** 0000 0000 --->NO PROTECT: ---------->None of the Array 0000 0001 --->PROTECT Q1: --- 0000h - 007Fh ---------->Lower Quadrant (Q1) 0000 0010 --->PROTECT Q2: --- 0080h - 00FFh---------->Q2 0000 0011 --->PROTECT Q3: --- 0100h - 017Fh---------->Q3 0000 0100 --->PROTECT Q4: --- 0180h - 01FFh---------->Upper Quadrant (Q4) 0000 0101 --->PROTECT H1: --- 0000h - 00FFh---------->Lower Half of the Array (H1) 0000 0110 --->PROTECT S0: --- 0000h - 000Fh---------->Lower Sector (S0) 0000 0111 --->PROTECT Sn: --- 01F0h - 01FFh---------->Upper Sector (Sn)
0000 0101	READ STATUS: Reads Block Lock Protection & nonvolatile write in progress status on SO Pin
0000 0010	PROGRAM: Program operation followed by address and data
0000 0011	READ: Read operation followed by address

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*Instructions are shown with MSB in leftmost position. Instructions are transferred MSB first.

Figure 2. Read Operation Sequence

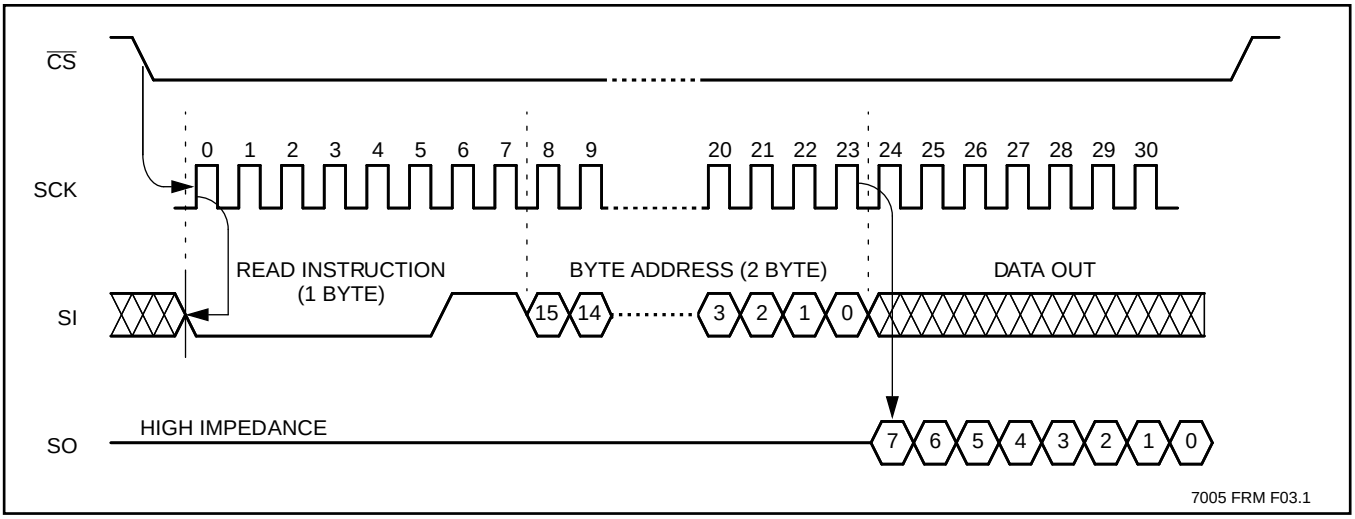


Figure 3. Read Status Operation Sequence

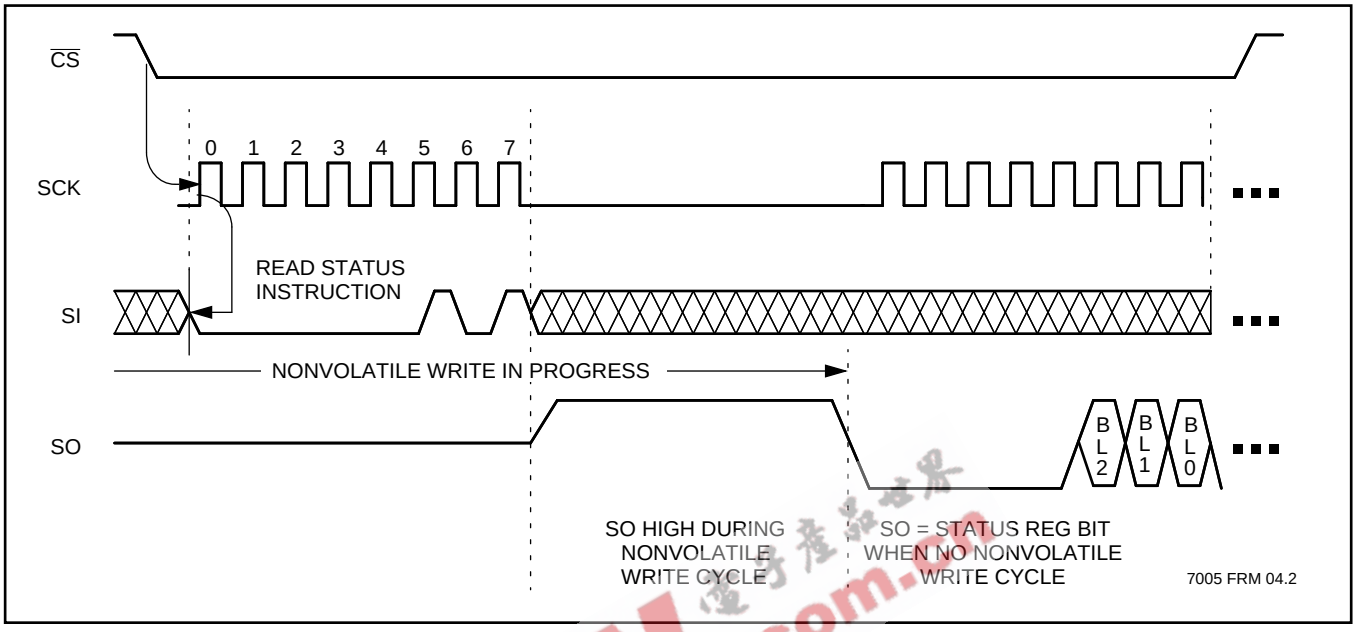


Figure 4. Program Enable/Program Disable Sequence

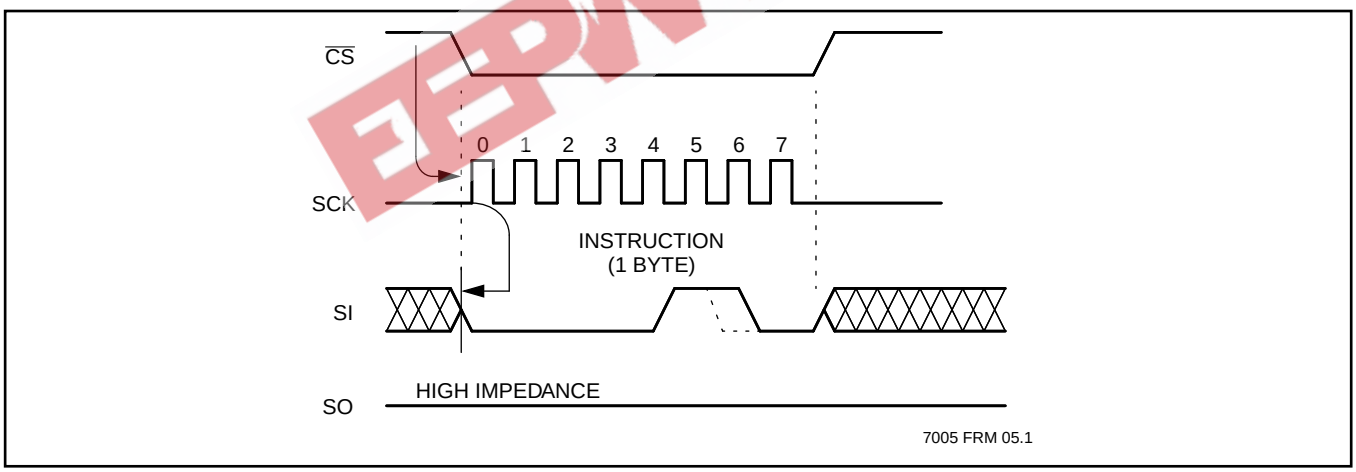


Figure 5. Sector Program Operation Sequence

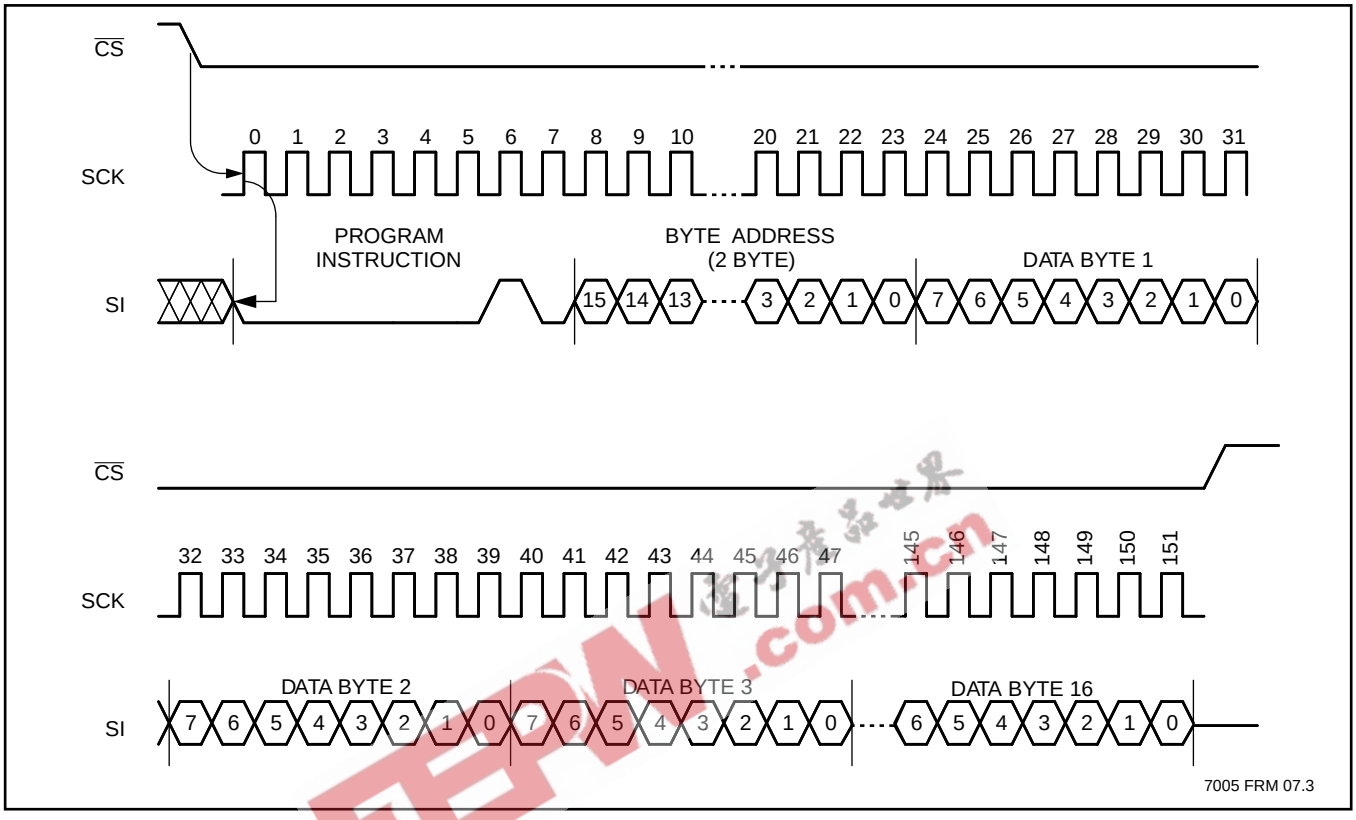
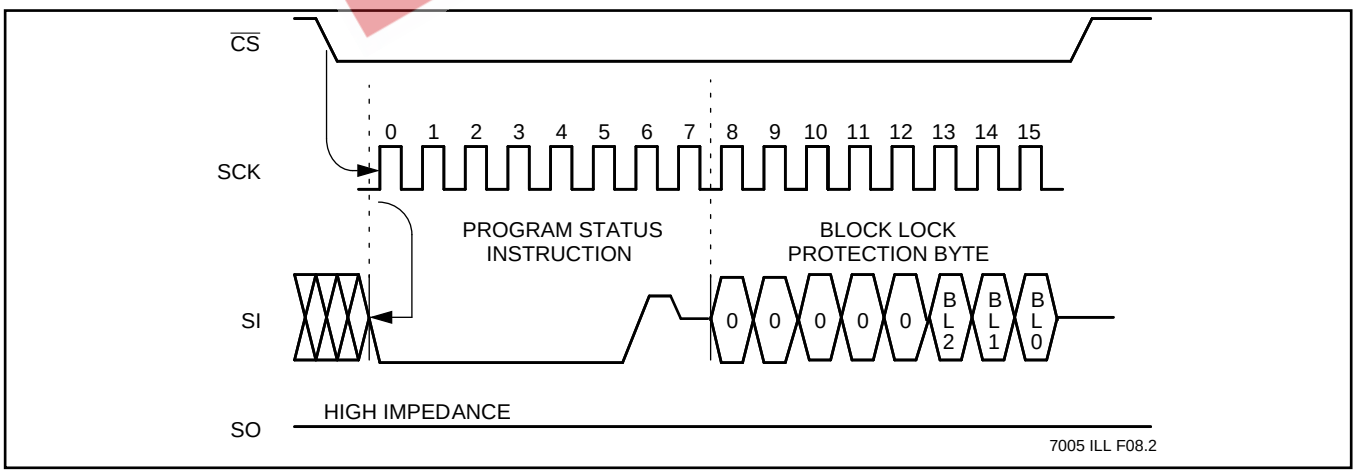


Figure 6. Program Status Operation Sequence



ABSOLUTE MAXIMUM RATINGS*

Temperature under Bias .....–65°C to +135°C
Storage Temperature.....–65°C to +150°C
Voltage on any Pin with
Respect to V_{SS}.....–1V to +7V
D.C. Output Current 5mA
Lead Temperature
(Soldering, 10 seconds) .....300°C

*COMMENT

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	+70°C
Industrial	–40°C	+85°C

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Supply Voltage	Limits
X25F047	1.8V to 3.6V
X25F047-5	4.5V to 5.5V

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D.C. OPERATING CHARACTERISTICS (Over the recommended operating conditions, unless otherwise specified.)

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I_{CC1}	V_{CC} Read Current (Active)		1	mA	SCK = V_{CC} x 0.1/V_{CC} x 0.9 @ 1MHz, SO = Open, $\overline{CS}$ = V_{SS}
I_{CC2}	V_{CC} Write Current (Active)		3	mA	SCK = V_{CC} x 0.1/V_{CC} x 0.9 @ 1MHz, SO = Open, $\overline{CS}$ = V_{SS}
I_{SB}	V_{CC} Supply Current (Standby)		1	µA	$\overline{CS}$ = V_{CC} - 0.1, V_{IN} = V_{SS} or V_{CC}
I_{LI}	Input Leakage Current		10	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output Leakage Current		10	µA	V_{OUT} = V_{SS} to V_{CC}
V_{IL}(1)	Input LOW Voltage	–0.5	V_{CC} x 0.3	V	
V_{IH}(1)	Input HIGH Voltage	V_{CC} x 0.7	V_{CC} + 0.5	V	
V_{OL1}	Output LOW Voltage		0.4	V	V_{CC} = 5.5V, I_{OL} = 2.1mA
V_{OH1}	Output HIGH Voltage	V_{CC} – 0.8		V	V_{CC} = 5.5V, I_{OH} = –1.0mA
V_{OL2}	Output LOW Voltage		0.4	V	V_{CC} = 3.6V, I_{OL} = 1.0mA
V_{OH2}	Output HIGH Voltage	V_{CC} – 0.4		V	V_{CC} = 3.6V, I_{OH} = –0.4mA
V_{OL3}	Output LOW Voltage		0.4	V	V_{CC} = 1.8V, I_{OL} = 0.5mA
V_{OH3}	Output HIGH Voltage	V_{CC} – 0.2		V	V_{CC} = 1.8V, I_{OH} = –0.25mA

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POWER-UP TIMING

Symbol	Parameter	Min.	Max.	Units
t_{PUR}(3)	Power-up to Read Operation		1	ms
t_{PUW}(3)	Power-up to Write Operation		5	ms

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CAPACITANCE T_A = +25°C, f = 1MHz, V_{CC} =5V.

Symbol	Parameter	Max.	Units	Conditions
C_{OUT}(2)	Output Capacitance (SO)	8	pF	V_{OUT} = 0V
C_{IN}(2)	Input Capacitance (SCK, SI, $\overline{CS}$, $\overline{PP}$)	6	pF	V_{IN} = 0V

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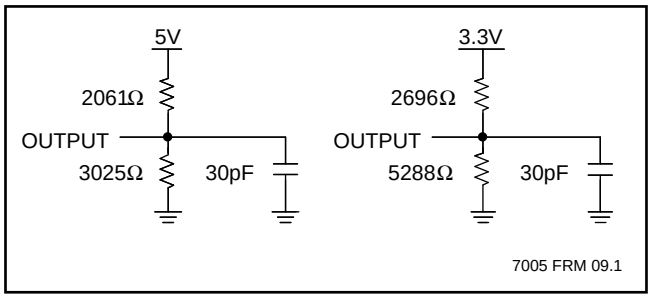
Notes: (1) V_{IL} Min. and V_{IH} Max. are for reference only and are not 100% tested.
(2) This parameter is periodically sampled and not 100% tested.
(3) t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated. These parameters are periodically sampled and not 100% tested.

EQUIVALENT A.C. LOAD CIRCUIT



A.C. TEST CONDITIONS

Input Pulse Levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input Rise and Fall Times	10ns
Input and Output Timing Level	V_{CC} X 0.5

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A.C. CHARACTERISTICS (Over the recommended operating conditions, unless otherwise specified.)

Data Input Timing

Symbol	Parameter	Min.	Max.	Units
f_{SCK}	Clock Frequency	0	1	MHz
t_{CYC}	Cycle Time	1000		ns
t_{LEAD}	$\overline{CS}$ Lead Time	500		ns
t_{LAG}	$\overline{CS}$ Lag Time	500		ns
t_{WH}	Clock HIGH Time	400		ns
t_{WL}	Clock LOW Time	400		ns
t_{SU}	Data Setup Time	100		ns
t_H	Data Hold Time	100		ns
t_{RI}(4)	Data In Rise Time		2	µs
t_{FI}(4)	Data In Fall Time		2	µs
t_{CS}	$\overline{CS}$ Deselect Time	2.0		µs
t_{WC}(5)	Write Cycle Time		10	ms

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Data Output Timing

Symbol	Parameter	Min.	Max.	Units
f_{SCK}	Clock Frequency	0	1	MHz
t_{DIS}	Output Disable Time		500	ns
t_V	Output Valid from Clock LOW		400	ns
t_{HO}	Output Hold Time	0		ns
t_{RO}(4)	Output Rise Time		300	ns
t_{FO}(4)	Output Fall Time		300	ns

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Notes: (4) This parameter is periodically sampled and not 100% tested.

(5) t_{WC} is the time from the rising edge of $\overline{CS}$ after a valid program sequence has been sent to the end of the self-timed internal nonvolatile write cycle.

Figure 7. Serial Output Timing

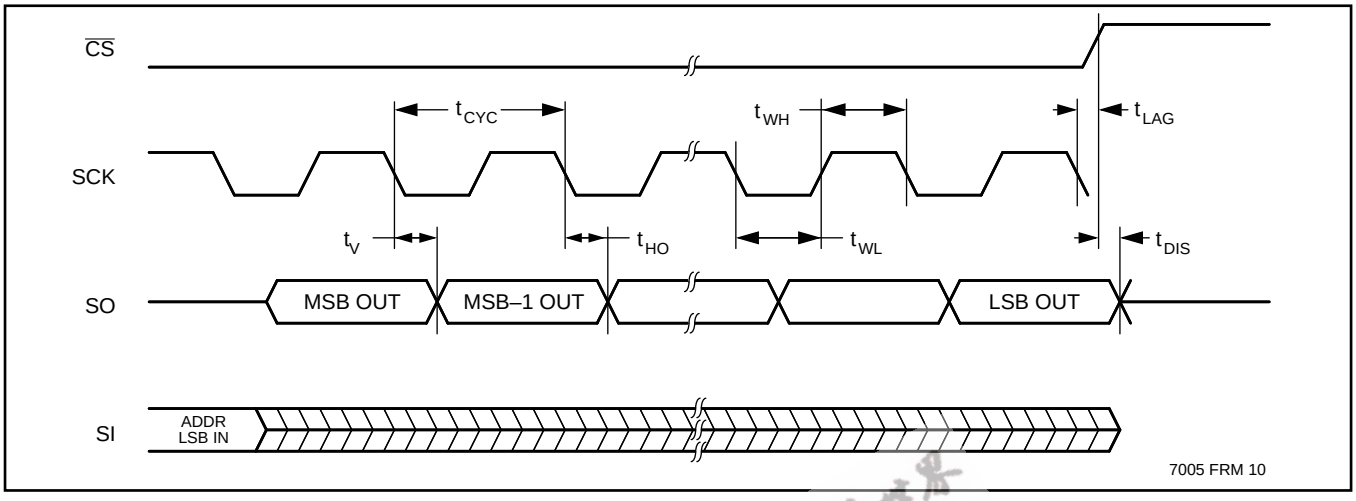
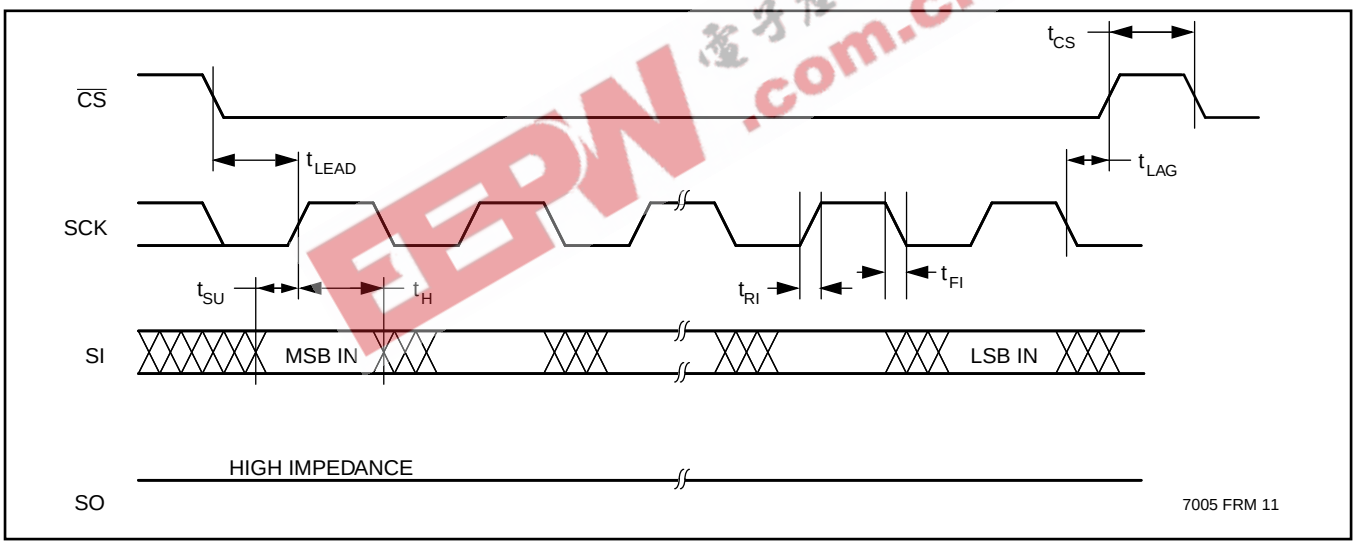


Figure 8. Serial Input Timing

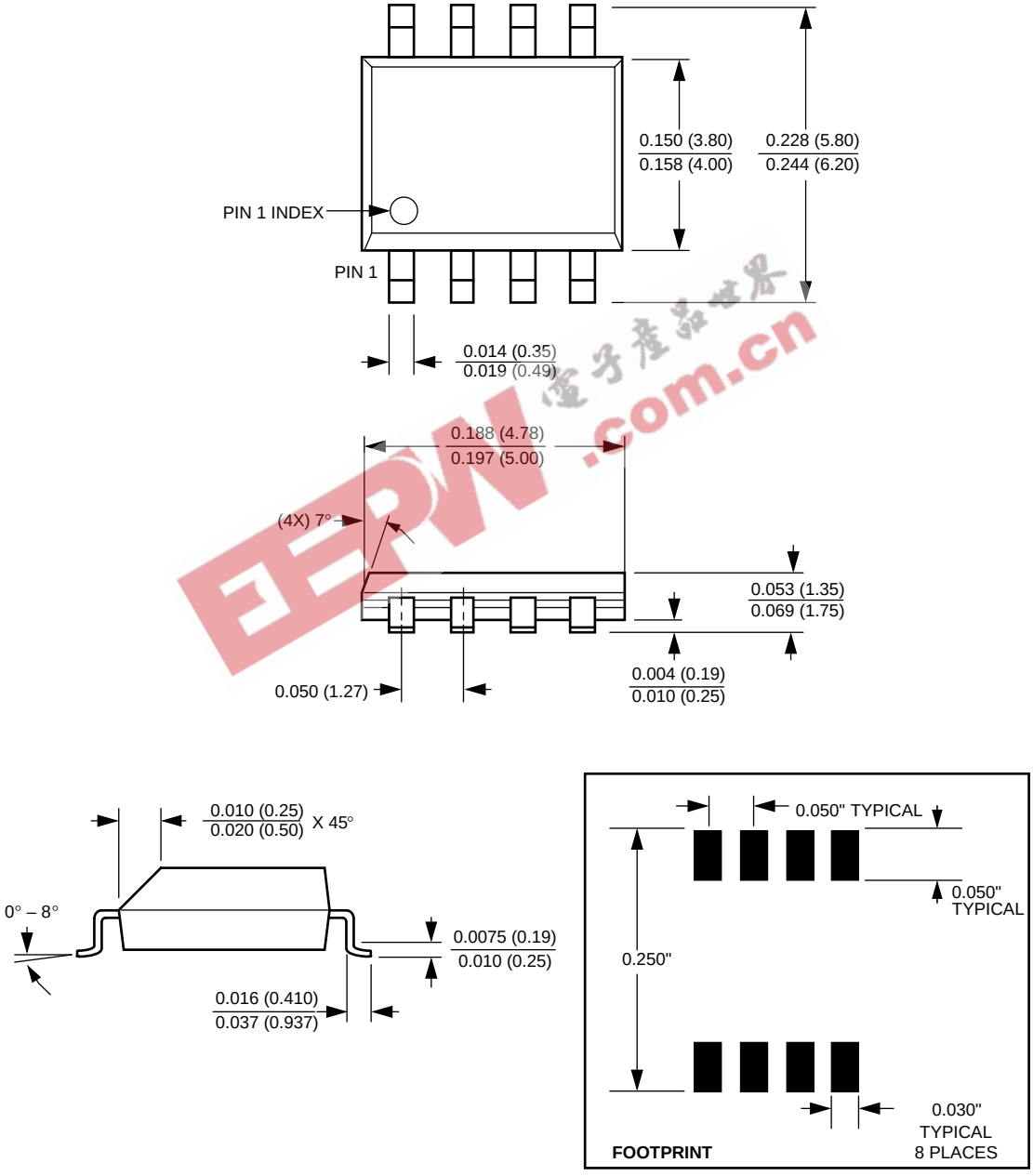


SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

PACKAGING INFORMATION

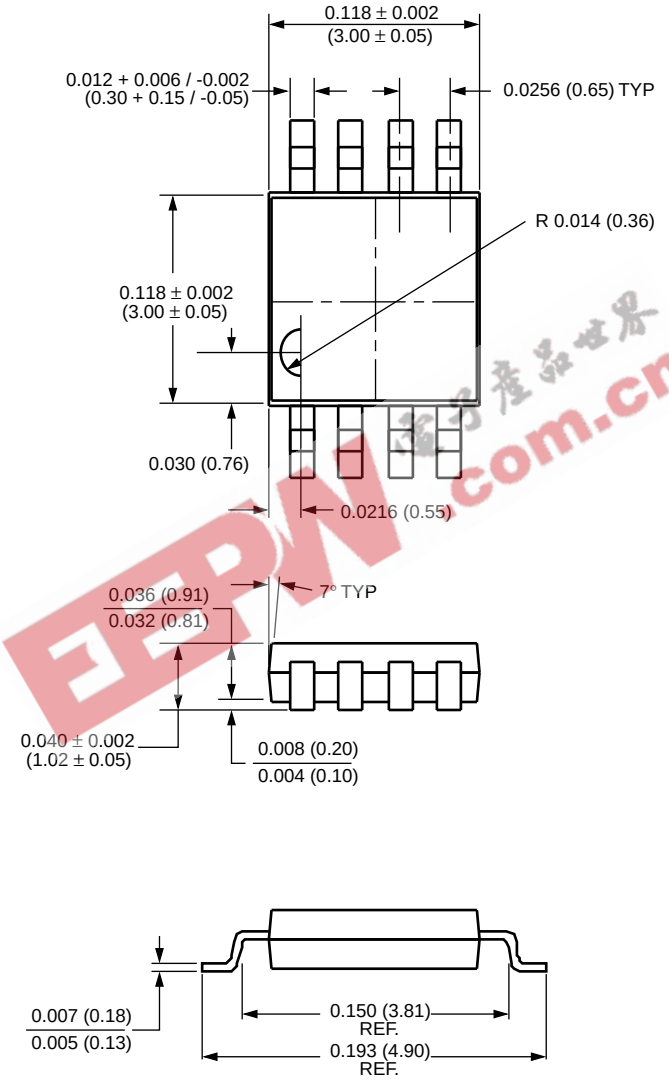
8-LEAD PLASTIC SMALL OUTLINE GULL WING PACKAGE TYPE S



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

PACKAGING INFORMATION

8-LEAD MINIATURE SMALL OUTLINE GULLWING PACKAGE TYPE M



NOTE:
1. ALL DIMENSIONS IN INCHES AND (MILLIMETERS)

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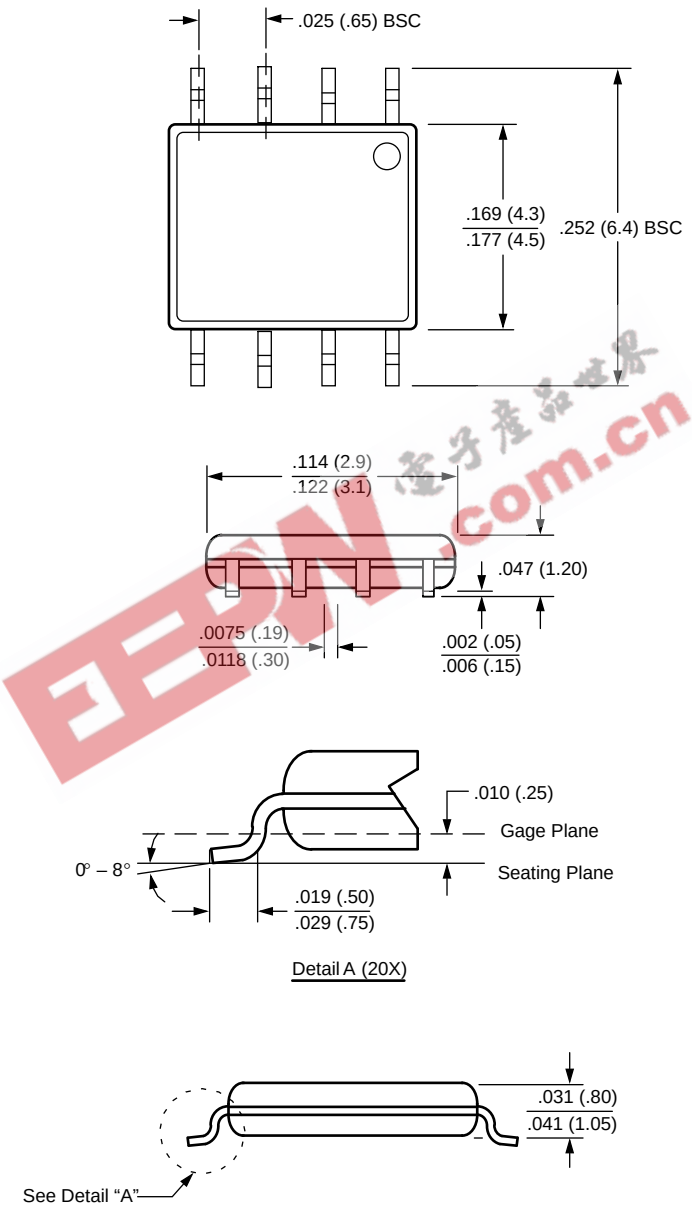
PACKAGING INFORMATION

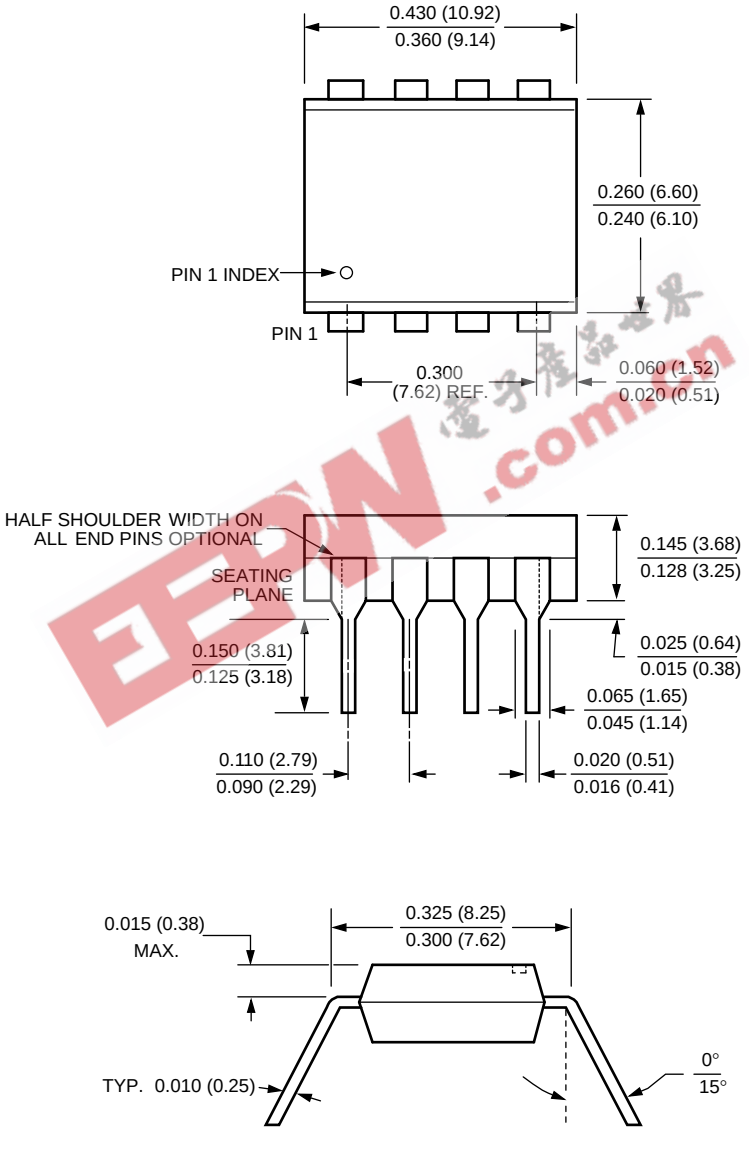
8-LEAD PLASTIC, TSSOP, PACKAGE TYPE V



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

PACKAGING INFORMATION

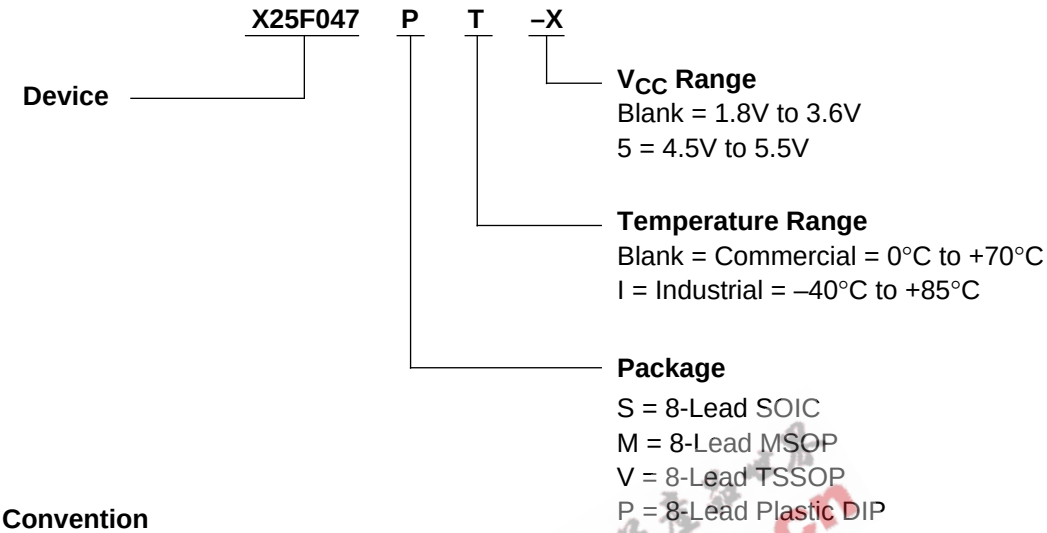
8-LEAD PLASTIC DUAL IN-LINE PACKAGE TYPE P



NOTE:

1. **ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)**
2. **PACKAGE DIMENSIONS EXCLUDE MOLDING FLASH**

ORDERING INFORMATION



Part Mark Convention

8-Lead MSOP

EYWW
XXX

AAH = 1.8 to 3.6V, 0°C to +70°C
AAI = 1.8 to 3.6V, -20°C to +85°C
AAJ = 1.8 to 3.6V, -40°C to +85°C
AAK = 2.5 to 5.5V, 0°C to +70°C
AAL = 2.5 to 5.5V, -40°C to +85°C
AAM = 4.5 to 5.5V, 0°C to +70°C
AAN = 4.5 to 5.5V, -40°C to +85°C

8-Lead TSSOP

EYWW
5F47XX

Blank = 1.8 to 3.6V, 0°C to +70°C
I = 1.8 to 3.6V, -40°C to +85°C
AE = 2.5 to 5.5V, 0°C to +70°C
AF = 2.5 to 5.5V, -40°C to +85°C
5 = 4.5 to 5.5V, 0°C to +70°C
I5 = 4.5 to 5.5V, -40°C to +85°C

8-Lead SOIC/PDIP

X25F047 X
XX

Blank = 8-Lead SOIC
P = 8-Lead Plastic DIP

Blank = 1.8 to 3.6V, 0°C to +70°C
I = 1.8 to 3.6V, -40°C to +85°C
AE = 2.5 to 5.5V, 0°C to +70°C
AF = 2.5 to 5.5V, -40°C to +85°C
5 = 4.5 to 5.5V, 0°C to +70°C
I5 = 4.5 to 5.5V, -40°C to +85°C