

APPLICATION NOTES
A V A I L A B L E
AN4 • AN12 • AN22 • AN26 • AN32



128 Bit

X24C00

16 x 8 Bit

Serial E<sup>2</sup>PROM

FEATURES

- 2.7V to 5.5V Power Supply
- 128 Bit Serial E<sup>2</sup>PROM
- Low Power CMOS
  - Active Current Less Than 3mA
  - Standby Current Less Than 50µA
- Internally Organized 16 x 8
- 2 Wire Serial Interface
  - Bidirectional Data Transfer Protocol
- Byte Mode Write
- Self Timed Write Cycle
  - Typical Write Cycle Time of 5ms
- Push/Pull Output
- High Reliability
  - Endurance: 100,000 Cycles
  - Data Retention: 100 Years
- Available Packages
  - 8-Lead MSOP
  - 8-Lead PDIP
  - 8-Lead SOIC

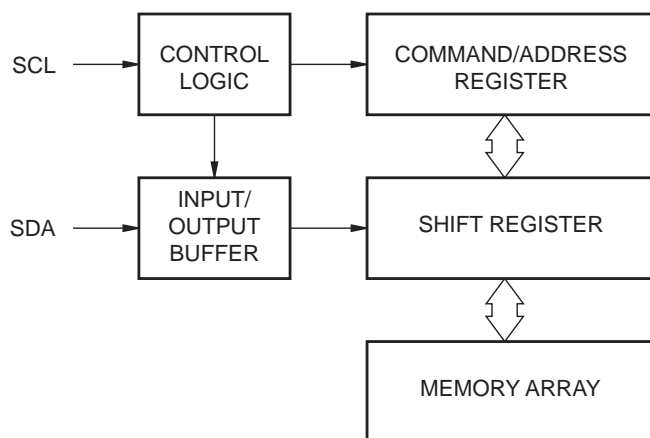
DESCRIPTION

The X24C00 is a CMOS 128 bit serial E<sup>2</sup>PROM, internally organized as 16 x 8. The X24C00 features a serial interface and software protocol allowing operation on a simple two wire bus.

Xicor E<sup>2</sup>PROMs are designed and tested for applications requiring extended endurance. Inherent data retention is greater than 100 years.

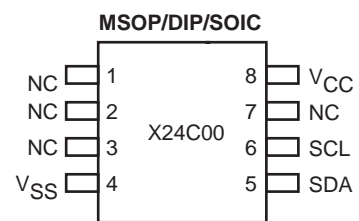
The X24C00 is fabricated with Xicor's Advanced CMOS Floating Gate technology.

FUNCTIONAL DIAGRAM



3836 FHD F01

PIN CONFIGURATION



3836 FHD F02.1

# X24C00

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## PIN DESCRIPTIONS

### Serial Clock (SCL)

The SCL input is used to clock all data into and out of the device.

### Serial Data (SDA)

SDA is a bidirectional pin used to transfer data into and out of the device. It is a push/pull output and does not require the use of a pull-up resistor.

## PIN NAMES

Symbol	Description
NC	No Connect
V <sub>SS</sub>	Ground
V <sub>CC</sub>	Supply Voltage
SDA	Serial Data
SCL	Serial Clock

3836 PGM T01

## DEVICE OPERATION

The X24C00 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master will always initiate data transfers and provide the clock for both transmit and receive operations. Therefore, the X24C00 will be considered a slave in all applications.

## Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions. Refer to Figures 1 and 2.

### Start Condition

All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The X24C00 continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

A start may be issued to terminate the input of a control word or the input of data to be written. This will reset the device and leave it ready to begin a new read or write command. Because of the push/pull output, a start cannot be generated while the part is outputting data. Starts are also inhibited while a write is in progress.

### Stop Condition

The stop condition is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is used to reset the device during a command or data input sequence and will leave the device in the standby mode. As with starts, stops are inhibited when outputting data and while a write is in progress.

### Write Operation

The byte write operation is initiated with a start condition. The start condition is followed by an eight bit control byte which consists of a two bit write command (0,1), four address bits, and two "don't care" bits (Figure 3).

# X24C00

Figure 1. Data Validity

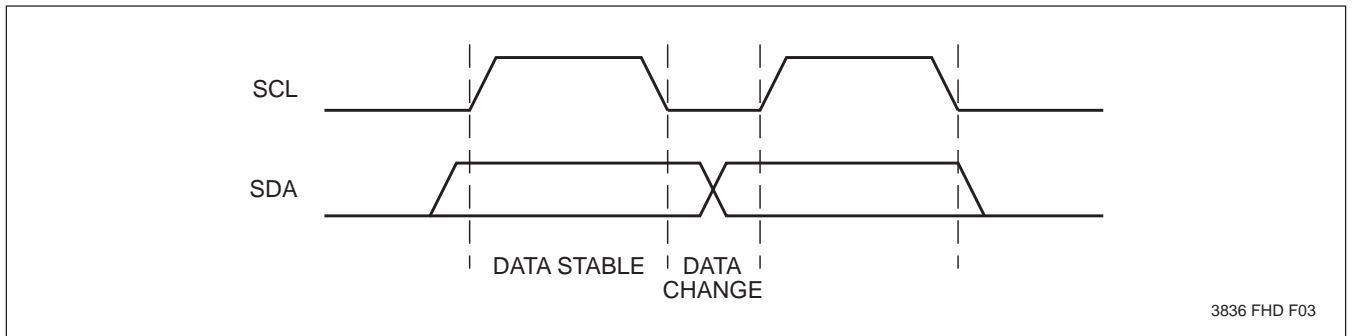


Figure 2. Definition of Start and Stop Conditions

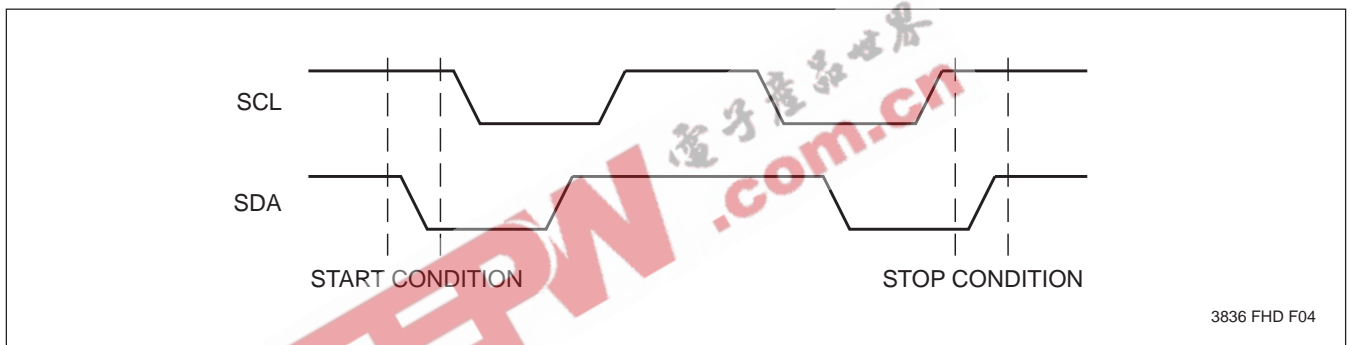
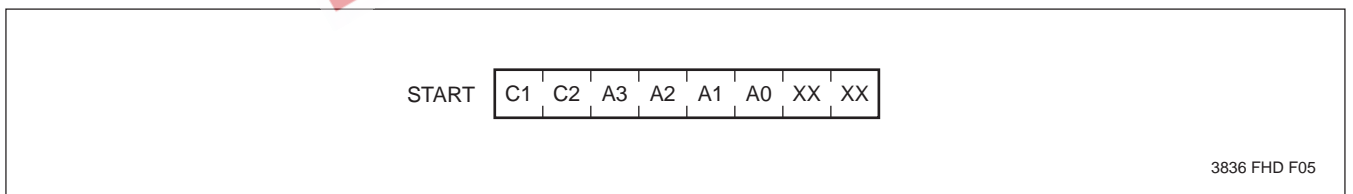


Figure 3. Control Byte



# X24C00

After receipt of the control byte, the X24C00 will enter the write mode and await the data to be written. This data is shifted into the device on the next eight SCL clocks. Once eight clocks have been received, the data in the shift register will be written into the memory array. While the write is in progress the X24C00 will not respond to any inputs. At any time prior to clocking in the last data bit, a stop command or a new start command will terminate the operation. If a start command is given, the X24C00 will reset all counters and will prepare to clock in the next control byte. If a stop command is given, the X24C00 will reset all counters and await the next start command.

At the end of the write the X24C00 will automatically reset all counters and enter the standby mode. (Figure 4).

## Read Operation

The byte read operation is initiated with a start condition. The start condition is followed by an eight-bit control byte which consists of a two-bit read command (1,0), four address bits, and two “don’t care” bits. After receipt of the control byte the X24C00 will enter the read mode and transfer data into the shift register from the array. This data is shifted out of the device on the next eight SCL clocks. At the end of the read, all counters are reset and the X24C00 will enter the standby mode. As with a write, the read operation can be interrupted by a start or stop condition while the command or address is being clocked in. While clocking data out, starts or stops cannot be generated.

During the second don’t care clock cycle, starts and stops are ignored. The master must free the bus prior to the end of this clock cycle to allow the X24C00 to begin outputting data (Figures 5 and 6).

Figure 4. Write Sequence



Figure 5. Read Sequence

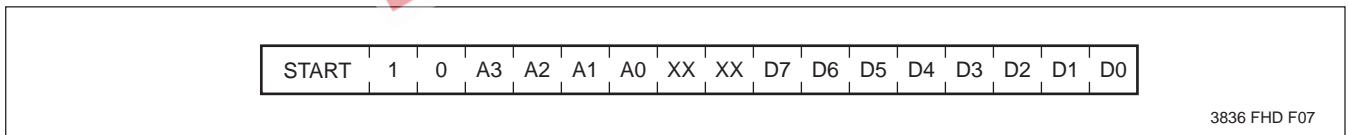
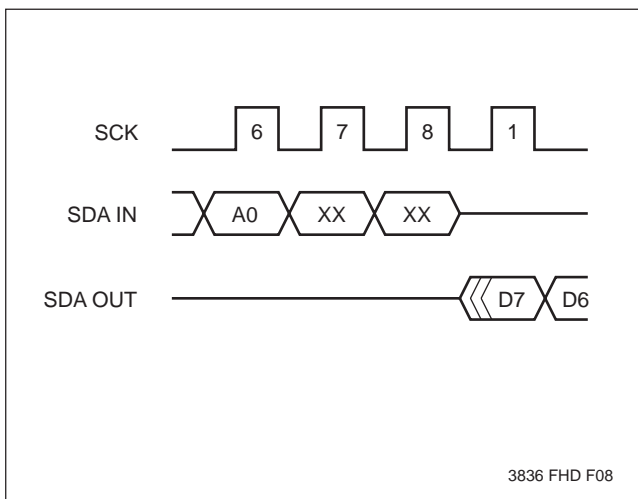


Figure 6. Read Cycle Timing



## SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

# X24C00

## ABSOLUTE MAXIMUM RATINGS\*

Temperature under Bias	
X24C00 .....	-65°C to +135°C
Storage Temperature .....	-65°C to +150°C
Voltage on any Pin with	
Respect to $V_{SS}$ .....	-1V to +7V
D.C. Output Current .....	5mA
Lead Temperature	
(Soldering, 10 seconds) .....	300°C

## \*COMMENT

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	+70°C
Industrial	-40°C	+85°C
Military	-55°C	+125°C

3836 PGM T02.1

Supply Voltage	Limits
X24C00	5V ±10%
X24C00-3	3V to 5.5V
X24C00-2.7	2.7V to 5.5V

3836 PGM T03.1

## D.C. OPERATING CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
$I_{CC1}$	$V_{CC}$ Supply Current Read		1	mA	SCL = $V_{CC} \times 0.1/V_{CC} \times 0.9$ Levels @ 1MHz, SDA = Open
$I_{CC2}$	$V_{CC}$ Supply Current Write		3		
$I_{SB1}$	$V_{CC}$ Standby Current		100	$\mu A$	SCL = SDA = $V_{CC}$ $V_{CC} = 5V \pm 10\%$
$I_{SB2}$	$V_{CC}$ Standby Current		50	$\mu A$	SCL = SDA = $V_{CC}$ $V_{CC} = 2.7V$
$I_{LI}$	Input Leakage Current		10	$\mu A$	$V_{IN} = V_{SS}$ to $V_{CC}$
$I_{LO}$	Output Leakage Current		10	$\mu A$	$V_{OUT} = V_{SS}$ to $V_{CC}$
$V_{IL}^{(1)}$	Input LOW Voltage	-1	$V_{CC} \times 0.3$	V	
$V_{IH}^{(1)}$	Input HIGH Voltage	$V_{CC} \times 0.7$	$V_{CC} + 0.5$	V	
$V_{OL}$	Output LOW Voltage		0.4	V	$I_{OL} = 2.1mA$
$V_{OH}$	Output HIGH Voltage	$V_{CC} - 0.8$		V	$I_{OH} = 1mA$

3841 PGM T04.3

## CAPACITANCE $T_A = +25^\circ C, f = 1MHz, V_{CC} = 5V$

Symbol	Parameter	Max.	Units	Test Conditions
$C_{I/O}^{(2)}$	Input/Output Capacitance (SDA)	8	pF	$V_{I/O} = 0V$
$C_{IN}^{(2)}$	Input Capacitance (SCL)	6	pF	$V_{IN} = 0V$

3836 PGM T05.1

- Notes:** (1)  $V_{IL}$  min. and  $V_{IH}$  max. are for reference only and are not tested.  
(2) This parameter is periodically sampled and not 100% tested.

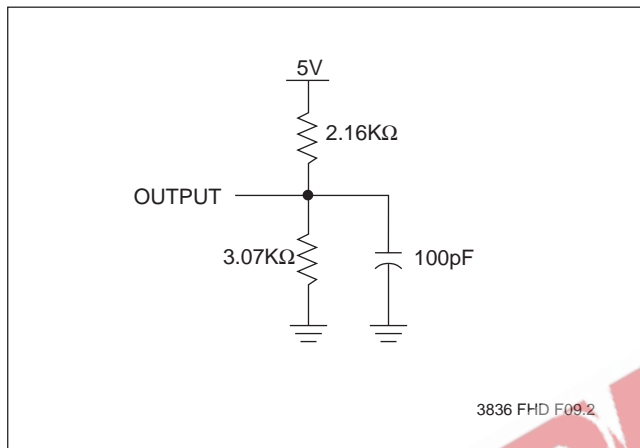
# X24C00

## POWER-UP TIMING

Symbol	Parameter	Max.	Units
$t_{PUR}^{(3)}$	Power-up to Read Operation	2	ms
$t_{PUW}^{(3)}$	Power-up to Write Operation	5	ms

3836 PGM T08

## EQUIVALENT A.C. LOAD CIRCUIT



## A.C. CONDITIONS OF TEST

Input Pulse Levels	$V_{CC} \times 0.1$ to $V_{CC} \times 0.9$
Input Rise and Fall Times	10ns
Input and Output Timing Levels	$V_{CC} \times 0.5$

3836 PGM T06.1

## A.C. CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified.)

### Read & Write Cycle Limits

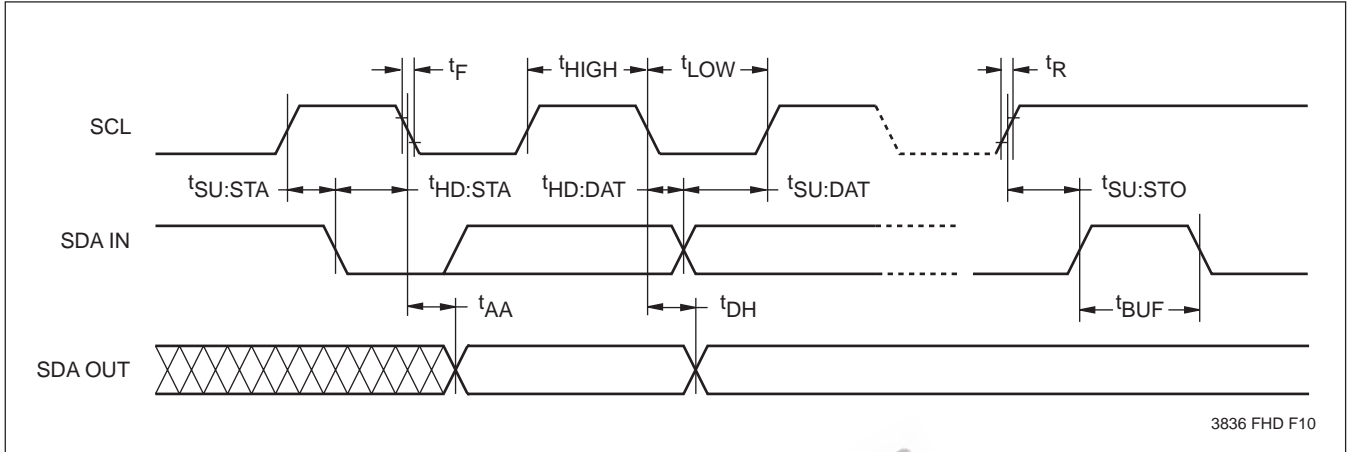
Symbol	Parameter	Min.	Max.	Units
$f_{SCL}$	SCL Clock Frequency	0	1	MHz
$t_{AA}$	SCL LOW to SDA Data Out Valid		350	ns
$t_{BUF}$	Time the Bus Must Be Free Before a New Transmission Can Start	500		ns
$t_{HD:STA}$	Start Condition Hold Time	250		ns
$t_{LOW}$	Clock LOW Period	500		ns
$t_{HIGH}$	Clock HIGH Period	500		ns
$t_{SU:STA}$	Start Condition Setup Time	250		ns
$t_{HD:DAT}$	Data In Hold Time	0		$\mu s$
$t_{SU:DAT}$	Data in Setup Time	250		ns
$t_R$	SDA and SCL Rise Time		1	$\mu s$
$t_F$	SDA and SCL Fall Time		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	250		ns
$t_{DH}$	Data Out Hold Time	50		ns

3836 PGM T07.1

**Note:** (3)  $t_{PUR}$  and  $t_{PUW}$  are the delays required from the time  $V_{CC}$  is stable until the specified operation can be initiated. These parameters are periodically sampled and not 100% tested.

# X24C00

## Bus Timing

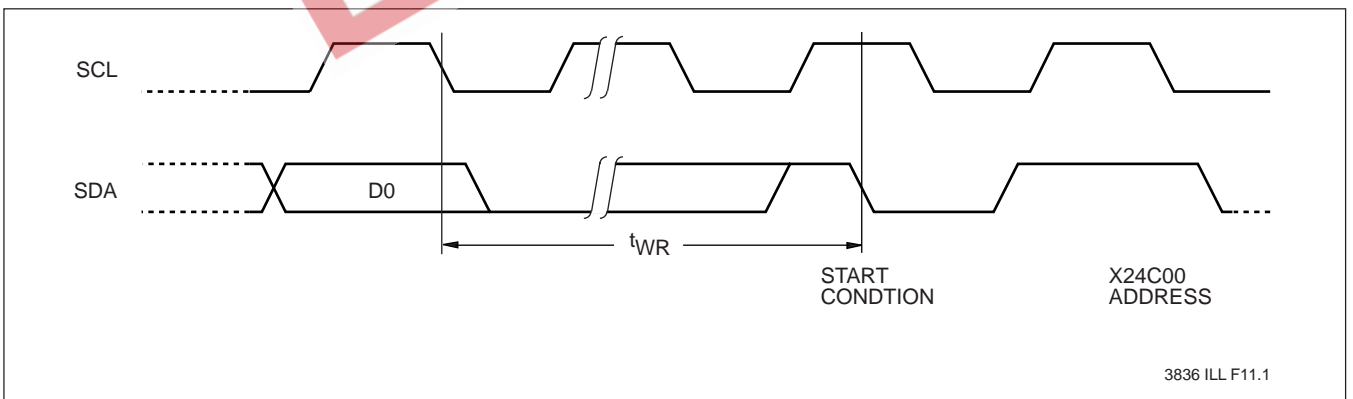


## WRITE CYCLE LIMITS

Symbol	Parameter	Min.	Max.	Units
$t_{WR}^{(4)}$	Write Cycle Time		5	ms

3836 PGM T09

## Write Cycle Timing



**Note:** (4) The write cycle time is the time from the initiation of a write sequence to the end of the internal erase/program cycle. During the write cycle, the X24C00 bus interface circuits are disabled, SDA is high impedance, and the device does not respond to start conditions.

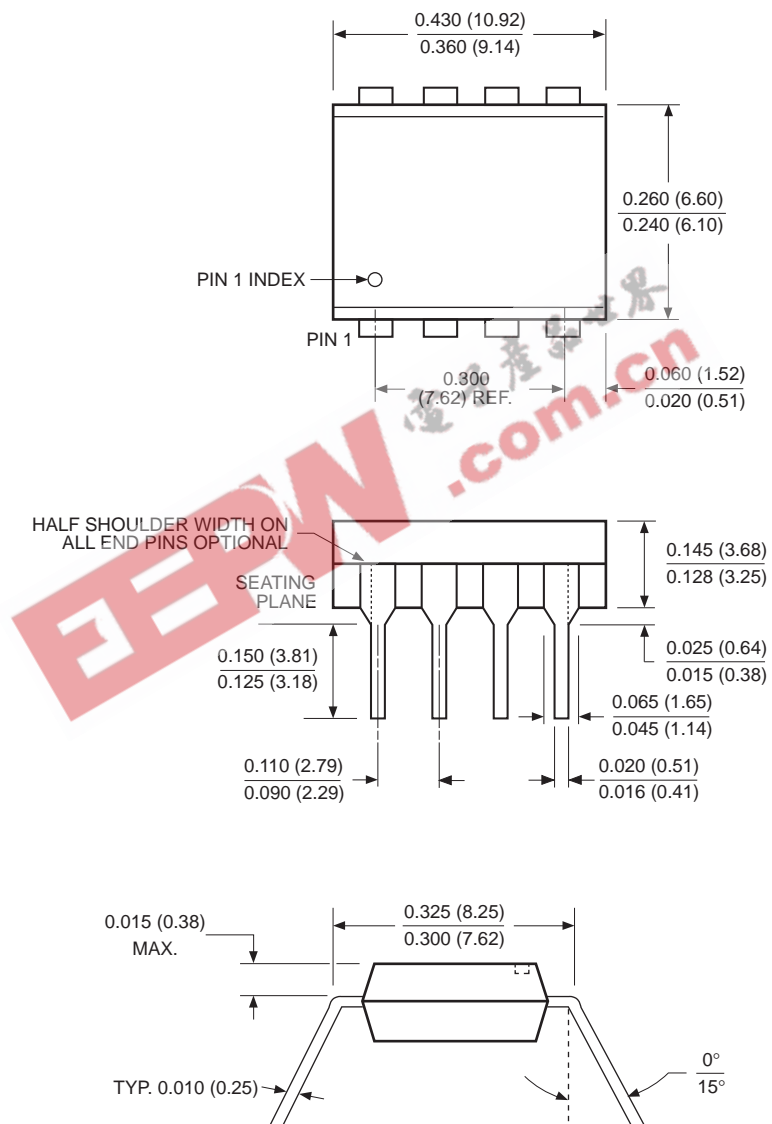




# X24C00

## PACKAGING INFORMATION

### 8-LEAD PLASTIC DUAL IN-LINE PACKAGE TYPE P



**NOTE:**

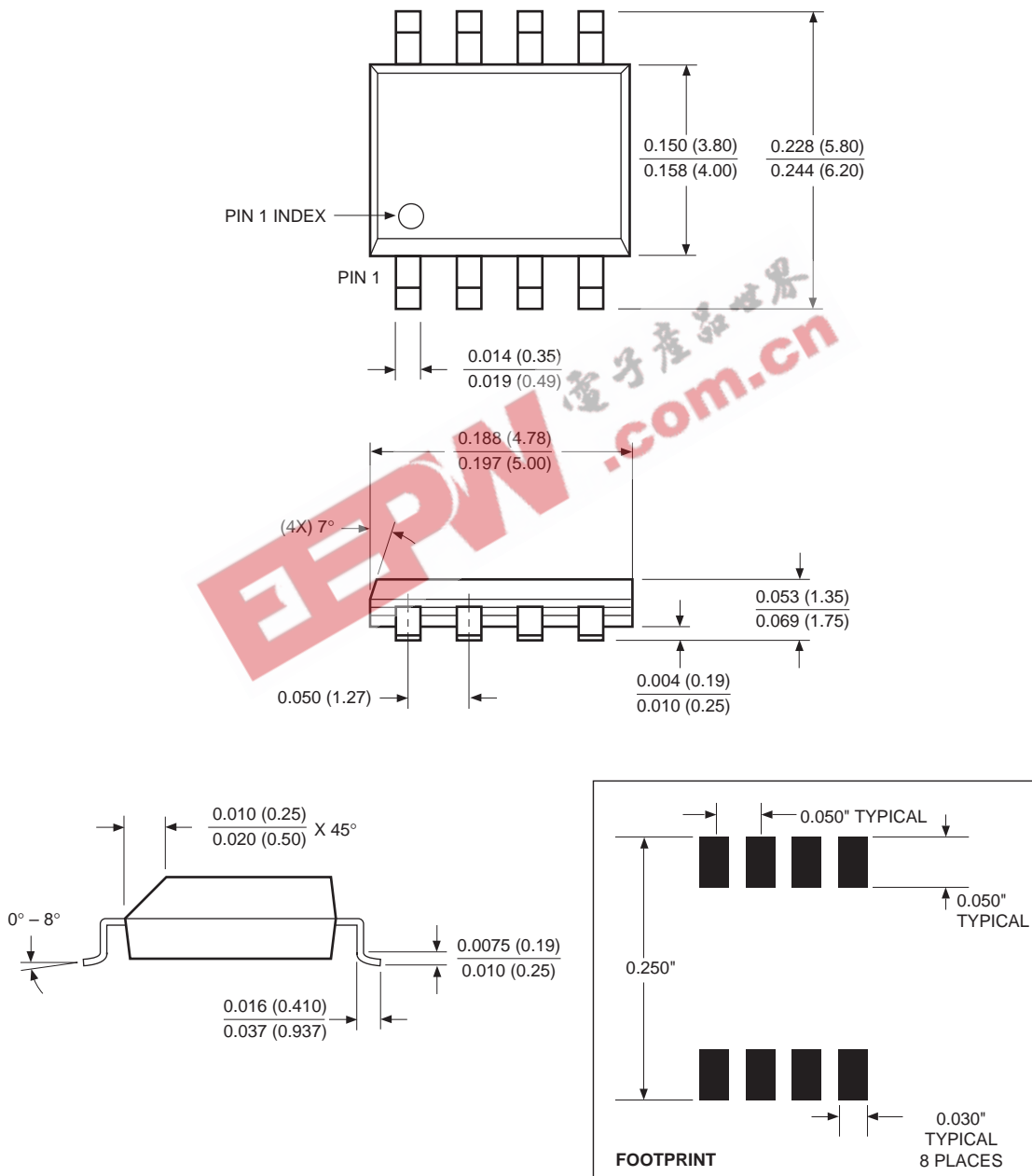
1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
2. PACKAGE DIMENSIONS EXCLUDE MOLDING FLASH

3926 FHD F01

# X24C00

## PACKAGING INFORMATION

### 8-LEAD PLASTIC SMALL OUTLINE GULL WING PACKAGE TYPE S

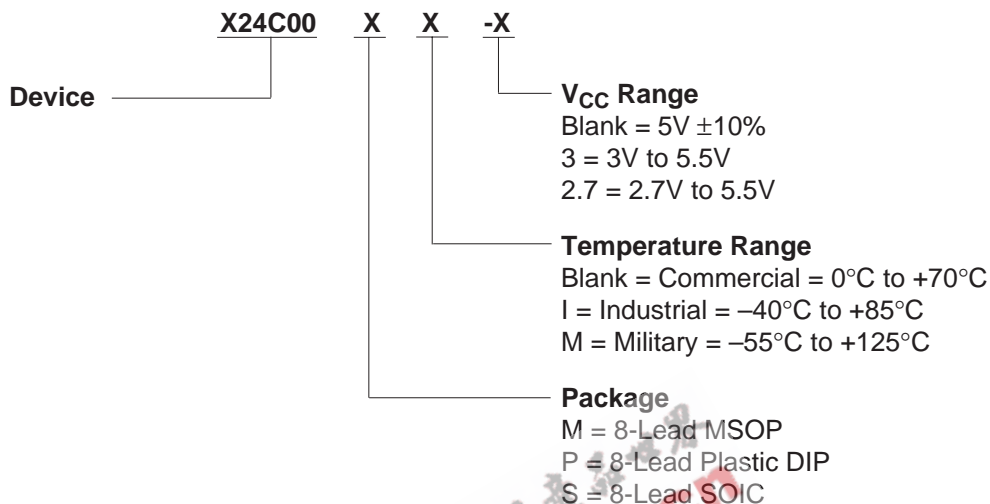


NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

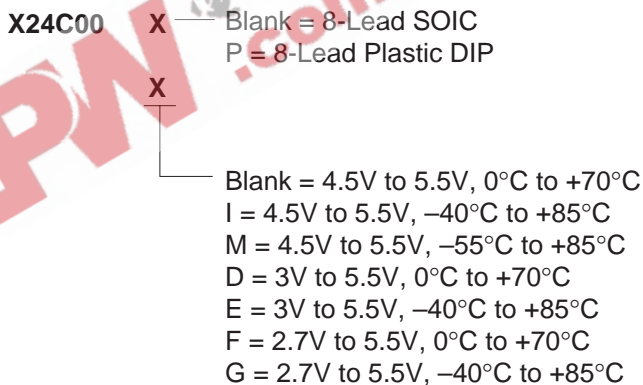
3926 FHD F22.1

# X24C00

## ORDERING INFORMATION



## Part Mark Convention



## LIMITED WARRANTY

Devices sold by Xicor, Inc. are covered by the warranty and patent indemnification provisions appearing in its Terms of Sale only. Xicor, Inc. makes no warranty, express, statutory, implied, or by description regarding the information set forth herein or regarding the freedom of the described devices from patent infringement. Xicor, Inc. makes no warranty of merchantability or fitness for any purpose. Xicor, Inc. reserves the right to discontinue production and change specifications and prices at any time and without notice.

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## US. PATENTS

Xicor products are covered by one or more of the following U.S. Patents: 4,263,664; 4,274,012; 4,300,212; 4,314,265; 4,326,134; 4,393,481; 4,404,475; 4,450,402; 4,486,769; 4,488,060; 4,520,461; 4,533,846; 4,599,706; 4,617,652; 4,668,932; 4,752,912; 4,829,482; 4,874,967; 4,883,976; 4,980,859; 5,012,132; 5,003,197; 5,023,694. Foreign patents and additional patents pending.

## LIFE RELATED POLICY

In situations where semiconductor component failure may endanger life, system designers using this product should design the system with appropriate error detection and correction, redundancy and back-up features to prevent such an occurrence.

Xicor's products are not authorized for use as critical components in life support devices or systems.

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.