X5114

System Controller

FEATURES

- **Simplifies Backplane Communications**
- **Monitor Fault and "Hot Docking" Conditions**
- **Ten Level Selectable Input Threshold**
- **Two Fully Redundant SPI Serial I/O Ports**
- **Programmable Output or Input Port Pins**
  - **—16 General I/O pins**
  - **—8 bit Port with 4 Handshake Modes**
    - **Single Read Input Mode**
    - **Multiple Read Input Mode**
    - **Output Mode**
    - **Bidirectional Mode**
  - **—Port Tristate Control**
- **Programmable Interrupt and Mask Options**
- **8-bit Direct Address Decoder allows Cascaded 255+ devices on one SPI bus**
- **4K bits of EEPROM with 32 byte page write**
- **Default Output Data on Port at Power-up**
- **High Reliability EEPROM**
  - **—Endurance - 10^5 Data Changes**
  - **—Data Retention - 100 years**
- **44-Pin PLCC, 48-Lead TQFP**

DESCRIPTION

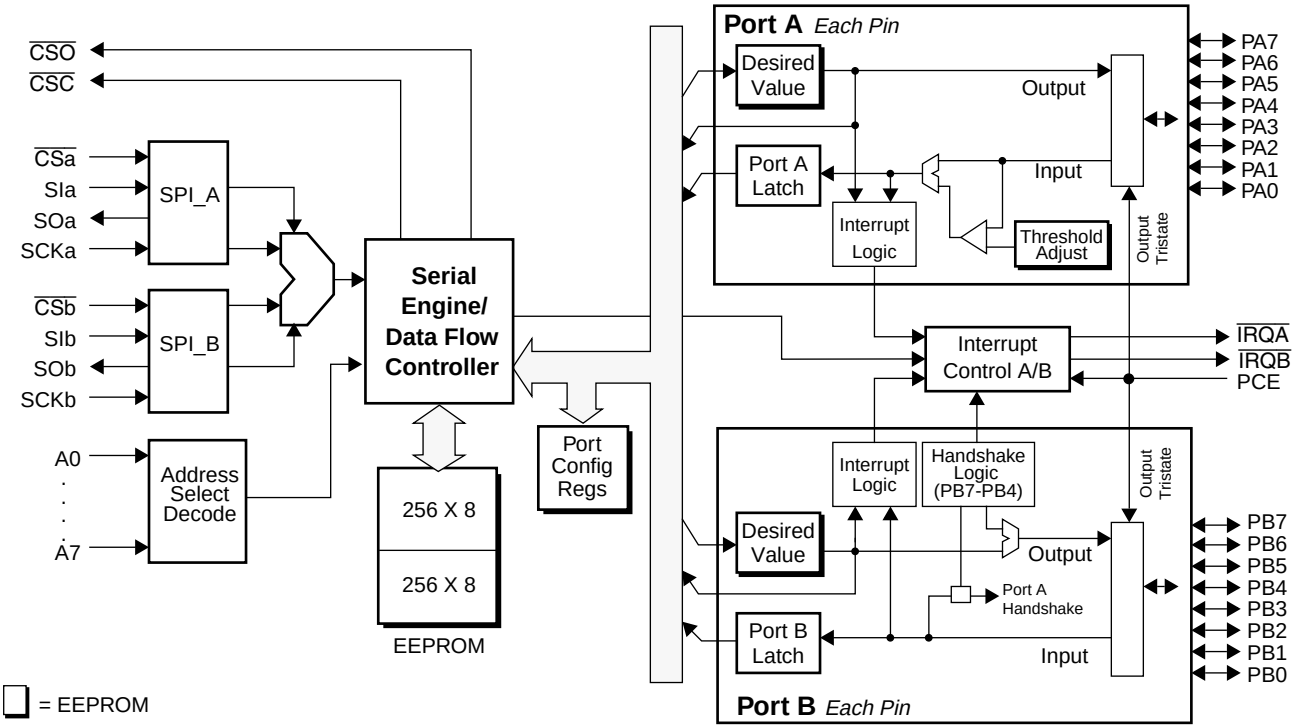
The X5114 is a single-chip system controller that is used in applications such as multiprocessing, telecommunications, data communications, cable systems, set top boxes, etc. The chip can implement features such as backplane communication, hot docking, cable diagnostics, etc.

The X5114 makes extensive use of nonvolatile memory with 4,096 bits of general purpose EEPROM, nonvolatile configuration registers, and nonvolatile programming of the port pins. The ports can be set up as sixteen general I/Os with pin selectable data direction (including eight inputs with nonvolatile threshold selections) or as an eight bit port with handshake. The chip is controlled via two redundant 2MHz SPI serial ports.

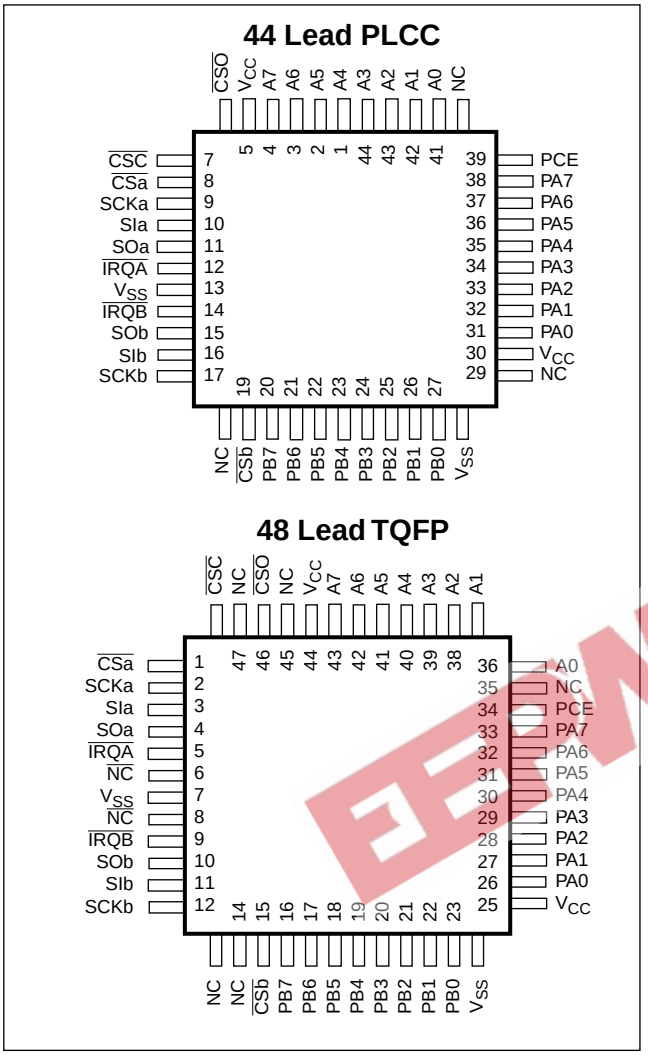
A sophisticated interrupt controller provides notification of a failed SPI command, changing conditions on an input, handshake status, and I/O errors. Interrupts are maskable.

On-chip EEPROM provides nonvolatile storage of system status, manufacturing information, board ID or other parameters.

FUNCTIONAL DIAGRAM



PIN CONFIGURATION



PIN NAMES

Symbol	Function
SCKa, SCKb	SPI A, B Serial Clock
SIa, SIb, SOa, SOb	SPI A, B, Serial Data I/O
$\overline{CSa}$, $\overline{CSb}$	SPI A, B select
A7-A0	Device Address
$\overline{IRQA}$, $\overline{IRQB}$	Interrupt A, B Outputs
PCE	Port Chip Enable
PA7-PA0	Port A pins
PB7-PB0	Port B pins
CSO	Chip Select Output
CSC	Chip Select Cascade Output
V_{CC}, V_{SS}	System Supply, Ground
NC	No Connection

PIN DESCRIPTIONS

$\overline{CSa}$ /$\overline{CSb}$ (SPI A/B Chip Select)

These are schmitt trigger input pins used by the host system to select the X5114 SPI port. A HIGH to LOW (falling) transition on $\overline{CSa}$ or $\overline{CSb}$ starts the X5114 serial access. Both of these pins at logic “1” deselects the device and places the SOa and SOb pins in a high impedance state. In the event of a stuck LOW on either of these pins, a HIGH to LOW transition on the other chip select will override the inoperative serial port.

SCKa/SCKb (SPI A/B Serial Clock)

These are schmitt trigger input pins used by the host system to supply the SPI serial clock. Only clock mode 3 is supported by X5114. When inactive, the SPI serial clock is to be driven to a logic HIGH level.

SIa/SIb (SPI A/B Serial Input)

These are schmitt trigger, serial data inputs. They receive device address, opcode, and data from the host system at the rising edge of the serial clock (i.e. SCKa or SCKb).

SOa/SOb (SPI A/B Serial Output)

These are push-pull serial data outputs. They shift out data after each falling edge of the serial clock and are stable on the rising edge of the serial clock (i.e. SCKa or SCKb). When the device is not outputting data or is in standby, the serial data outputs will be in a high impedance state.

$\overline{IRQA}$/$\overline{IRQB}$ (Interrupt Outputs)

These are open-drain Interrupt Request output pins. They are designed for multidrop wired ORing. Internal registers control the operation of the IRQ lines. See "CONTROL/STATUS REGISTERS" on page 12 for information about the internal control registers. See “INTERRUPT REQUESTS” on page 23. for an operational description of the IRQ lines.

PA7-PA0/PB7-PB0 (Port A/Port B)

Each bit of these 8-bit ports can be programmed to act as either an input or output. An 8-bit nonvolatile Data Direction Control Register for each port (DDRA/DDRB) controls the direction of each pin. All I/Os can enter a high impedance state when PCE is inactive. This is a configurable option (see "Port I/O Configuration Register (PCR)" on page 14 for details). In addition to the I/O programmability, Port A and Port B can be configured with handshake to provide a high speed parallel data transfer pathway. See "Handshake I/O subsystem" on page 17 for details.

A7-A0 (Device Address Inputs)

These inputs set a slave address for the X5114 (see "Device Addressing" on page 3 for details about addressing modes). These pins can be either hardwired or actively driven. If hardwired, these pins need to be tied to Vcc or Vss. If actively driven, the pins must be driven to V_{IH} or V_{IL} and they must be constant and stable during each transmission period.

V_{CC} (System Supply)

This is the system supply voltage input for the device. Two V_{CC} pins are provided.

V_{SS} (System Ground)

This is the system ground voltage reference input for the device. Two V_{SS} pins are provided.

$\overline{CSO}$ (Chip Select Output)

This is an output pin to indicate that the host system is in communication with the device. The $\overline{CSO}$ is asserted active LOW (logic “0”) whenever the device is selected by the host system. The $\overline{CSO}$ shall remain active during all communications and shall be de-asserted with the rising edge of either the $\overline{CSa}$ or the $\overline{CSb}$ signal. This signal helps manage access to the SPI ports by two independent host processors.

$\overline{CSC}$ (Chip Select Cascade Output)

This is an output pin that enables device cascading. When receiving a NOP instruction, the device asserts the $\overline{CSC}$ signal active LOW (logic “0”). This enables another bank of devices while the device executing the NOP ignores subsequent commands and data. The rising edge of either the $\overline{CSa}$ or the $\overline{CSb}$ signal de-assertes the $\overline{CSC}$ signal.

PCE (Port Chip Enable)

This is a dedicated active HIGH schmitt trigger input pin to the X5114. The primary function of this input is to inhibit the generation of interrupts via an external control signal. When de-asserted (logic “0”), this input disables the $\overline{IRQA}$ and $\overline{IRQB}$ outputs. This input may be configured to both disable the $\overline{IRQA}$ and $\overline{IRQB}$ outputs and tri-state all of the Port A and Port B output drivers when de-asserted.

DEVICE ARCHITECTURE

The X5114 consists of two major sections. The first is a dual independent SPI serial interface. This full duplex interface provides seperate SPI ports for primary and secondary host controllers, but does not support simultaneous access. The SPI interface is compatible with industry standard SPI hardware. The host uses a command protocol to read the status of the X5114, to read and write various function registers that control device operation and to access the memory array.

The second section of the X5114 consists of a sophisticated port structure. The dual 8 bit ports can be configured in a number of ways to meet the specific needs of the application. The port can serve as a general I/O, with default outputs or default input compare values. The port can also be configured with one of four different handshake options.

In addition to these two main sections, an interrupt controller can be configured to report a number of conditions back to the host microcontroller. See Figure 21 on page 23. These include failed SPI communications, input changes, handshake conditions, or port interrupts.

SERIAL COMMUNICATIONS

Two independent Serial Peripheral Interface (SPI) Ports provide the primary communication connection to the X5114.

Device Addressing

The X5114 supports a bidirectional bus oriented protocol. This protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is a slave.

The master will always initiate data transfers and provide the clock for both transmit and receive operations. The X5114 is considered a slave for all operations.

The X5114 has special addressing mechanisms to allow up to 255 devices (or more after using the NOP command) to reside on one SPI communication bus. This reduces the number of bus lines required to talk to multiple X5114 devices.

Communication to the device begins with a start condition. This consists of the falling edge of $\overline{CSa}$ or $\overline{CSb}$. Following a $\overline{CSa}$/$\overline{CSb}$ HIGH to LOW, the master selects one of many X5114 devices on the SPI bus, by transmitting a slave address (Software Device Addressing) or selects the only device on the bus using the $\overline{CSa}$/$\overline{CSb}$ signal (Hardware Device Addressing).

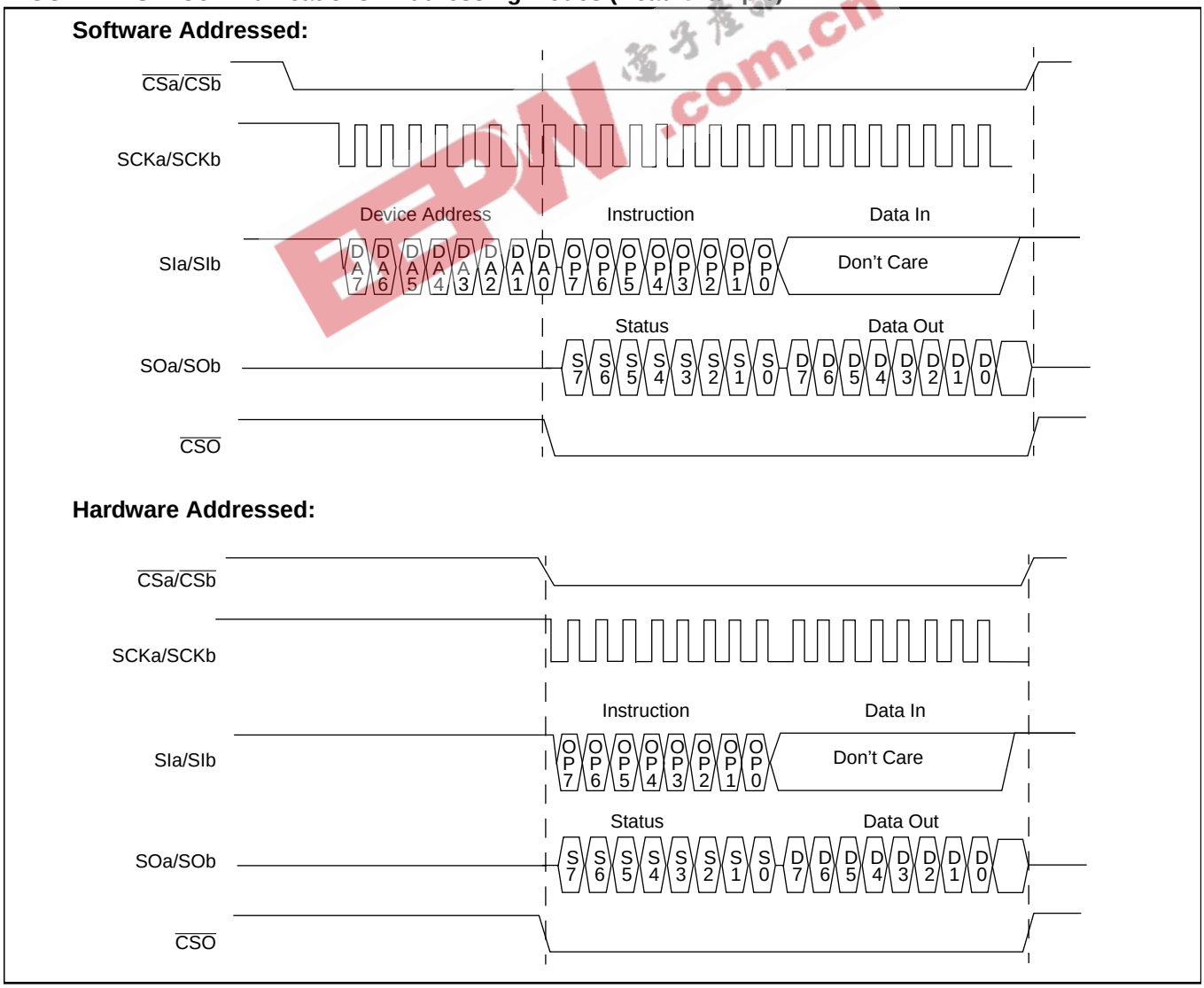
Software Device Addressing Mode

In this device addressing mode, each X5114 has a unique slave address externally specified by the A7-A0 pins. The first byte transmitted to the device contains the device address. This address is compared with the external address pins, A7-A0. If matched, the device performs the task specified by the Instruction opcode sent in the next byte. If there is no match, the X5114 returns to the standby state.

Device Address (Software Addressing only)

DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
MSB							LSB

FIGURE 1. SPI Communications - Addressing Modes (Read example)



Hardware Device Addressing Mode

In this addressing mode, all the external address pins are tied to logic “0”. The device is selected solely by the $\overline{CSa}$ or $\overline{CSb}$ pins. As soon as the $\overline{CSa}$ or $\overline{CSb}$ pin goes LOW and stays LOW, the device will be in the active state. No slave address byte is needed in this mode.

Chip Select Output/Device Cascade ($\overline{CSO}$/$\overline{CSC}$)

The $\overline{CSO}$ and $\overline{CSC}$ output pins have two major functions. The $\overline{CSO}$ pin can be used as a chip select indicator. This signal indicates that the host processor has selected this device.

The $\overline{CSC}$ signal allows the cascade of multiple banks of X5114 devices. In a cascade mode, the $\overline{CSC}$ output of a selected X5114 selects another external device by using the NOP instruction. (see "NOP" on page 7)

Instruction Opcode

The second byte transmitted to the device (or the first byte in hardware addressing mode) contains the Instruction opcode that defines the operation to be performed. All the opcode bits have been specially arranged to achieve a 2-bit difference between opcodes to reduce the possibility of inadvertent operations.

Instruction Opcode

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MSB							LSB

OP7, OP6

“00” = memory operation,

“01” = port A operation,

“10” = port B operation,

“11” = Control Register operation.

OP5, OP4

“01” = port-related read command,

“10” = port-related write command.

OP3, OP2, OP1, OP0

“0000” = Configuration Register operation,

“0001” = Port Latch operation,

“0010” = Port Desired Value Register operation,

“0100” = Port Data Direction Register operation,

“1000” = Port IRQ Mask Register operation,

“0011” = Port IRQ Configuration Register operation,

“0101” = Port I/O Configuration Register operation,

“1100” = Port IRQ Error Register operation,

“1110” = Port IRQ Failed Command Register operation,

“1111” = Port Registers operation.

INSTRUCTION SUMMARY

Each instruction must be proceeded with a HIGH to LOW transition on $\overline{CSa}$ or $\overline{CSb}$ and be terminated by a LOW to HIGH transition on $\overline{CSa}$ or $\overline{CSb}$. There is no restriction as to which of the two SPI interface ports receives an instruction or combination of instructions.

If the instruction initiates a nonvolatile write operation, as indicated in Table 1, “Instruction Opcodes,” on page 6 and in the instruction definitions, the write cycle begins at the rising edge of the $\overline{CSa}$ or $\overline{CSb}$ signals. However if the $\overline{CSa}$ or $\overline{CSb}$ goes HIGH before the device address, command, and data are sent completely (e.g. when the clock is not a multiple of eight), then no nonvolatile write cycle starts, the WEL will not reset, and there will be an incomplete transmission (i.e. a failed command). In a failed command, an interrupt signal informs the host processor of a fault condition. After completion of a nonvolatile write cycle, the circuitry automatically clears the Write Enable Latch (WEL).

The nonvolatile write typically takes much less than the maximum time to complete. However, the Status Register WIP bit indicates the nonvolatile wrte status. After receiving a valid address, the X5114 returns the status register contents so an host has an early end of write cycle indication. If WIP is HIGH, the write is still in progress. If WIP is LOW, the X5114 is available for continued operations.

Table 1. Instruction Opcodes

Command	Operation	Opcode (3)	Operation	HV Write Cycle	Bytes(2)
NOP	Memory Access	00h [0000 0000]	No Operation		2+
RML		05h [0000 0101]	Read Memory Low		4+
RMH		06h [0000 0110]	Read Memory High		4+
WML		09h [0000 1001]	Write Memory Low	Y	4+
WMH		0Ah [0000 1010]	Write Memory High	Y	4+
SWEL		03h [0000 0011]	Set Write Enable Latch		2
RWEL		0Ch [0000 1100]	Reset Write Enable Latch		2
RMPR	Read Port	DFh [1101 1111]	Read Multiple Port Registers		16
RPAL		51h [0101 0001]	Read Port A Latch		3
RPBL		91h [1001 0001]	Read Port B Latch		3
RDVRA		52h [0101 0010]	Read Desired Value Register Port A		3
RDVRB		92h [1001 0010]	Read Desired Value Register Port B		3
RDDRA		54h [0101 0100]	Read Data Direction Register Port A		3
RDDRB		94h [1001 0100]	Read Data Direction Register Port B		3
WMPR	Write Port	EFh [1110 1111]	Write Multiple Port Registers	Y	11
WDVRA		62h [0110 0010]	Write Desired Value Register Port A	Y(1)	3
WDVRB		A2h [1010 0010]	Write Desired Value Register Port B	Y(1)	3
WDDRA		64h [0110 0100]	Write Data Direction Register Port A	Y	3
WDDRB		A4h [1010 0100]	Write Data Direction Register Port B	Y	3
RIAE	Read Error Condition	5Ch [0101 1100]	Read IRQA Error Register		3
RIBE		9Ch [1001 1100]	Read IRQB Error Register		3
RFCR		DEh [1101 1110]	Read IRQ Failed Command Register		3
RIAM	Read Configura-tion	58h [0101 1000]	Read IRQ Mask Register Port A		3
RIBM		98h [1001 1000]	Read IRQ Mask Register Port B		3
RICR		D3h [1101 0011]	Read IRQ Configuration Register		3
RPCR		D5h [1101 0101]	Read Port I/O Configuration Register		3
RTBL		D0h [1101 0000]	Read Threshold/Block Lock Register		3
WIAM	Write Configura-tion	68h [0110 1000]	Write IRQ Mask Register Port A	Y	3
WIBM		A8h [1010 1000]	Write IRQ Mask Register Port B	Y	3
WICR		E3h [1110 0011]	Write IRQ Configuration Register	Y	3
WPCR		E5h [1110 0101]	Write Port I/O Configuration Register	Y	3
WTBL		E0h [1110 0000]	Write Threshold/Block Lock Register	Y	3

Notes:

(1) In this condition, the HV Write Cycle will not proceed when the X5114 is configured in the handshake mode.

(2) The number of command bytes listed here is for software addressing mode. For memory sequential read and page write, the minimum number is 4. The minimum number of bytes required for NOP is 2.

(3) All other possible instruction opcodes are illegal commands.

NOP

No Operation

NOP is a special instruction opcode which accesses the device without any operation. It is primarily used in conjunction with the $\overline{CSC}$ output. After a NOP, $\overline{CSC}$ goes LOW and the device goes into standby, ignoring any subsequent data sent on the SI pin and putting the SO pin in a high impedance state. With the NOP instruction, the host processor can communicate with other SPI devices (including other X5114s) in the system without affecting the currently selected device. In this way, an unlimited number of X5114s can reside in a system.

Memory Access Operations

To decode all 512 bytes in the memory array requires a 9-bit address. This would normally require a 2-byte memory address. However, the X5114 uses two different read opcodes (RMH and RML) and two different write opcodes (WMH and WML) to reduce the number of bytes in the command, with the most significant bit of the address incorporated in the instruction opcode. The RMH and WMH Opcodes access the upper half ($100h-$1FFh) of the array while the RML and WML Opcodes access the lower half ($000h-$0FFh).

RML

Read Memory Low

The Read Memory Low instruction reads the data in the lower half of the memory array, from address $000h to $0FFh. After sending the instruction opcode and byte address, the data at the selected address shifts out on the SO line. Continued clocking sequentially shifts out data stored in memory at the next address and automatically increments the address to the next location after each byte of data. When reaching the lower half array boundary ($0FFh), the address counter continues to the first address in the upper half of the memory ($100h). When reaching the upper address boundary ($1FFh), the address counter rolls over to address $000h, allowing the read cycle to be continued indefinitely. The read cycle is terminated by taking $\overline{CSa}$ or $\overline{CSb}$ high.

RMH

Read Memory High

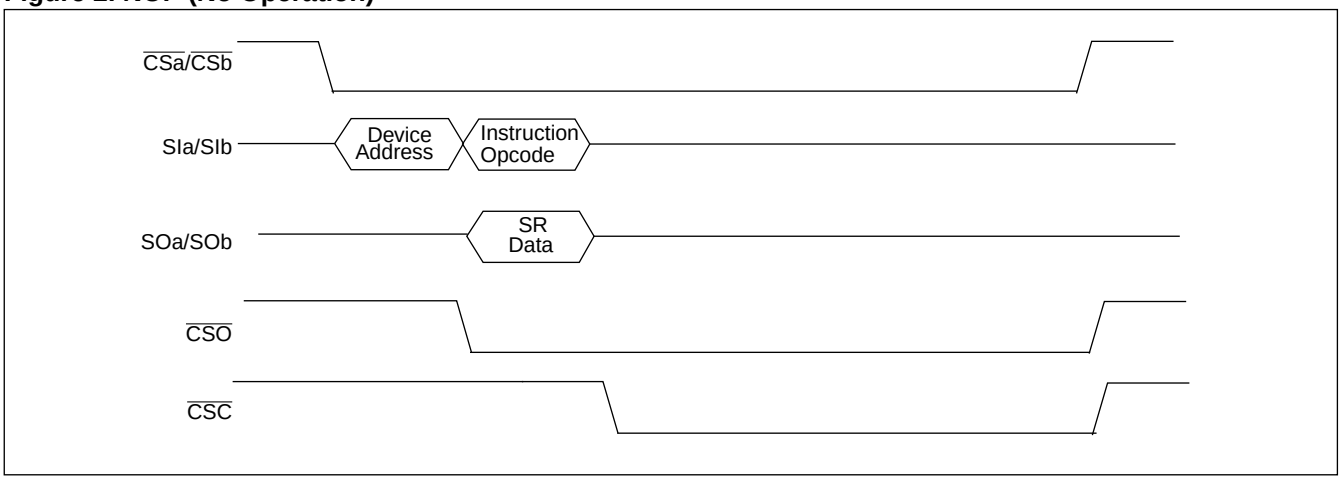
The Read Memory High instruction allows users to read the data in the upper half of the memory array from $100h to $1FFh. Its function is similar to the RML Command.

WML NONVOLATILE

Write Memory Low

The Write Memory Low instruction writes new data to the lower half of the memory array from $000h to $0FFh. Prior to any attempt to write data into the memory array, the Write Enable Latch must first be set by issuing the SWEL instruction. The user may write up to 32 bytes of data to the memory in a single write instruction. The only restriction is that the 32-byte data must reside on the same page, i.e. the upper 3 address bits must be the same for all of the bytes of data to be written. The lowest 5 address bits automatically increment after transmission of each byte. After the lowest 5 address bits reach $11111b, they roll over to $00000b while the 3 higher order address bits remain unchanged. The 32-byte page can be written with data and then over-written indefinitely. In this case, only the last 32 bytes of data transmitted will be written to the EEPROM during the nonvolatile write cycle which follows.

Figure 2. NOP (No Operation)



WMH NONVOLATILE

Write Memory High

The Write Memory High instruction allows users to write new data to the upper half of the memory array from $100h to $1FFh. Its function is similar to Write Memory Low.

SWEL VOLATILE

Set Write Enable Latch

The Set Write Enable Latch instruction sets the Write Enable Latch. This instruction must be completed before any nonvolatile write cycle operation can begin. Setting the WEL is not required prior to a write to a volatile register. Setting the Write Enable Latch sets the WEL flag in the Status Register (SR) to "1". The Write Enable Latch remains set until a Reset WEL instruction, the device powers down, or the completion of a nonvolatile write operation.

RWEL VOLATILE

Reset Write Enable Latch

The Reset Write Enable Latch instruction resets the Write Enable Latch. Resetting the Write Enable Latch resets the WEL flag in the Status Register (SR) to "0". The WEL bit LOW inhibits any nonvolatile memory write operation.

Figure 3. Read Memory (RML or RMH)

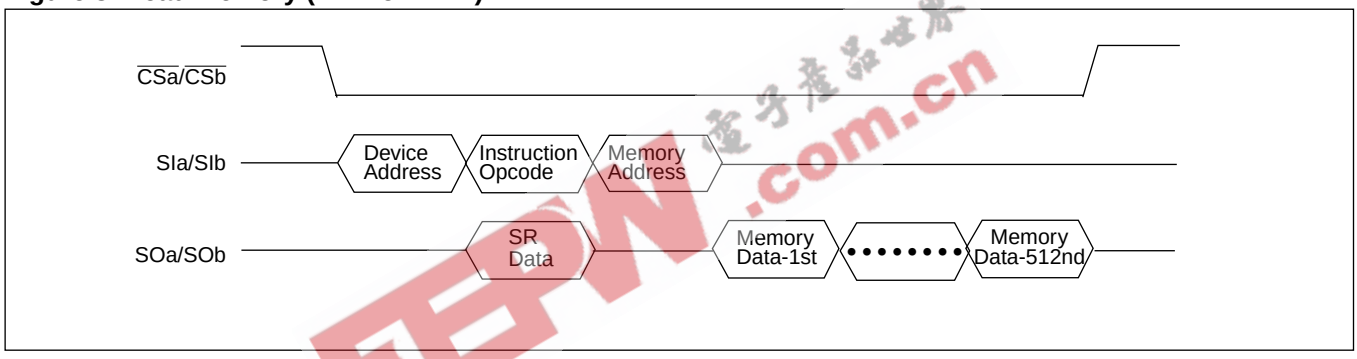


Figure 4. Write Memory (WML or WMH)

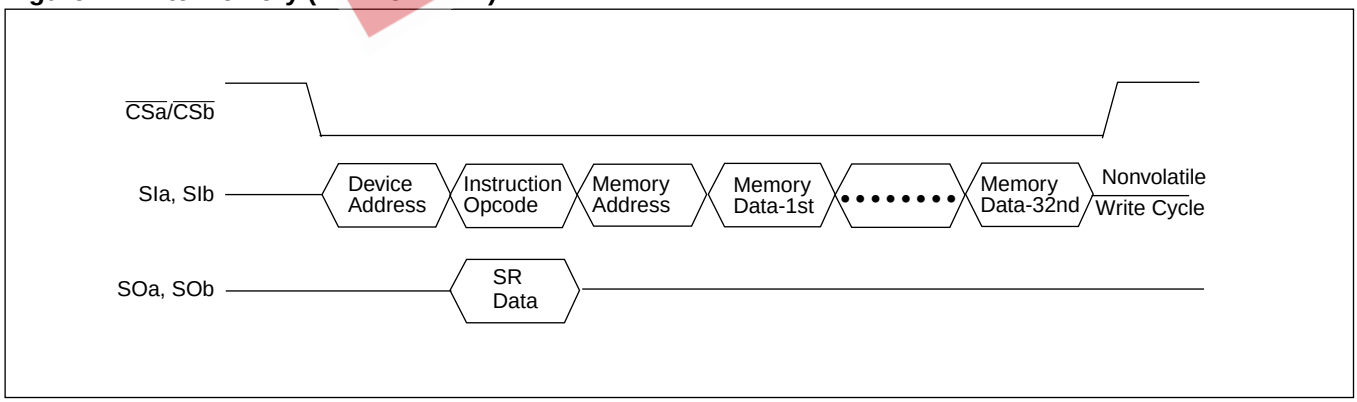
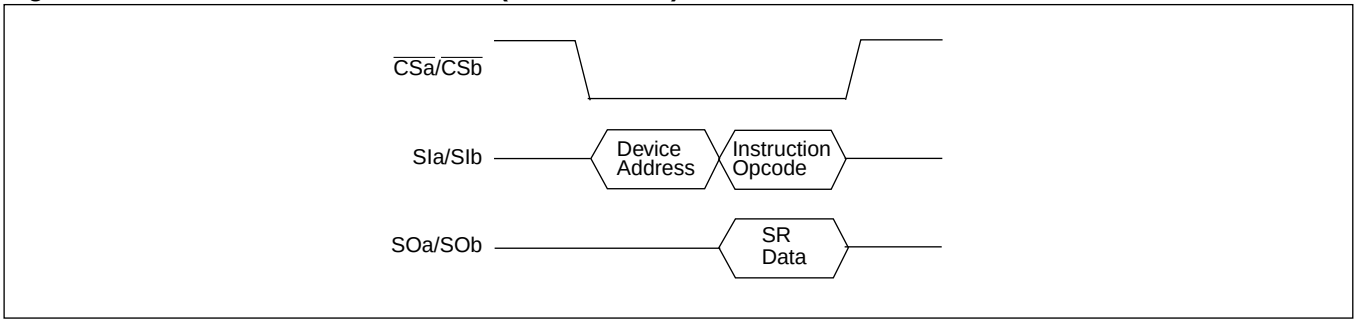


Figure 5. Set/Reset Write Enable Latch (SWEL/RWEL)



Read Port Operations

RMPR

Read Multiple Port Registers

The RMPR Instruction allows the user to read all of the Port-related registers, both volatile and non-volatile. See Figure 6 on page 10. After the sending the instruction opcode on the SIa or SIb line, the host reads data out on the SOa or SOb line in the order as shown in Table 2, “Multiple Register Read Order (RMPR),” on page 9. Maintaining $\overline{CSa}$ or $\overline{CSb}$ LOW and clocking SCKa or SCKb allows continuous reading of the registers. Once the $\overline{CSa}$ or $\overline{CSb}$ goes HIGH, the command terminates.

Table 2. Multiple Register Read Order (RMPR)

Read Order	Register	Description
1	PAL	Port A Latch
2	PBL	Port B Latch
3	DDRA	Data Direction Reg. A
4	DDRB	Data Direction Reg. B
5	IAM	IRQ Mask Register A
6	IBM	IRQ Mask Register B
7	DVRA	Desired Value Register A
8	DVRB	Desired Value Register B
9	IAE	IRQA Error Register
10	IBE	IRQB Error Register
11	PCR	Port I/O Configuration Register
12	CR	Configuration Register
13	ICR	IRQ Configuration Register
14	FCR	IRQ Failed Command Register

RPAL, RPBL

Read Port A, B Latch

The Port A Latch and Port B Latch are read only. The RPAL and RPBL instructions read data from the Port A Latch or Port B Latch.

In the General I/O mode, decoding of the RPAL instruction latches data into the PORT A Latch. The data returned from the Port A Latch provides a “snapshot” of the conditions at the port pins when the RPAL instruction was decoded.

In the handshake mode, the external strobe signal (STRA) latches data into the PORT A Latch. The RPAL instruction triggers the input handshake sequence and reads data from the PORT A Latch.

For Port B, the data is always latched by the decoding of the RPBL instruction.

RDVRA, RDVRB

Read Desired Value Register A, B

The RDVRA and RDVRB instructions read the contents of the respective Desired Value Register (DVRA or DVRB). See Figure 8 on page 10. In the general I/O mode, the contents of DVRA or DVRB relate to fault monitoring. In the handshake mode, the DVRA and DVRB contain the status of the output pins.

RDDRA, RDDRB

Read Data Direction Register A, B

The RDDRA and RDDRB instructions read the current settings of the Data Direction Register. See Figure 8 on page 10.

Write Port Operations

WMPR NONVOLATILE

Write Multiple Port Registers

The WMPR instruction writes to a number of Port-related configuration registers in a single write operation. Figure on page 10. After sending the device address and the instuction opcode, data sent through the SI line will be written successively to the registers. The data must be written to the device in order, as shown in Table 3, “Multiple Register Write Order (WMPR),” on page 11. After the completing the sequence of data, a nonvolatile write cycle begins after the $\overline{CSa}$ or $\overline{CSb}$ goes HIGH.

Figure 6. Read Multiple Port Registers (RMPR)

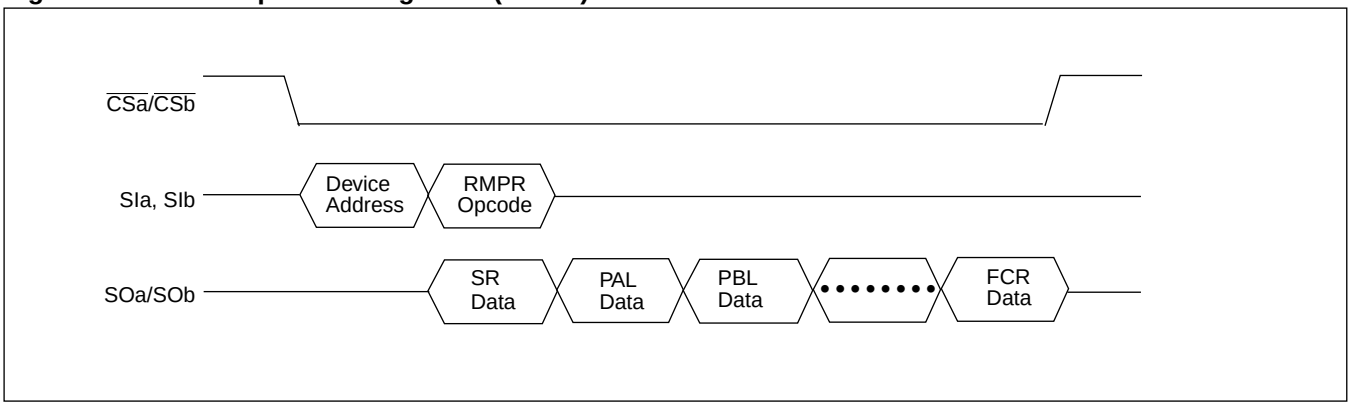


Figure 7. Write Multiple Port Registers (WMPR)

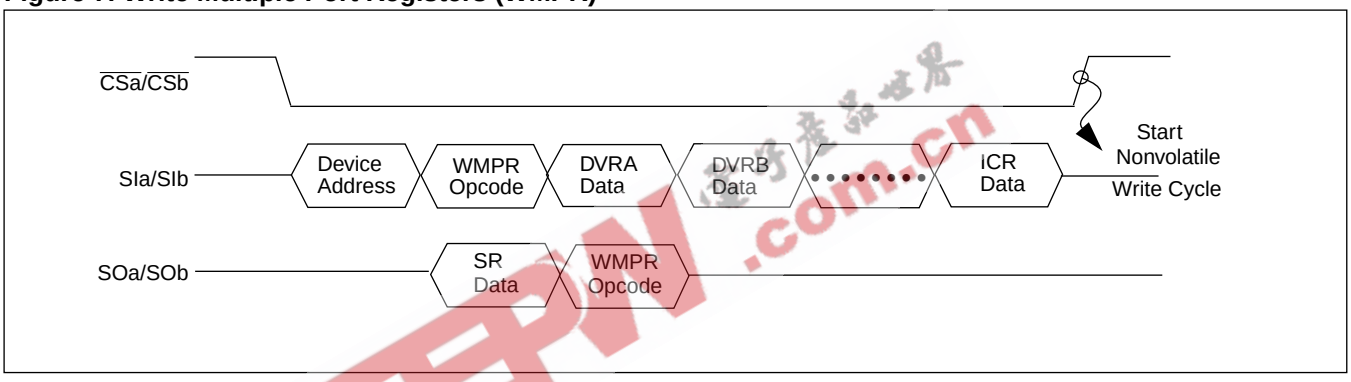


Figure 8. Read Register - Single

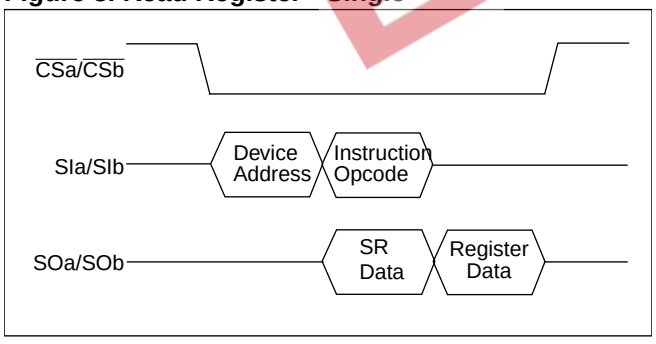


Figure 9. Write Register - Single

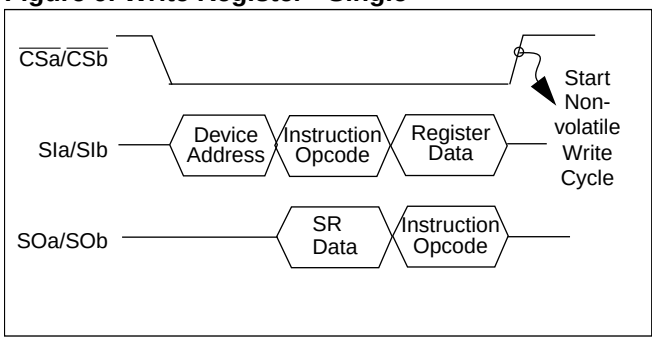


Table 3. Multiple Register Write Order (WMPR)

Write Order	Register	Description
1	DVRA	Desired Value Reg. A
2	DVRB	Desired Value Reg. B
3	DDRA	Data Direction Reg. A
4	DDRB	Data Direction Reg. B
5	IAM	IRQ Mask Register A
6	IBM	IRQ Mask Register B
7	PCR	Port I/O Configuration Register
8	CR	Configuration Register
9	ICR	IRQ Configuration Register

WDVRA, WDVRB NONVOLATILE

Write Desired Value Register A, B

The WDVRA and WDVRB instructions write data to the Desired Value Registers. See Figure 9 on page 10.

In the general I/O mode, these instructions load the Desired Value Registers with desired data to monitor the input/output pin level (Fault Monitoring). This data value compares with the signal on the corresponding input port pins. Any differences can generate an interrupt. Taking $\overline{CSa}$ or $\overline{CSb}$ HIGH following the WDVRA or WDVRB instruction starts a nonvolatile write cycle that mirrors the data into a nonvolatile location. Power cycling the device restores the nonvolatile value to the DVRA and DVRB registers.

In the handshake mode, the WDVRA instruction writes data directly to the Port A output pins (i.e., no nonvolatile write cycle) and triggers an output handshake sequence. The WDVRB instruction writes data directly to the Port B output pins 3-0 (pins 7-4 are not available since they are part of the handshake mechanism). Data on Port B pins 3-0 are mirrored into a nonvolatile location by a nonvolatile write cycle.

WDDRA, WDDRB NONVOLATILE

Write Data Direction Register A, B

The WDDRA and WDDRB instructions write new data to the Data Direction Registers. See Figure 9 on page 10. This selects the direction of each of the port pins.

Read Error Conditions

RIAE, RIBE

Read IRQA, IRQB Error Register

The RIAE and RIBE instructions return the contents of the IRQ Error Registers. See Figure 8 on page 10. This provides status on port error conditions.

RFCR

Read Failed Command Register

The Read Failed Command Register instruction allows the host to track the most recent bad command. A bad command is defined as one with:

- an unknown or illegal instruction opcode
- an incomplete transmission of a command which can be instruction opcode, address, or data. As an example, $\overline{CSa}$ or $\overline{CSb}$ goes HIGH when the clock count is not a multiple of 8.

Detection of a bad command sets a Failed Command (FC) flag in the Status Register (SR) and asserts the IRQA or IRQB signal, if enabled. The Failed Command Register contains the Error information. The host read of the Failed Command Register clears $\overline{IRQA}$ and $\overline{IRQB}$ signals and the FC flag. However, the RFCR instruction will not clear the Failed Command Register.

The FCR will only store the most recent bad command if there were more than one bad command in a sequence. Also the information in the FCR is only updated when a bad command is discovered.

Read Configuration

RIAM, RIBM

Read IRQA, IRQB Mask Register

The RIAM and RIBM instructions return the contents of the respective IRQ Mask Register. See Figure 8 on page 10.

RICR

Read IRQ Configuration Register

The RICR instruction returns the contents of the IRQ Configuration Register. See Figure 8 on page 10.

RPCR

Read Port I/O Configuration Register

The RPCR instruction returns the contents of the PORT I/O Configuration Register. See Figure 8 on page 10.

RTBL

Read Threshold/Block Lock Register
The RTBL instruction returns the contents of the Threshold/Block Lock Register. See Figure 8 on page 10.

Write Configuration

WIAM, WIBM NONVOLATILE

Write IRQA, IRQB Mask Register
The WIAM and WIBM instructions write new data to the respective IRQ Mask Register. See Figure 9 on page 10.

WICR NONVOLATILE

Write IRQ Configuration Register
The WICR instruction writes new data into the IRQ Configuration Register to change interrupt operations. See Figure 9 on page 10.

WPCR NONVOLATILE

Write Port I/O Configuration Register
The WPCR instruction writes new data into the Port I/O Configuration Register to change the Port I/O functionality. See Figure 9 on page 10.

WTBL NONVOLATILE

Write Threshold/Block Lock Register
The WTBL instruction writes new data to the Threshold/Block Lock Register to select different modes of operations. See Figure 9 on page 10.

CONTROL/STATUS REGISTERS

The X5114 has a number of registers to monitor and control the operation of the device. Access to the control registers are via SPI Commands.

The status register contains the status of the most critical operating conditions. The contents are placed on the output pins in synchronization with the incoming op code (providing the device is addressed correctly). The status register cannot be written to directly.

Status Register (SR)

WIP	WEL	PCE	FC	RDR	XRE	IRQA	IRQB
Volatile							

MSB LSB

WIP	**Write In Progress flag.**
0	no nonvolatile write cycle in progress
1	nonvolatile write cycle is in progress
WEL	**Write Enable Latch flag**
0	write enable latch has not been set
1	write enable latch is set
PCE	**PCE Pin Input Status**
0	PCE pin is at Logic 0
1	PCE pin is at Logic 1
FC	**Failed Command flag—Power on default = 1**
0	no command failures
1	command failure (abnormal termination)
RDR	**Receive Data Ready flag** (Single Read Input and Bidirectional Modes)
0	no data is latched
1	latched data is ready for read at Port A
XRE	**Transmit Register Empty flag** (Output and Bidirectional Modes)
0	Port A data has not been read by the external system and is not ready to accept new data from the SPI interface
1	Port A is ready to accept the new data from the SPI interface.
IRQA	**Interrupt Port A**
0	Interrupt A is not asserted
1	Interrupt A is asserted
IRQB	**Interrupt Port B**
0	Interrupt B is not asserted
1	Interrupt B is asserted

Threshold/Block Lock Register (TBL).

TU2	TU1	TU0	TL2	TL1	TL0	AIN	BL
Nonvolatile							

MSB LSB

TU2, TU1, TU0 Input Threshold level upper bits

These bits store the desired input threshold level for the analog mode of pins PA7 to PA4

TL2, TL1, TL0 Input Threshold level lower bits

These bits store the desired input threshold level for the analog mode of pins PA3 to PA0

ADS Analog/Digital Mode Select Bit

0	digital mode
1	analog mode

BL Block Lock Configuration

0	no memory block locked
1	address $000h to $1FFh locked (writes prohibited)

Port Desired Value Register (DVRA and DVRB)

DVR A7	DVR A6	DVR A5	DVR A4	DVR A3	DVR A2	DVR A1	DVR A0
General I/O = Nonvolatile, Handshake = Volatile							

MSB LSB

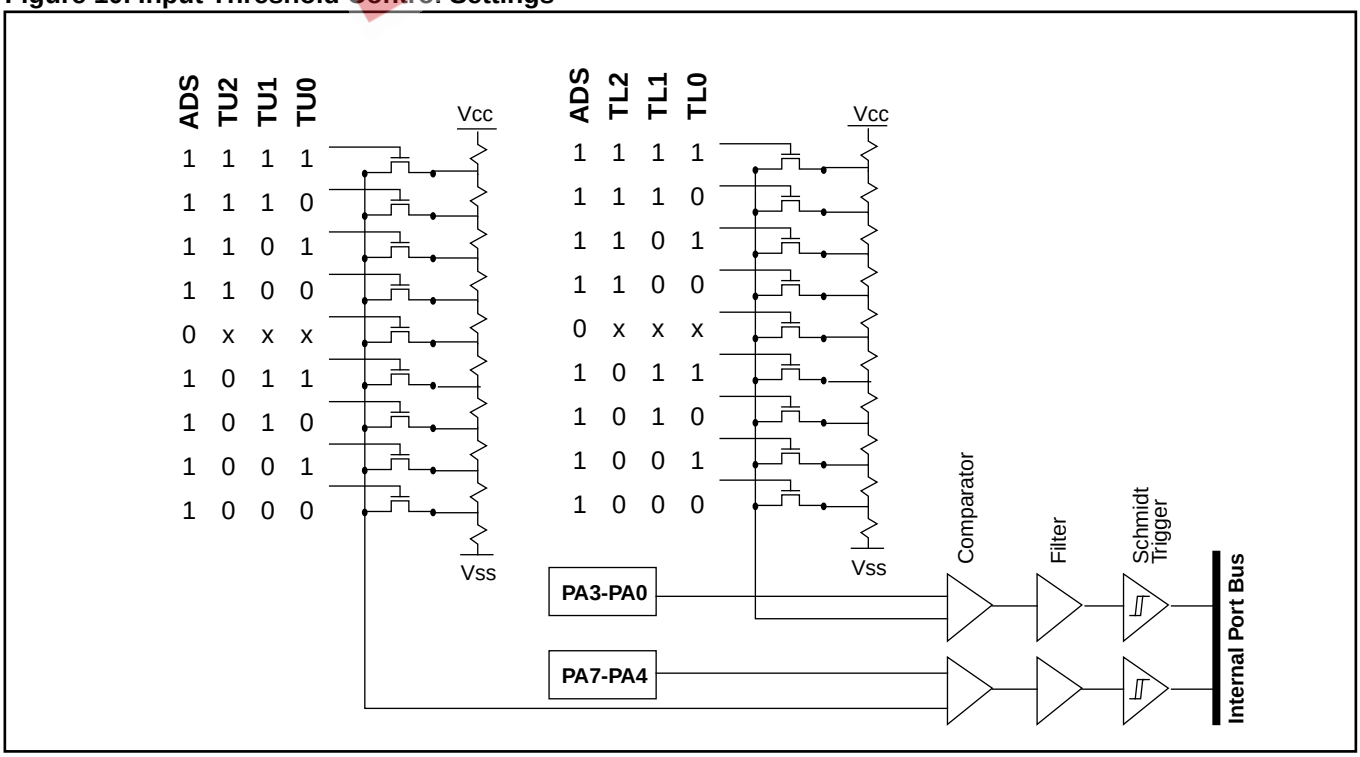
DVR B7	DVR B6	DVR B5	DVR B4	DVR B3	DVR B2	DVR B1	DVR B0
General I/O = Nonvolatile, Handshake = Volatile				Nonvolatile			

MSB LSB

The DVRA register has two functions. In the general I/O mode, DVRA is nonvolatile and stores the desired output data or the desired value for I/O monitoring. Writes to DVRA in this mode generate a nonvolatile write cycle. In the handshake mode, DVRA is volatile and there is no nonvolatile write.

The DVRB Register bit3 to bit0 are always nonvolatile regardless of the mode. DVRB7 to DVRB4 are nonvolatile in the general I/O mode and store the Port B output data or the desired value for I/O monitoring. DVRB7 to DVRB4 are volatile in the handshake mode .

Figure 10. Input Threshold Control Settings



Port I/O Configuration Register (PCR)

TRI	CEM	HS2	HS1	HS0	PLS	EGA	INVB
Nonvolatile							

MSB LSB

TRI Port tri-state configuration
(Output Mode only)

0 disables tri-state operation

1 enables tri-state operation

CEM Port Chip Enable Mode Configuration

0 PCE pin LOW disables $\overline{IRQA}$ and $\overline{IRQB}$,

1 PCE pin LOW disables $\overline{IRQA}$ and $\overline{IRQB}$ and tri-states all port outputs (regardless of the content of the DDR)

HS2, HS1, HS0 General/Handshake Mode configuration

0xx general I/O mode

100 Multiple Read Input Mode
(multiple read of the Port A Latch)

101 Single Read Input mode
(single read of the Port A Latch)

110 Output Mode

111 Bidirectional Mode

PLS Handshake Pulse/Interlocked Mode config.

0 interlocked handshake mode

1 pulse handshake mode

EGA Handshake strobe (STRA) active edge

0 falling edge active

1 rising edge active

INVB Handshake ready (STRB, TDRE, RDRF) active level

0 Logic '0' is the active level

1 Logic '1' is the active level

Port Latch (PAL and PBL)

PAL7	PAL6	PAL5	PAL4	PAL3	PAL2	PAL1	PAL0
Volatile							

MSB LSB

PBL7	PBL6	PBL5	PBL4	PBL3	PBL2	PBL1	PBL0
Volatile							

MSB LSB

Port Latches are read-only input registers. In the general I/O mode, decoding the SPI opcode latches data into the PORT A Latch. In the handshake mode, sensing the STRA input latches input data into the PORT A Latch.

Decoding the SPI opcode always latches data into the PORT B Latch, regardless of the I/O mode.

Port Data Direction Register (DDRA and DDRB)

DDR A7	DDR A6	DDR A5	DDR A4	DDR A3	DDR A2	DDR A1	DDR A0
Nonvolatile							

MSB LSB

DDR B7	DDR B6	DDR B5	DDR B4	DDR B3	DDR B2	DDR B1	DDR B0
Nonvolatile							

MSB LSB

DDRA7-DDRA0 Port A Data Direction Register

0 Port I/O in an input

1 Port I/O is an output

DDRB7-DDRB0 Port B Data Direction Register

0 Port I/O in an input

1 Port I/O is an output

During Handshake modes, all of DDRA and the upper half of DDRB (DDRB7-DDRB4) are ignored.

IRQ Mask Register (IAM and IBM)

IAM7	IAM6	IAM5	IAM4	IAM3	IAM2	IAM1	IAM0
Nonvolatile							

MSB LSB

IBM7	IBM6	IBM5	IBM4	IBM3	IBM2	IBM1	IBM0
Nonvolatile							

MSB LSB

IAM7-IAM0 Port A Interrupt Mask

0 Enables the Input/Output Error - Fault Monitoring on the corresponding Port A I/O pin

1 Disables the Input/Output Error - Fault Monitoring on the corresponding Port A I/O pin.

IBM7-IBM0 Port B Interrupt Mask

0 Enables the Input/Output Error - Fault Monitoring on the corresponding Port B I/O pin

1 Disables the Input/Output Error - Fault Monitoring on the corresponding Port B I/O pin.

IRQ Error Register (IAE and IBE)

IAE7	IAE6	IAE5	IAE4	IAE3	IAE2	IAE1	IAE0
Volatile (Read only)							

MSB LSB

IBE7	IBE6	IBE5	IBE4	IBE3	IBE2	IBE1	IBE0
Volatile (Read only)							

MSB LSB

IAE7–IAE0 Interrupt A Error Flags

0 no, the Port A I/O has no error (Fault Monitoring)

1 yes, the Port A I/O has an error (Fault Monitoring)

IBE7–IBE0 Interrupt B Error Flags

0 no, the Port B I/O has no error (Fault Monitoring)

1 yes, the Port B I/O has an error (Fault Monitoring)

IRQ Configuration Register (ICR)

0	ORAB	ENFC	ERDR	EXRE	EIOE	ENA	ENB
Fixed	Nonvolatile						

MSB LSB

ORAB $\overline{IRQA}$/$\overline{IRQB}$ Routing

0 $\overline{IRQA}$ and $\overline{IRQB}$ individually represent Port A and Port B interrupt status and are not ORed together

1 $\overline{IRQA}$ and $\overline{IRQB}$ provide redundancy and are ORed together

ENFC Failed Command Interrupt configuration

0 disables interrupt generated by Failed Command

1 enables interrupt generated by Failed Command

ERDR Receive Data Ready interrupt configuration

0 disables $\overline{IRQA}$ generated by the RDR flag

1 enables $\overline{IRQA}$ generated by the RDR flag.

EXRE XRE interrupt configuration

0 disables $\overline{IRQA}$ generated by XRE flag

1 enables $\overline{IRQA}$ generated by XRE flag

EIOE Input/Output Error interrupt configuration

0 disables interrupt generated by Input/Output Error

1 enables interrupt generated by Input/Output Error

ENA $\overline{IRQA}$ output configuration

0 disables $\overline{IRQA}$ interrupt output

1 enables $\overline{IRQA}$ interrupt output

ENB $\overline{IRQB}$ output configuration

0 disables $\overline{IRQB}$ interrupt output

1 enables $\overline{IRQB}$ interrupt output

Failed Command Register (FCR)

FCR7	FCR6	FCR5	FCR4	FCR3	FCR2	FCR1	FCR0
Volatile							

MSB LSB

The Failed Command Register (FCR) contains an $FFh if the bad command is unknown or is an incomplete transmission of an opcode. The FCR contains the corresponding instruction opcode, following an incomplete transmission of the address or data.

PORT I/O OPERATION

The X5114 has a total of 16 I/O pins equally divided between Ports A and B. The functionality of the pins is established by several non-volatile configuration registers.

The I/O Ports can be configured as General I/O or as one of four Handshake Configurations.

Configured as general I/O, each of the pins of Port A and Port B can be set as either an input or output via bits in a nonvolatile Data Direction Register. In each of the four handshake modes below, Port A provides an 8-bit parallel data transfer with one, two or four of Port B's pins used for handshake signals (depending upon the operational mode). Port B pins not used for handshake are always used as general I/O.

General I/O

Ports A and B each consist of eight bidirectional pins independently configured by a corresponding bit in a non-volatile Data Direction Register (DDRA/DDRB). The internal interface to Ports A and B consist of two independent registers, the Desired Value Register (DVRA/DVRB) and the Port Latch (PAL/PBL). The DVRA/DVRB registers consist of a volatile and a nonvolatile part.

Port fault management logic allows each I/O the ability to generate an interrupt condition. A mismatch between the value at the pin and the Desired Value for that pin generates a fault condition and sets a flag. The flag triggers an output $\overline{IRQA}$ or $\overline{IRQB}$ signal when allowed to by the EIOE and ENA/ENB bits in the IRQ Configuration Register and by the PCE (Port Chip Enable) pin.

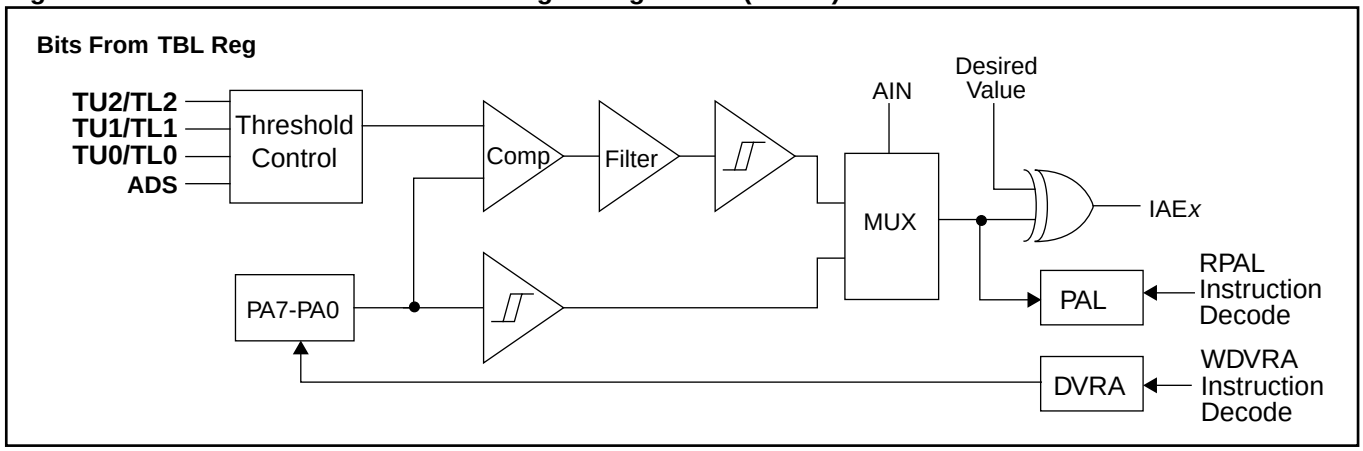
The PCE pin can be configured so a LOW PCE disables the output of interrupts. Or it will disable the output of interrupts and force all port pins to a high impedance state.

Port A and Port B pins configured as outputs power up with a preset state. This is valuable if control of peripherals is necessary before the host processor has initialized after a power failure. Data written through the SPI serial port to the DVRA or DVRB registers is latched into both the volatile and nonvolatile parts of the register. Upon a power up condition, the volatile part of the Desired Value Register is restored by the contents of the nonvolatile part and this restored data appears at the output. At the same time, data is readable with the Read Port instruction and the pin can generate an interrupt if the output does not match the value in the desired value register (for example, if the pin is shorted to ground and a HIGH signal is expected).

THRESHOLD CONTROL

Port A input pins can also be configured with an 10 level analog threshold. The digital reference value was found in the Desired Value Register with the compare threshold set at V_{CC}*0.5 by ADS bit LOW. Three nonvolatile bits in the TBL and ADS HIGH select an analog reference level

Figure 11. General I/O and Fault Monitoring Configuration (Port A)



for each port. If an input signal exceeds the analog threshold, a HIGH is detected. This input compares with the desired value register contents. A mismatch of the two values generates a fault condition, sets a flag and generates an interrupt as described for digital fault monitoring. Reading data in from the port A pins latches data into the PAL register.

Handshake I/O subsystem

The handshake I/O subsystem involves all of Port A and up to four Port B pins. The four primary modes of operation for the handshake I/O subsystem are:

- Single Read Input
- Multiple Read Input
- Output
- Bi-directional

The handshake I/O subsystem efficiently supports high speed data transfers between an external system and a controlling master through the SPI ports of the X5114. These four handshake modes support a variety of 8-bit parallel data applications, such as interfacing to a simple 8-bit latch, an A/D converter or a microcontroller. The 8-bit parallel data path uses Port A, with the handshake I/O signals interfacing to Port B.

For applications which do not require high speed 8-bit parallel data transfer, the handshake functions can generally be ignored. When handshake functions are used, the remaining Port B pins serve as general I/O without interfering with the handshake functions.

Table 4 on page 17 shows the different functions of port B pins for different port I/O handshake modes.

Table 4. Special Port B Pins in Handshake Modes

Handshake Mode	Mode Entry HS2 HS1 HS0	Port B Pin	Pin Function	Data Direction	Configure Signal Polarity
Read Input	1 0 1	PB7	STRA	IN	EGA bit (PCR reg)
		PB6	TDRE	OUT	INVB bit (PCR reg)
		PB5/PB4	X	X	X
Multiple Read Input	1 0 0	PB6	STRB	OUT	INVB
		PB7/PB5/PB4	X	X	X
Output	1 1 0	PB7	STRA	IN	EGA
		PB5	RDRF	OUT	INVB
		PB6/PB4	X	X	X
Bi-directional	1 1 1	PB7	R/$\overline{W}$	IN	none
		PB6	TDRE	OUT	INVB
		PB5	RDRF	OUT	INVB
		PB4	PEN	IN	none

Single Read Input Mode

EXAMPLE APPLICATION:

A local slave controller identifies a condition that requires action and initiates a sequence by sending a command byte to the X5114 through the parallel port. A Strobe signal from the slave controller latches in the data and generates an interrupt to a remote, host system. The host reads the data on the SPI lines and takes appropriate action. Reading the data automatically frees the port for the next input byte.

MODE ENTRY:

Set **HS2, HS1, HS0** bits in PCR register to 101

SIGNALS:

- **Port A** is the high speed input data port.
- **STRA** (PB7) is the stobe input. An external device uses this signal to write new data into the Port A Latch. The EGA bit selects which edge of the STRA input will register the input data.
- **TDRE** (PB6) is the ready output signal. This signal notifies the external device that new data can be written. Reading the port data via the SPI port automatically resets the TDRE signal. The invert bit (INVB) sets the active level of the TDRE output signal.
- **RDR** Flag - The STRA signal sets the RDR flag in the Status register. Once set, the RDR flag automatically inhibits further writes into PORT A from the external

Figure 12. Single Read Input Mode - Parallel Write

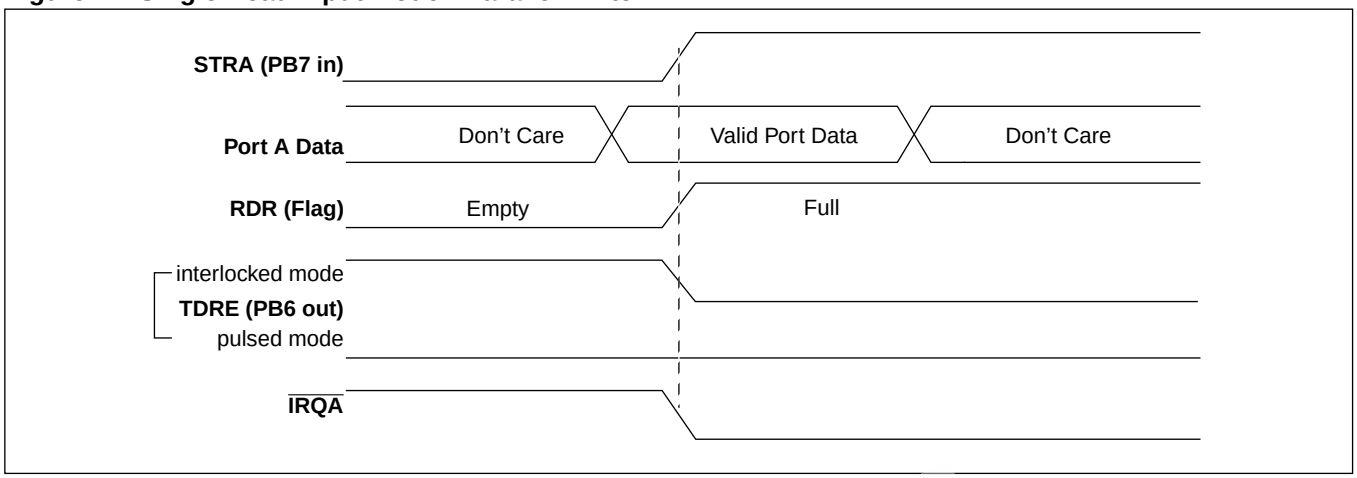
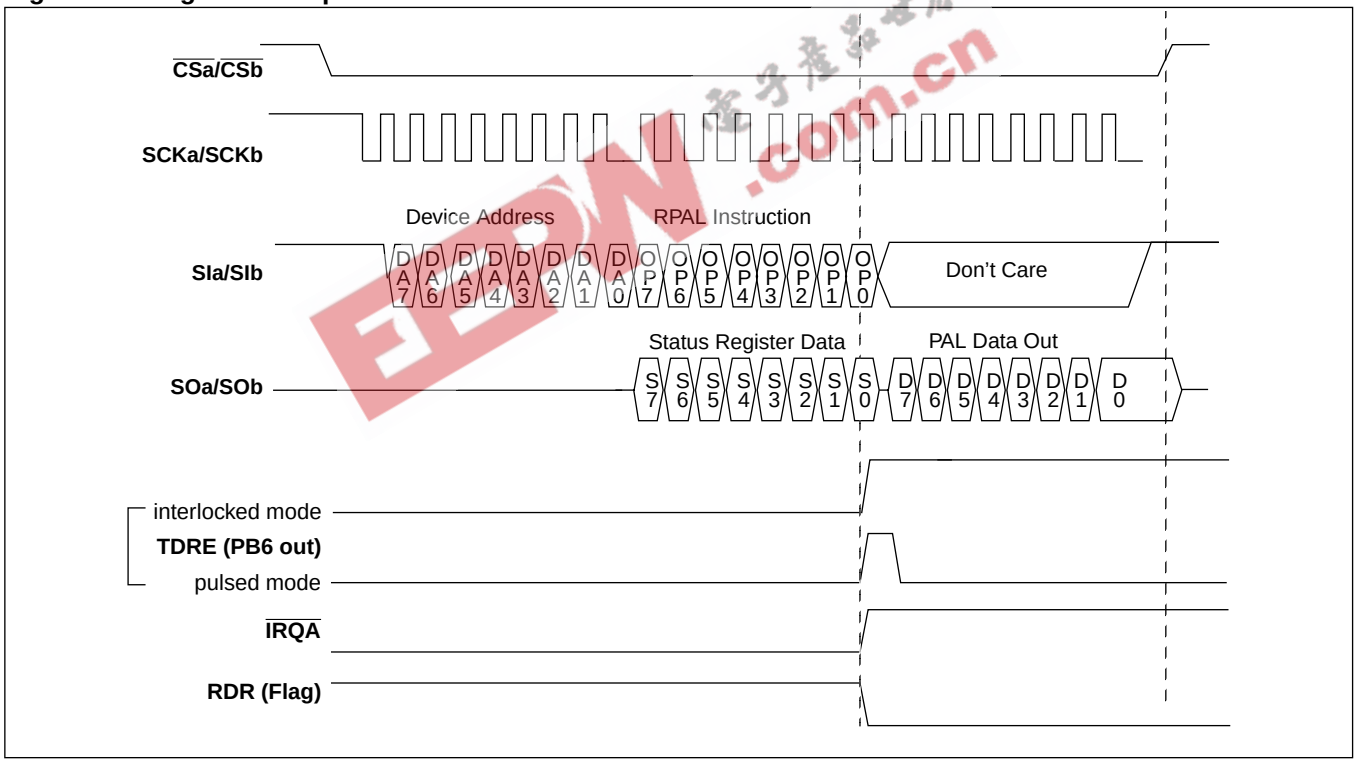


Figure 13. Single Read Input Mode - SPI Read

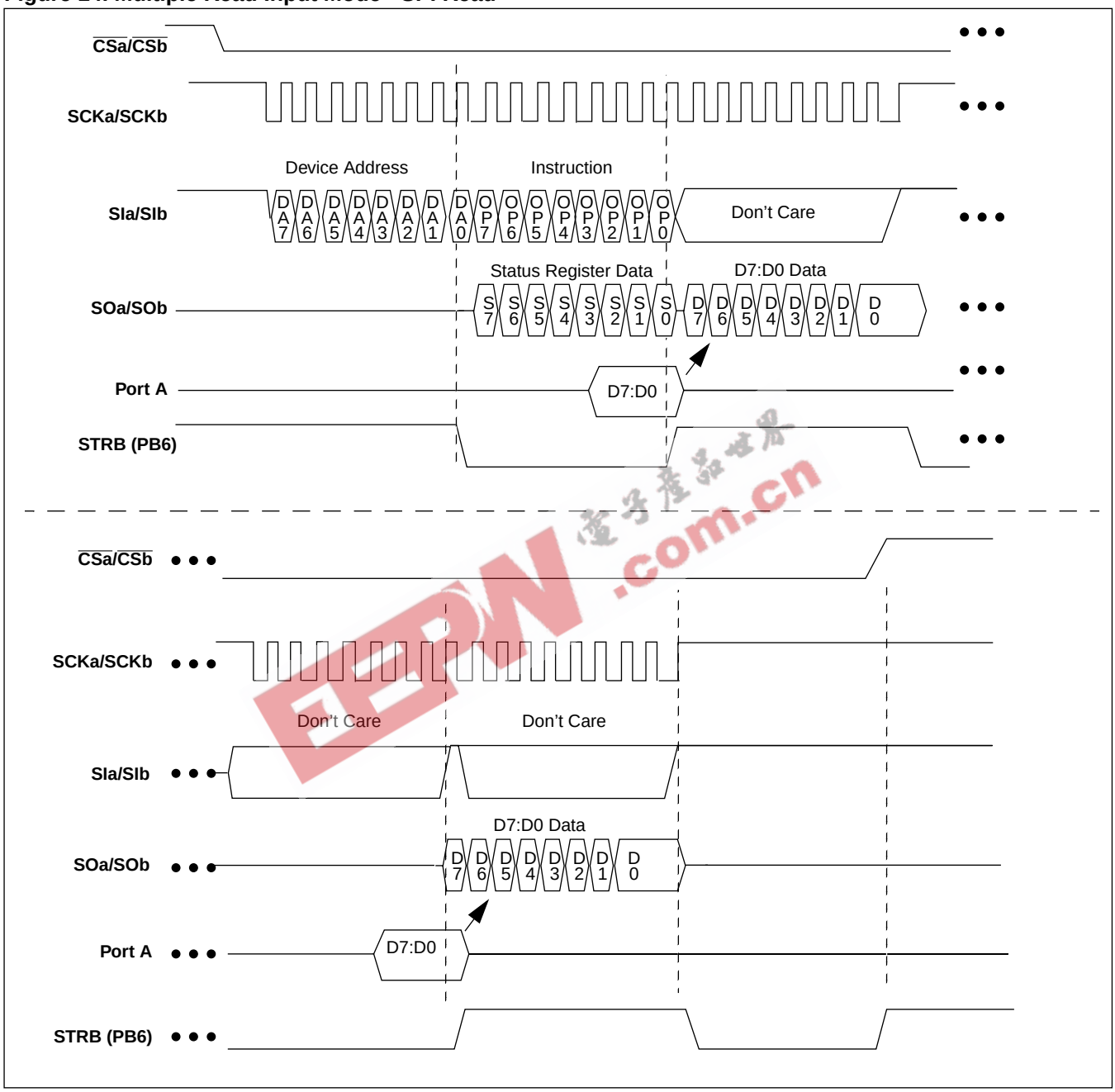


device. The host system should not attempt to write to the Port A Latch. The host processor can poll RDR through the SPI port or RDR can generate an external interrupt. The ERDR bit enables the RDR interrupt.

- **PLS** bit - The pulse bit (PLS) HIGH sets the TDRE signal to operate in an "interlocked" mode, where TDRE "tracks" the RDR flag. The PLS bit LOW sets the handshake to operate in a "pulsed" mode.

Fault monitoring on pins PA7-PA0 and PB7-PB6 is disabled in this mode. Fault monitoring and general I/O functionality of the remaining six Port B pins remains user configurable.

Figure 14. Multiple Read Input Mode - SPI Read



Multiple Read Input Mode

EXAMPLE APPLICATION:

An A/D converter connects to the X5114 parallel port. The host reads the A/D converter data through the SPI port. Reading the data automatically generates a STRB output signal that initiates a new A/D conversion cycle.

MODE ENTRY:

Set **HS2, HS1, HS0** bits in PCR register to 100

SIGNALS:

- **Port A** is the high speed input data port.
- **STRB** (PB6) is the strobe output. The invert bit (INVB) sets the active level of STRB in the multiple read mode. Reading Port A data through the SPI port automatically

Figure 15. Output Mode - SPI Write

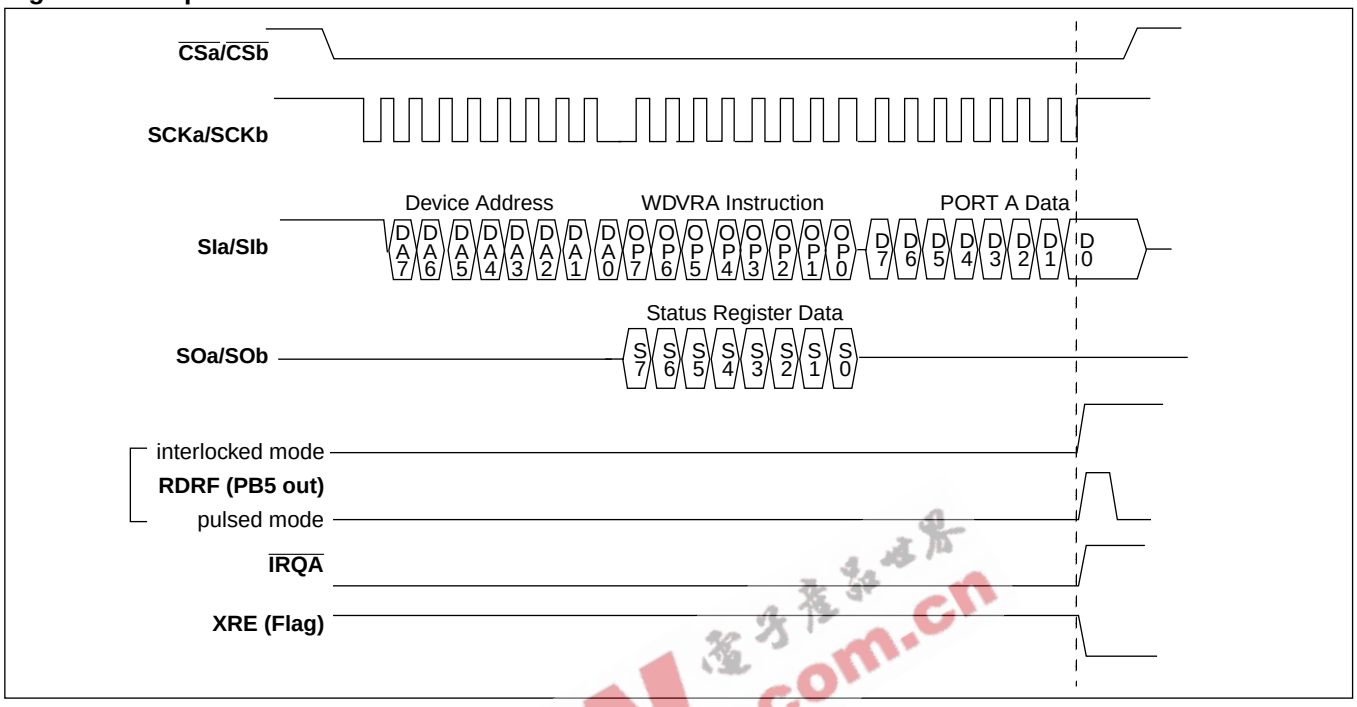
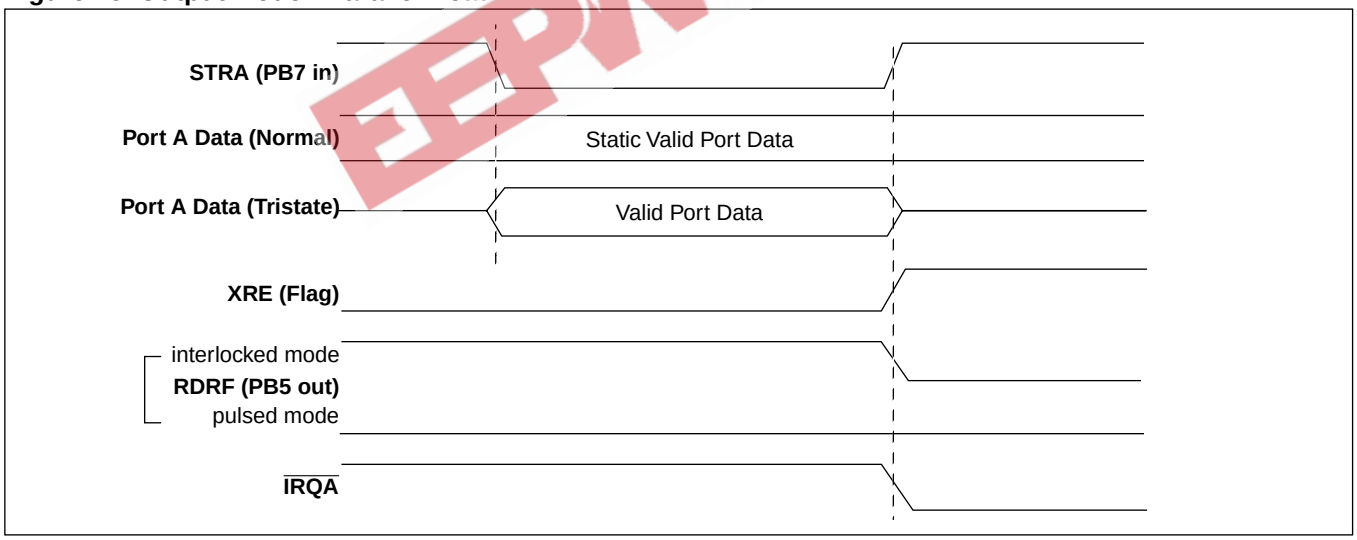


Figure 16. Output Mode - Parallel Read



generates STRB. This mode gives the X5114 the capability of performing multiple data reads while the SPI select line, $\overline{CSa}$ or $\overline{CSb}$ remains asserted and SCK clocks data through the SPI port.

Output Mode

EXAMPLE APPLICATION:

The host processor initiates a data byte transfer through the SPI and Port A to a slave processor. The slave then executes the command. This mechanism allows numerous remote processors to reside on the same SPI three wire bus to reduce interface complexity. In this case, the remote processor does not need an SPI port, but communicates via a parallel I/O.

MODE ENTRY:

Set **HS2, HS1, HS0** bits in PCR register to 110

SIGNALS:

- **Port A** - Parallel data is sent out through this port.
- **DVRA** Register - The host writes data through the SPI port to this register. In this case, DVRA data is not mirrored into non-volatile memory as in the general I/O mode.
- **RDRF** (PB6) is the output strobe signal. This signal notifies the external device that new data was written to the DVRA. The invert bit (INVB) sets the active level of the RDRF output signal.
- **STRA** (PB7) is the strobe input. An external device uses this signal to inform the host that data has been read from Port A and that new data can be written. The user selects the active edge of the STRA input with the EGA bit.
- **XRE** Flag - The STRA signal sets the XRE flag in the Status register. The host processor can poll XRE through the SPI port or XRE can generate an external interrupt. The EXRE bit in the ICR register enables the XRE interrupt.

Figure 17. Bi-directional Mode - SPI Write

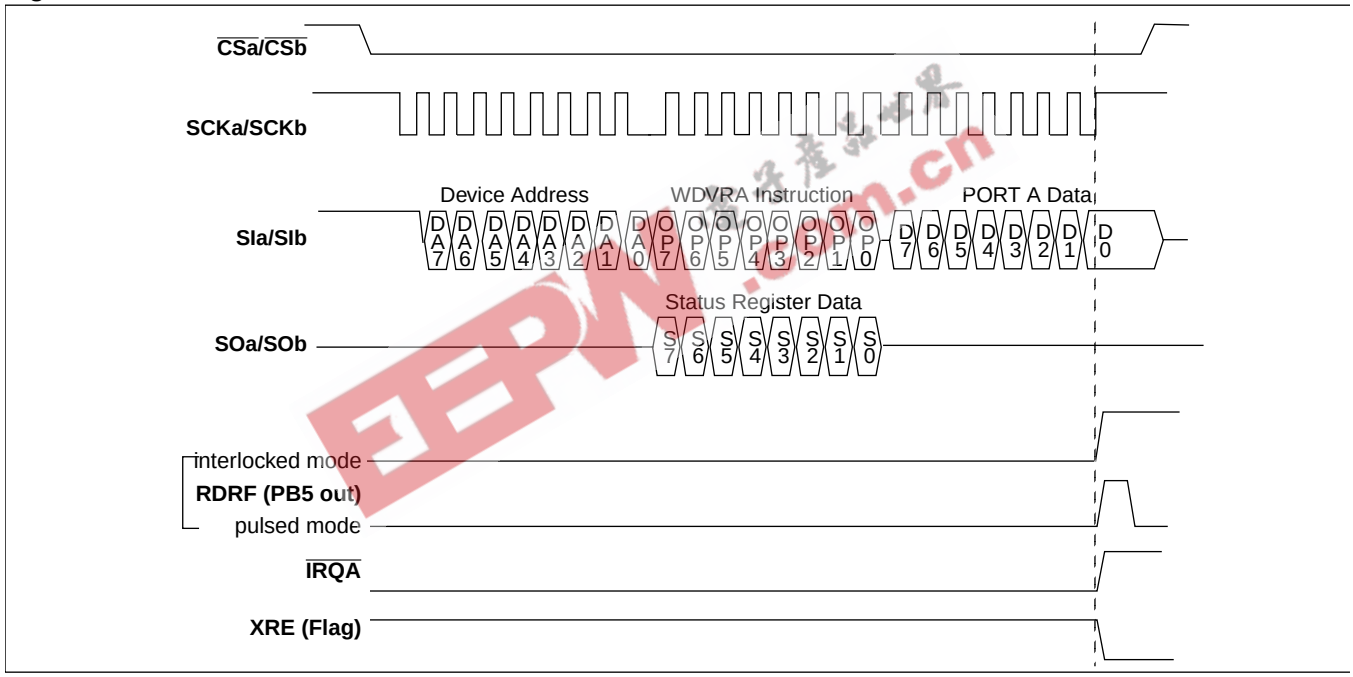


Figure 18. Bi-directional Mode - Parallel Read

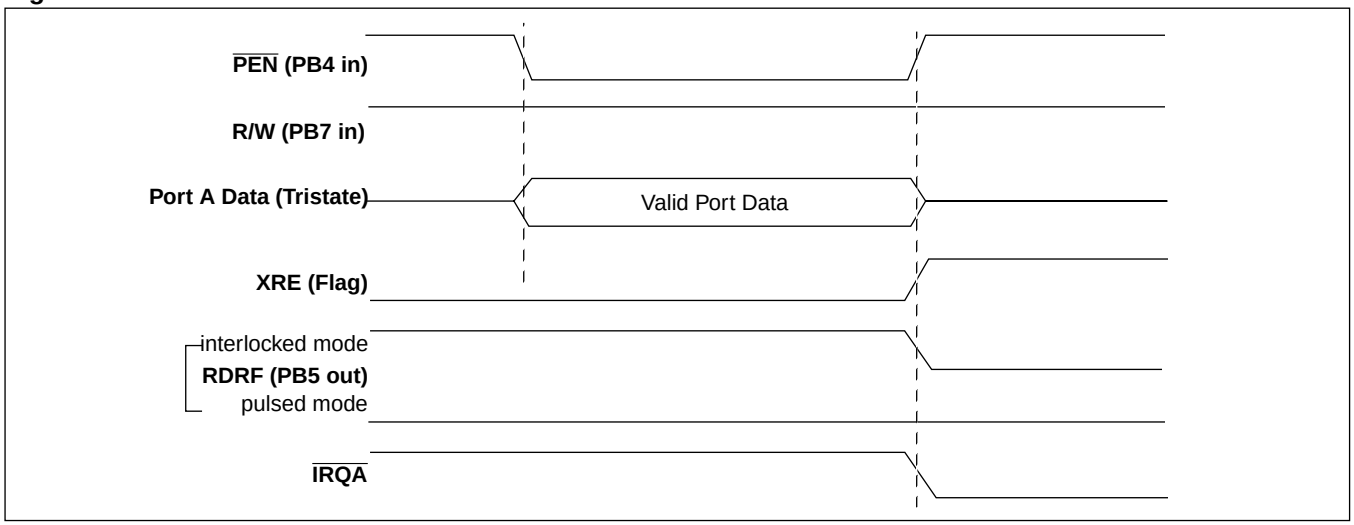


Figure 19. Bi-directional Mode - Parallel Write

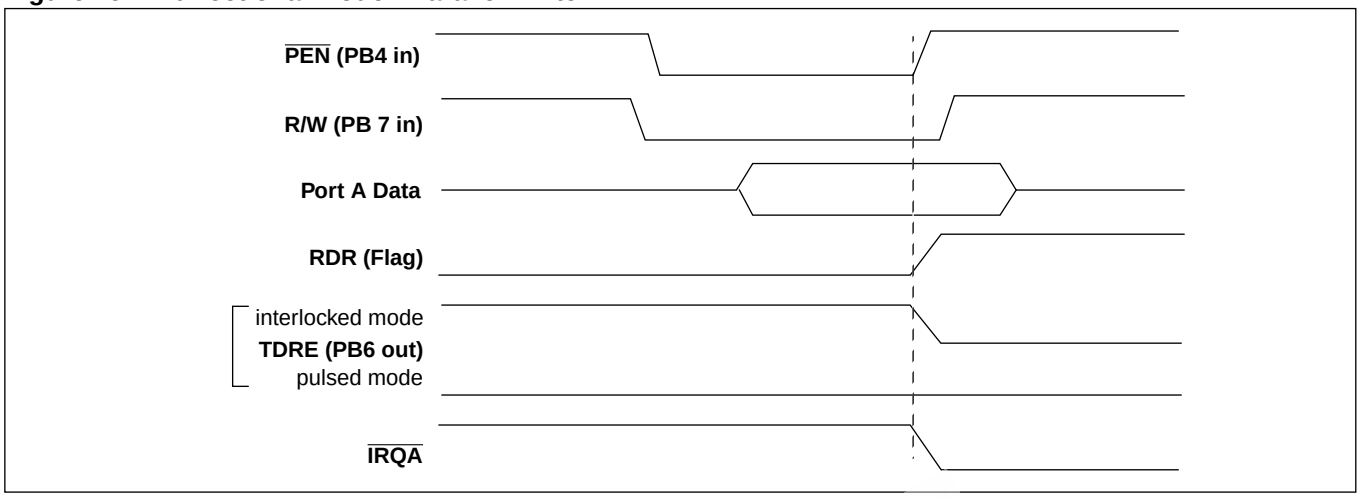
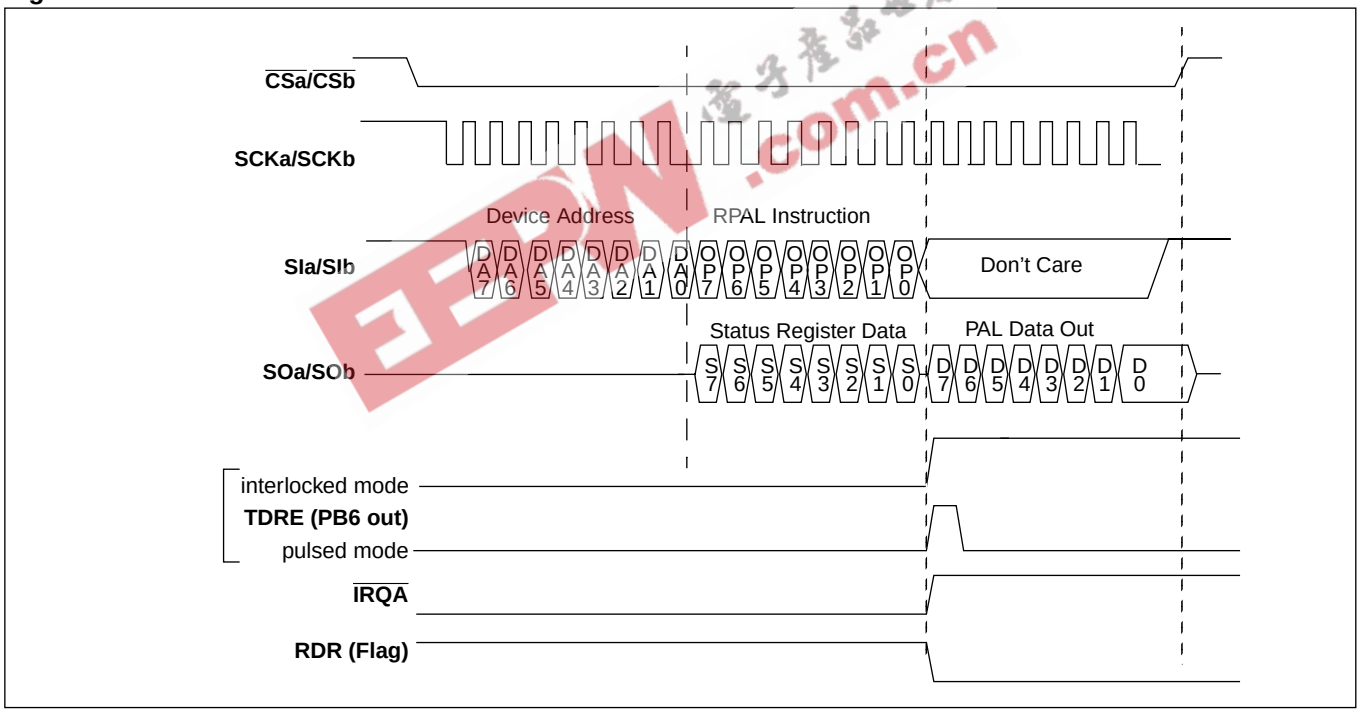


Figure 20. Bi-directional Mode - SPI Read



- **PLS** bit - The pulse bit (PLS) HIGH sets RDRF signal to operate in an "interlocked" mode, where RDRF "tracks" the XRE flag. The PLS bit HIGH sets RDRF to operate in a "pulsed" mode.
- The **TRI** bit HIGH disables the tri-state operation of the port, making the outputs always active in this mode.

Fault monitoring on pins PA7-PA0, PB7 and PB6 is disabled in this mode. Fault monitoring and general I/O functionality of the remaining six Port B pins remains user configurable.

Bi-directional Mode

EXAMPLE APPLICATION:

This Mode provides full handshake capability to allow bidirectional interraction between the host, communicating over the SPI port and a slave processor communicating over parallel port A. In this mode, Port A looks like an SRAM to the slave processor.

MODE ENTRY:

Set **HS2, HS1, HS0** bits in PCR register to 111.

SIGNALS:

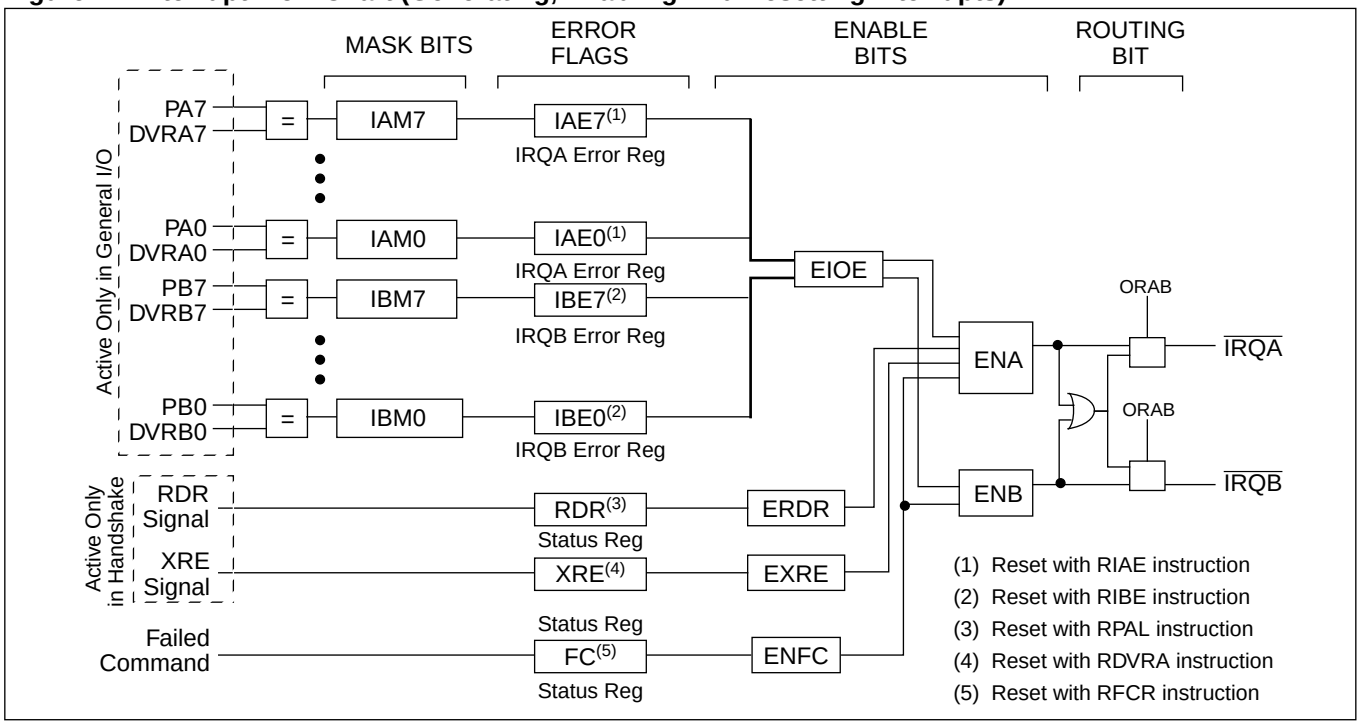
- **Port A** - Bidirectional data passes through this port.
- **DVRA** Register - The host writes data through the SPI port to this register. This SPI write operation sets the XRE status flag LOW and asserts the RDRF signal. The Slave Reads data from this register using $\overline{PEN}$ LOW and R/$\overline{W}$ HIGH.
- **Port A Latch** (PAL) - The slave processor writes data through Port A to this register, using $\overline{PEN}$ LOW and R/$\overline{W}$ LOW. This write operation sets the RDR flag. The host processor reads this register through the SPI port.
- **R/$\overline{W}$**(PB7) is the read/write control for the slave processor. This signal works with the $\overline{PEN}$ input to make the port look like a static RAM, where a HIGH on R/$\overline{W}$ selects a read and a LOW selects a write. A read outputs the contents of the DVRA register on the port A pins. A write transfers the data on the port A pins to the Port A Latch (PAL).
- The **$\overline{PEN}$**(PB4) input controls the Port A operation and functions like a chip select. $\overline{PEN}$ HIGH sets all Port A pins to a high impedance state. $\overline{PEN}$ LOW and R/$\overline{W}$ HIGH initiates a read operation that terminates on the rising edge of the $\overline{PEN}$ input. $\overline{PEN}$ LOW and R/$\overline{W}$ LOW initiates a write operation that termnates with either the R/$\overline{W}$ or $\overline{PEN}$ signals going HIGH.
- The **TDRE**(PB6) output signal provides notification that data was read from Port A and the buffer is now empty.
- The **RDRF**(PB5) output signal notifies the slave processor that new data is available on Port A.
- **INVB** bit - The invert bit (INVB) sets the active level of both the RDRF and TDRE output signals.
- The **RDR** flag in the status register provides status of an external write to Port A. Writing data to the PAL sets RDR HIGH. RDR going HIGH generates an interrupt when the ERDR bit is set. Reading the PAL register through the SPI port clears the RDR bit.
- The **XRE** flag in the status register provides status of an external read of Port A. Writing data to the DVRA through the SPI port sets XRE LOW. Reading the DVRA register through Port A sets the XRE bit. XRE going HIGH generates an interrupt when the EXRE bit is set.
- **PLS** Bit - The pulse bit (PLS) LOW causes the RDRF and TDRE signals to function “interlocked” with the XRE and RDR flags respectively. The PLS bit HIGH causes the RDR and TDRE signals to operate in a “pulsed” mode. The Bi-directional mode disables Fault monitoring on all Port A pins (PA7-PA0) and some Port B pins (PB7-PB4).

Fault monitoring and general I/O functions of the remaining four port B pins remain user configurable.

INTERRUPT REQUESTS

Figure 21 shows the conditions for generating and enabling the interrupts. If not masked out, the occurance of an interrupt sets a flag in the IRQ Error Register. If enabled (by setting the ENA or ENB bits), then an $\overline{IRQA}$

Figure 21. Interrupt Flow Chart (Generating, Enabling And Resetting Interrupts)



or $\overline{IRQB}$ output signal results, otherwise only the flag is set. Certain instructions clear the interrupt condition (See Figure 21). Clearing an interrupt condition resets the interrupt flag and releases the interrupt output.

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... -65°C to +135°C
Storage Temperature ..... -65°C to +150°C
Voltage on any pin with respect to Vss .....-1V to +7V
DC Output Current..... 10mA
Lead Temperature (Soldering, 10 Seconds) .....300°C

***COMMENT**

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temp	Min.	Max.
Commercial	0°C	+70°C
Industrial	–40°C	+85°C

Supply Voltage	Limits
X5114	5V ±10%

D.C. OPERATING CHARACTERISTICS

T_A = -40°C to +85°C, Vcc = +4.5V to +5.5V, unless otherwise specified.

Symbol	Parameter	Min	Max	Unit
I_{CC}	Vcc Supply Current, f_{SCKa} or f_{SCKb} = 2.0MHz; Vcc = +5.5V; SOa, SOb = Open (Active, Non-Volatile Write States only)		5	mA
I_{SB}	Standby Current, Vcc = +5.5V; V_{IN} = Vss or Vcc; $\overline{CSa}$ = $\overline{CSb}$ = Vcc;		2	mA
I_{LI}	Input Leakage current, V_{IN} = Vss to Vcc		10	uA
I_{LO}	Output Leakage current, V_{OUT} = Vss to Vcc		10	uA
V_{IL}(1)	Input Low Voltage	-0.5	Vcc x 0.3	V
V_{IH}(1)	Input High Voltage	Vcc x 0.7	Vcc + 0.5	V
V_{OL}	Output Low Voltage, I_{OL} = +3mA		0.4	V
V_{OH}	Output High Voltage, V_{CC} = +5V; I_{OH} = -3mA	Vcc - 0.8		V

(1) V_{IL} min. and V_{IH} max. are for reference only and not tested.

PORT A INPUT THRESHOLD

ADS	TU2	TU1	TU0	Parameter(1)	Typ	Typ (Vcc=5V)	Max. Error	Units	Comments
1	1	1	1	Input Port A Threshold Level	Vcc * .9	4.5	±0.1	V	ADS, TU2-TU0 are bits in the Threshold/Block Lock Register (TBL)
1	1	1	0		Vcc * .8	4.0	±0.1	V	
1	1	0	1		Vcc * .7	3.5	±0.1	V	
1	1	0	0		Vcc * .6	3.0	±0.1	V	
0	x	x	x		Vcc * .5	2.5	±0.1	V	
1	0	1	1		Vcc * .4	2.0	±0.1	V	
1	0	1	0		Vcc * .3	1.5	±0.1	V	
1	0	0	1		Vcc * .2	1.0	±0.1	V	
1	0	0	0		Vcc * .1	0.5	±0.1	V	

Notes: (1) These parameters are periodically sampled and not 100% tested.

CAPACITANCE

T_A = +25°C, V_{CC} = +5V, f_{SCK} = 2.0MHz

Symbol	Parameter	Max	Unit	Test Conditions
C_{OUT} (1)	Output Capacitance	10	pF	V_{OUT} = 0V
C_{IN} (1)	Input Capacitance	6	pF	V_{IN} = 0V

Notes: (1) This parameter is periodically sampled and not 100% tested.

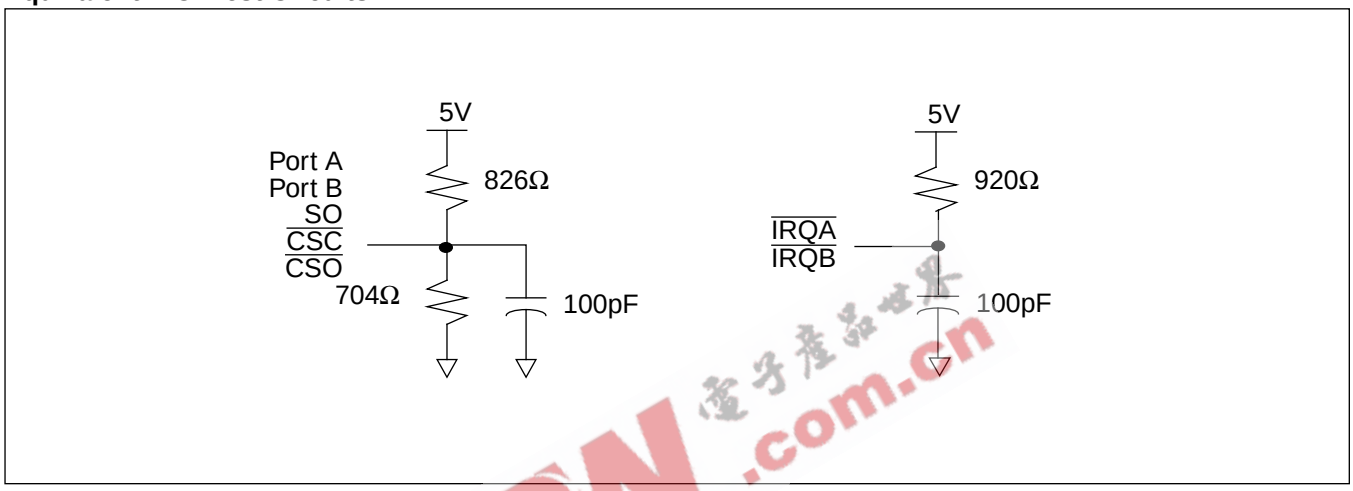
POWER-ON TIMING

Symbol	Parameter	Min	Max	Unit
t_{RVCC}	Vcc Rise Time		0.1	V/uS
t_{POR}(1)	Power Supply Stable to Issuance of an Instruction without nonvolatile write Cycle	1		mS
t_{POW}(1)	Power Supply Stable to Issuance of an Instruction with a nonvolatile write Cycle	5		mS

A.C. CONDITIONS OF TEST

Input Pulse Levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input Rise and Fall Times	10 nS
Input and Output Timing Levels	V_{CC} x 0.5
Output Load	Equivalent Output

Equivalent A.C. Test Circuits



A.C. CHARACTERISTICS

SPI Timing (SPI Clock Mode 3 Only)

T_A = -40°C to +85°C, Vcc = 4.5V to +5.5V, unless otherwise specified.

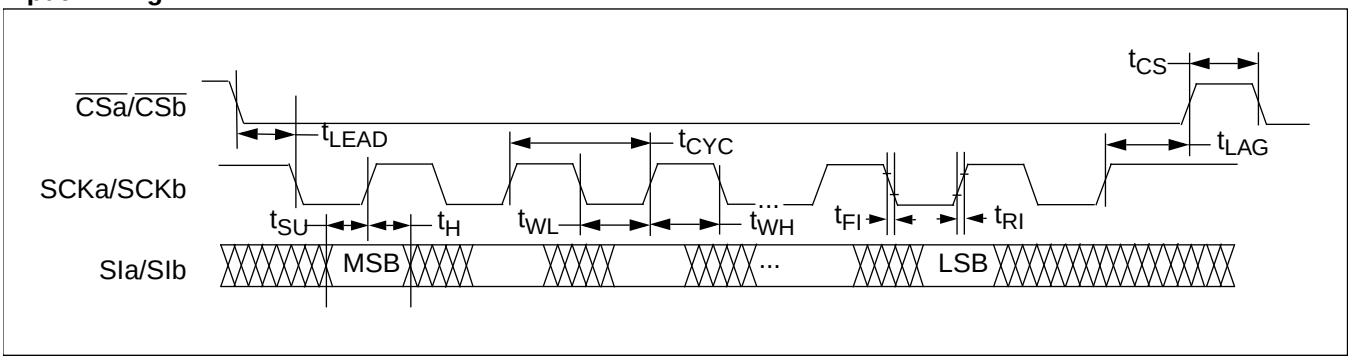
Symbol	Parameter	Min	Max	Unit
f_{SCK}	SPI Clock Frequency		2	MHz
t_{CYC}	SPI Clock Cycle Time	500		nS
t_{WH}	SPI Clock High Time	200		nS
t_{WL}	SPI Clock Low Time	200		nS
t_{LEAD}	Lead Time	200		nS
t_{LAG}	Lag Time	400		nS
t_{SU}	Input Setup Time	50		nS
t_H	Input Hold Time	50		nS
t_{RI} (1)	Input Rise Time		50	nS
t_{FI} (1)	Input Fall Time		50	nS
t_{DIS}	SO Output Disable Time	0		nS
t_V	SO Output Valid Time		100	nS
t_{HO}	SO Output Hold Time	0		nS
t_{RO} (1)	SO Output Rise Time		50	nS
t_{FO} (1)	SO Output Fall Time		50	nS
T_I	SPI Noise Suppression Time Constant		20	nS
t_{CS}	SPIA_$\overline{CS}$ or SPIB_$\overline{CS}$ Deselect Time	100		nS
t_{ASU}	Device Address Setup Time	100		nS
t_{AH}	Device Address Hold Time	0		nS

Notes: (1) This parameter is periodically sampled and not 100% tested.

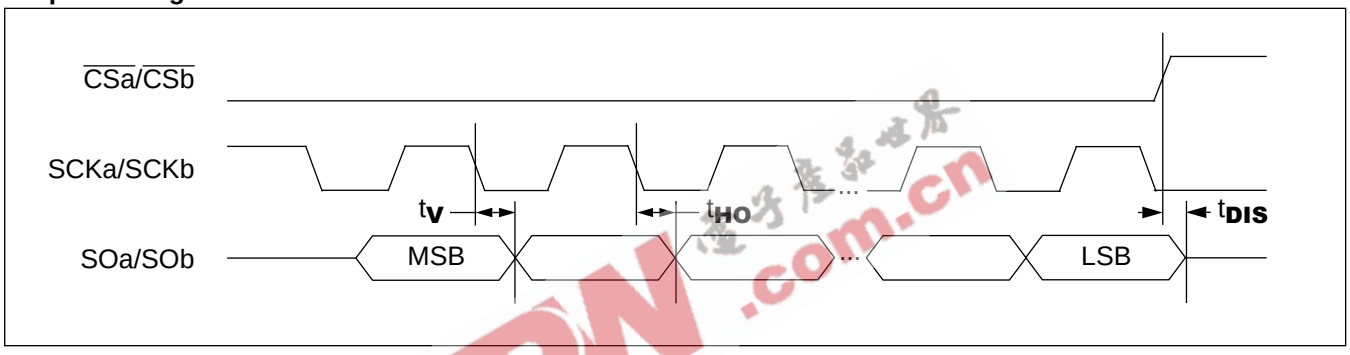
NONVOLATILE WRITE CYCLE TIMING

Symbol	Parameter	Typ	Max	Unit
t_{WC}	Nonvolatile Write Cycle Time	5	10	mS

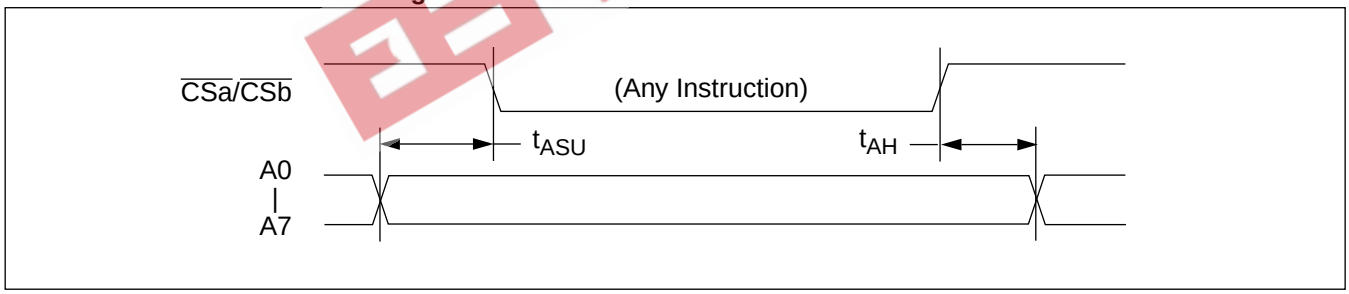
Input Timing



Output Timing



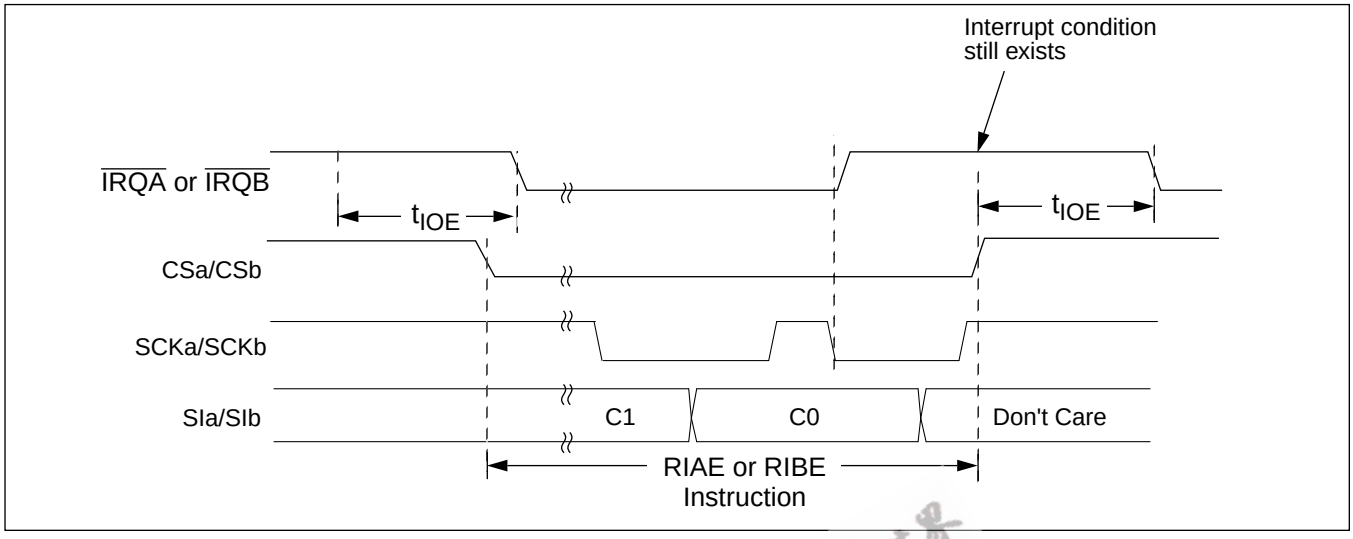
Hardware Device Address Timing



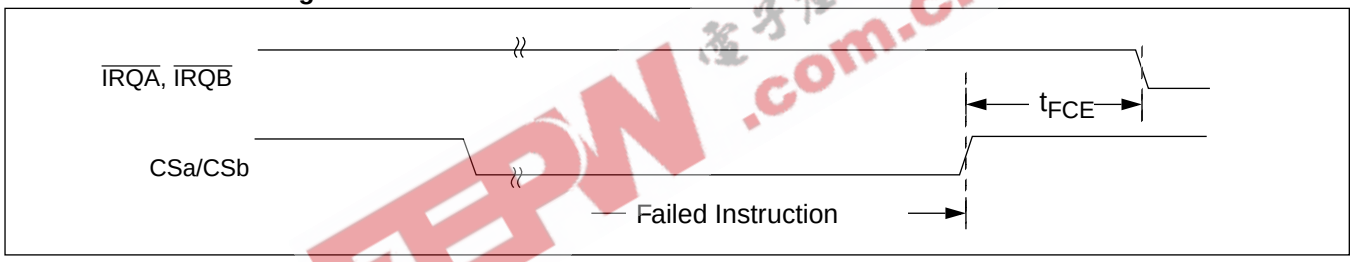
IRQ GENERATION TIMING

Symbol	Parameter	Min	Max	Unit
t_{IOE}	Interrupt Output Enable time (Initial error condition valid or Error condition still valid after reset of error flag.)	250	800	nS
t_{FCE}	Failed Command Enable time ($\overline{CS}$ HIGH to Failed Command error valid)	250	800	nS

Fault Condition



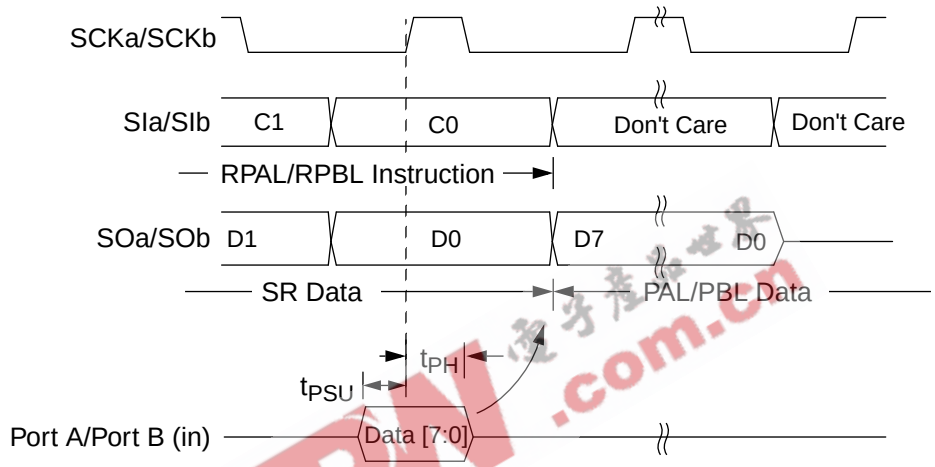
Failed Command Timing



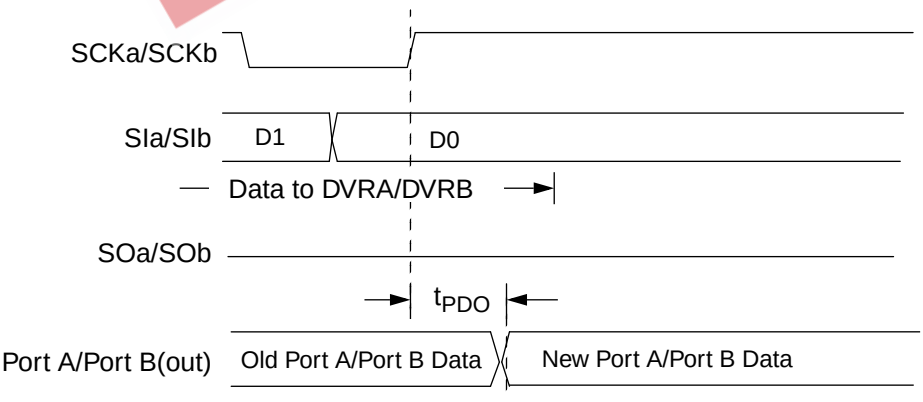
GENERAL I/O TIMING

Symbol	Parameter	Min	Max	Unit
t_{PSU}	Port Setup Time	50		nS
t_{PH}	Port Hold Time	50		nS
t_{PDO}	Port Data Output Valid Time	100		nS

Internal (SPI) Read Data From Port A/Port B



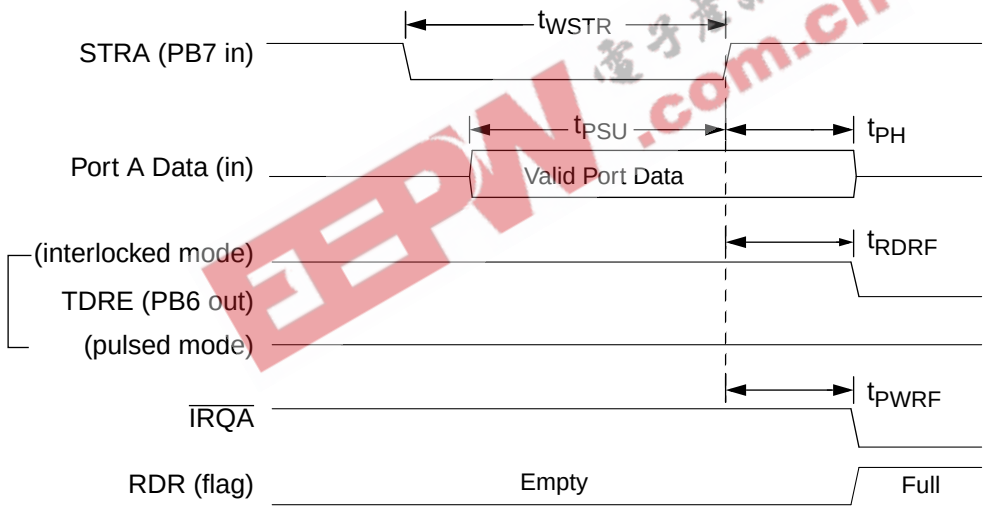
Internal (SPI) Write Data to Port A/Port B



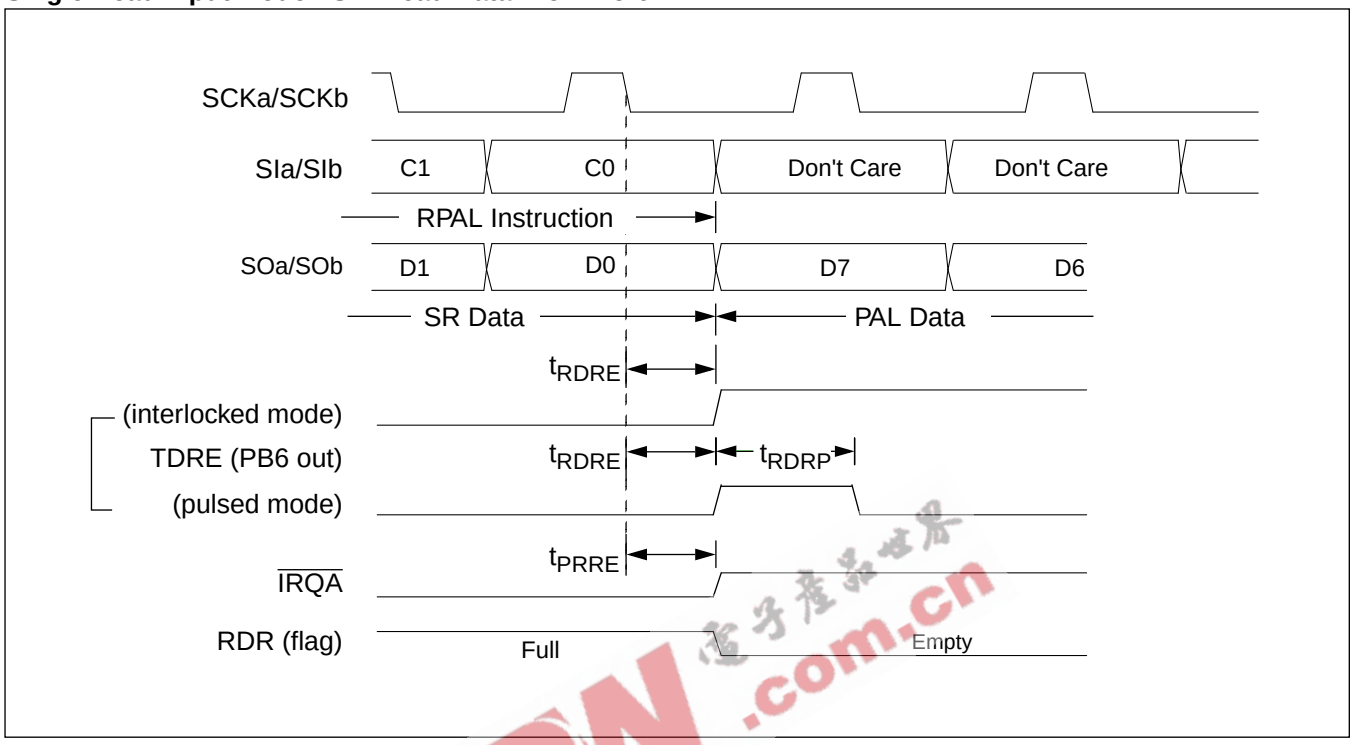
INPUT MODE TIMING

Symbol	Parameter	Min	Max	Unit
t_{PSU}	Port Setup Time	50		nS
t_{PH}	Port Hold Time	70		nS
t_{WSTR}	Write Strobe Time	150		nS
t_{RDRF}	RDR Full Time		100	nS
t_{RDRE}	RDR Empty Time		100	nS
t_{RDRP}	RDR Pulse Time	250	1000	nS
t_{PWRF}	Port Write RDR Full Time	250	800	nS
t_{PRRE}	Port Read RDR Empty Time		500	nS
t_{STRH}	Strobe High Time		100	nS
t_{STRL}	Strobe Low Time		100	nS

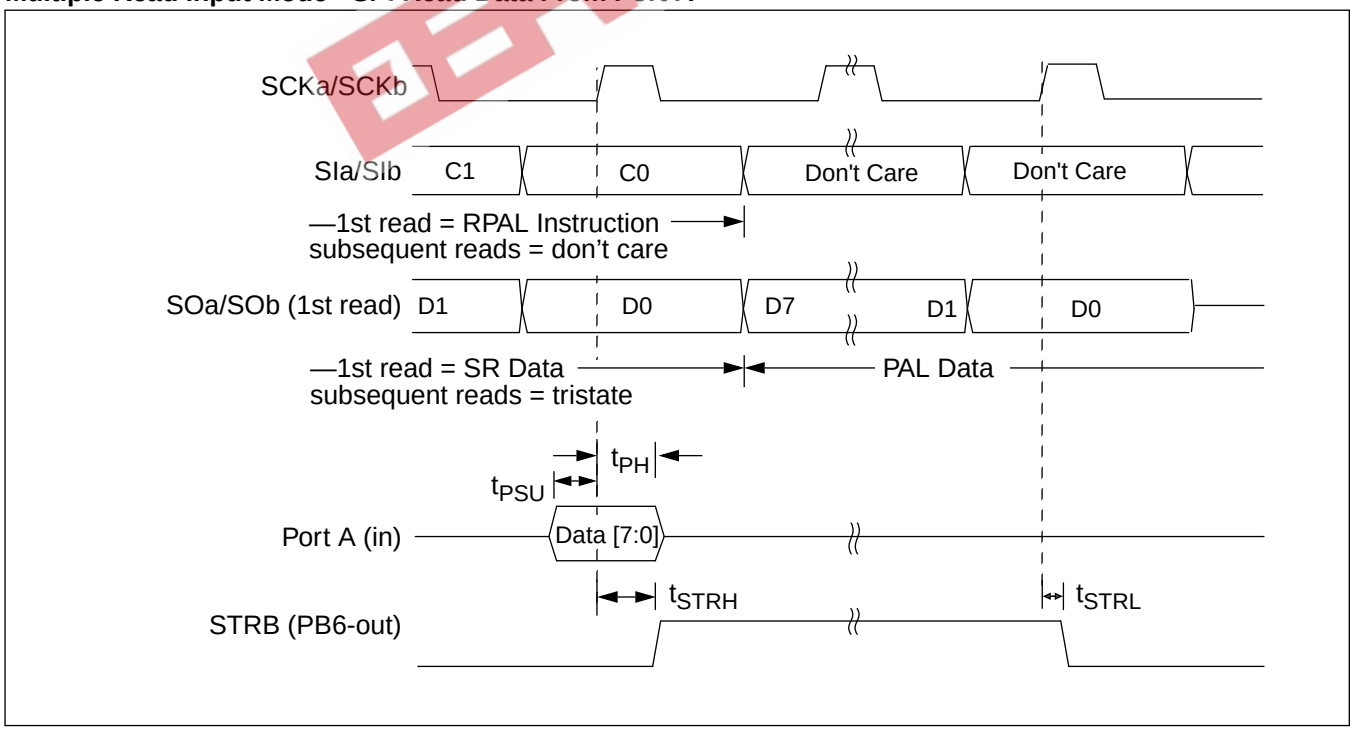
Single Read input Mode - Parallel Write Data to Port A



Single Read input Mode - SPI Read Data From Port A



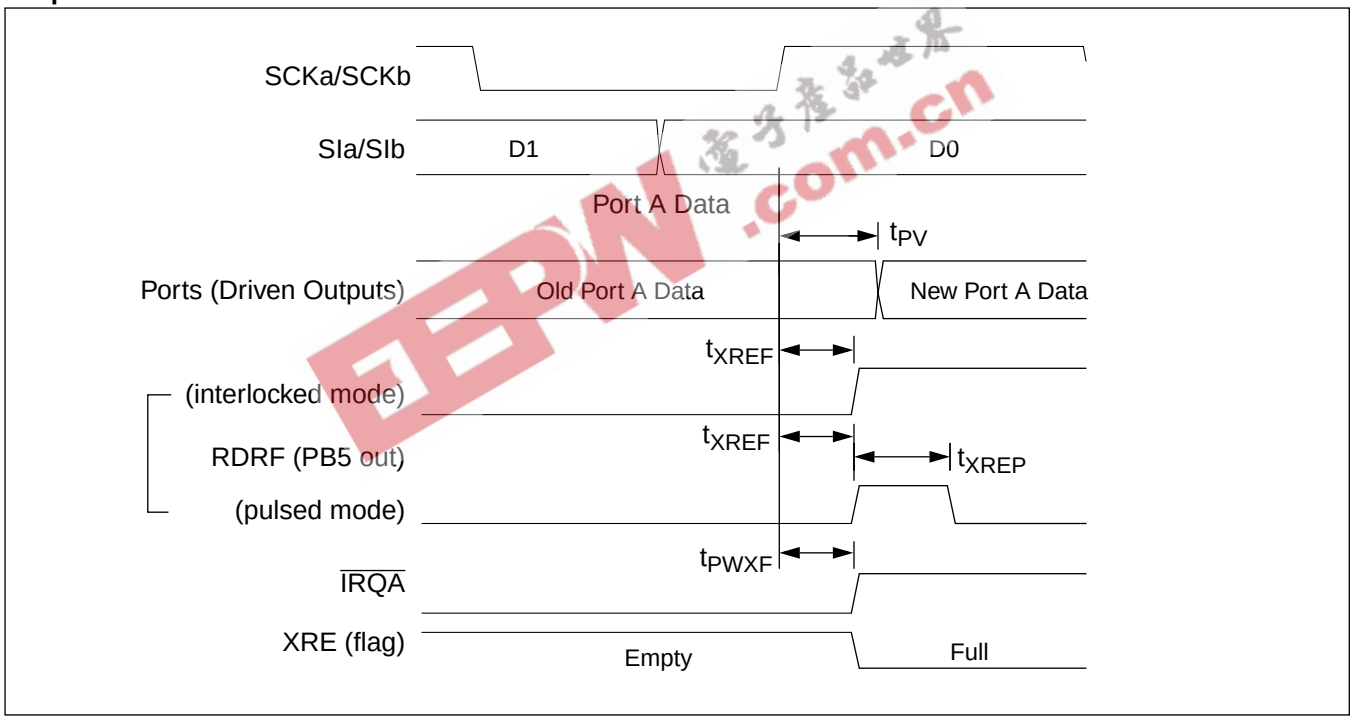
Multiple Read input Mode - SPI Read Data From Port A



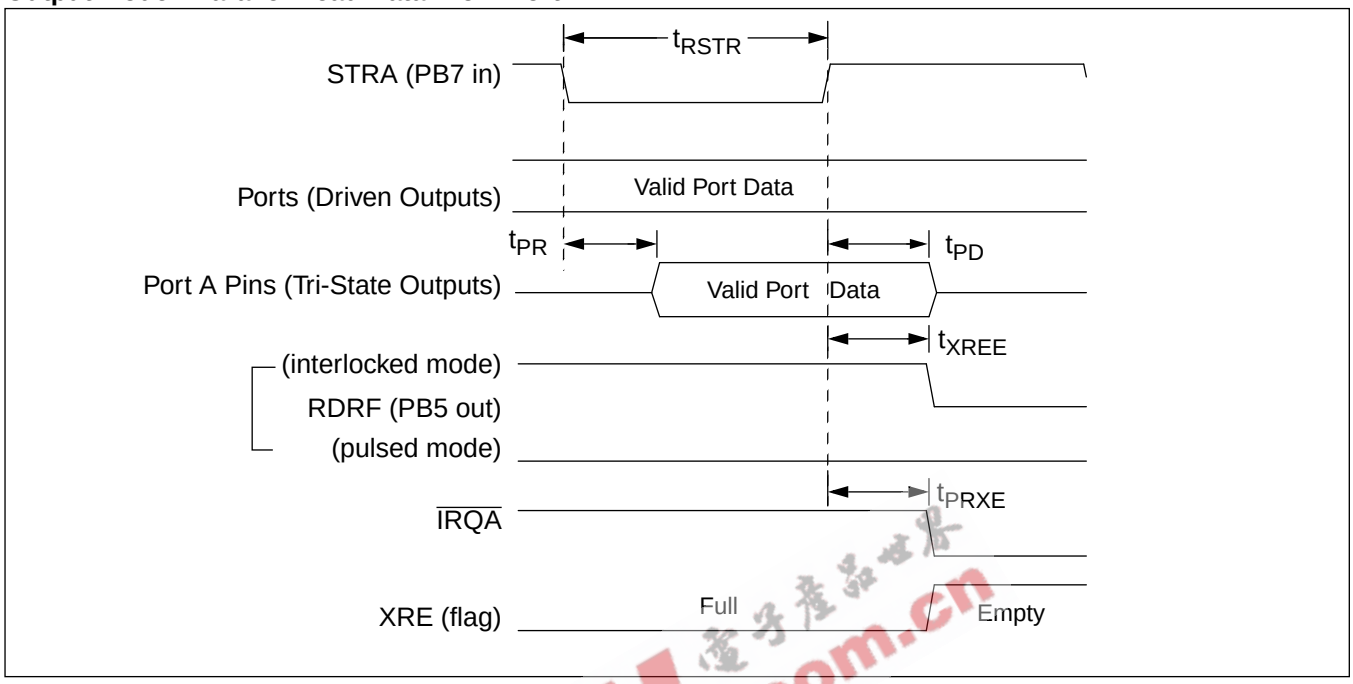
OUTPUT MODE TIMING

Symbol	Parameter	Min	Max	Unit
t_{PV}	Port Valid Time		150	nS
t_{PR}	Port Read Time		100	nS
t_{PD}	Port XRE Disable Time	0		ns
t_{RSTR}	Read Strobe Pulse	150		nS
t_{XREF}	XRE Full Time		250	nS
t_{XREE}	XRE Empty Time		100	nS
t_{XREP}	XRE Pulse Time	250	1000	nS
t_{PWXF}	Port Write XRE Full Set Time		500	nS
t_{PRXE}	Port Read XRE Empty Time	250	800	nS

Output Mode - SPI Write Data to Port A



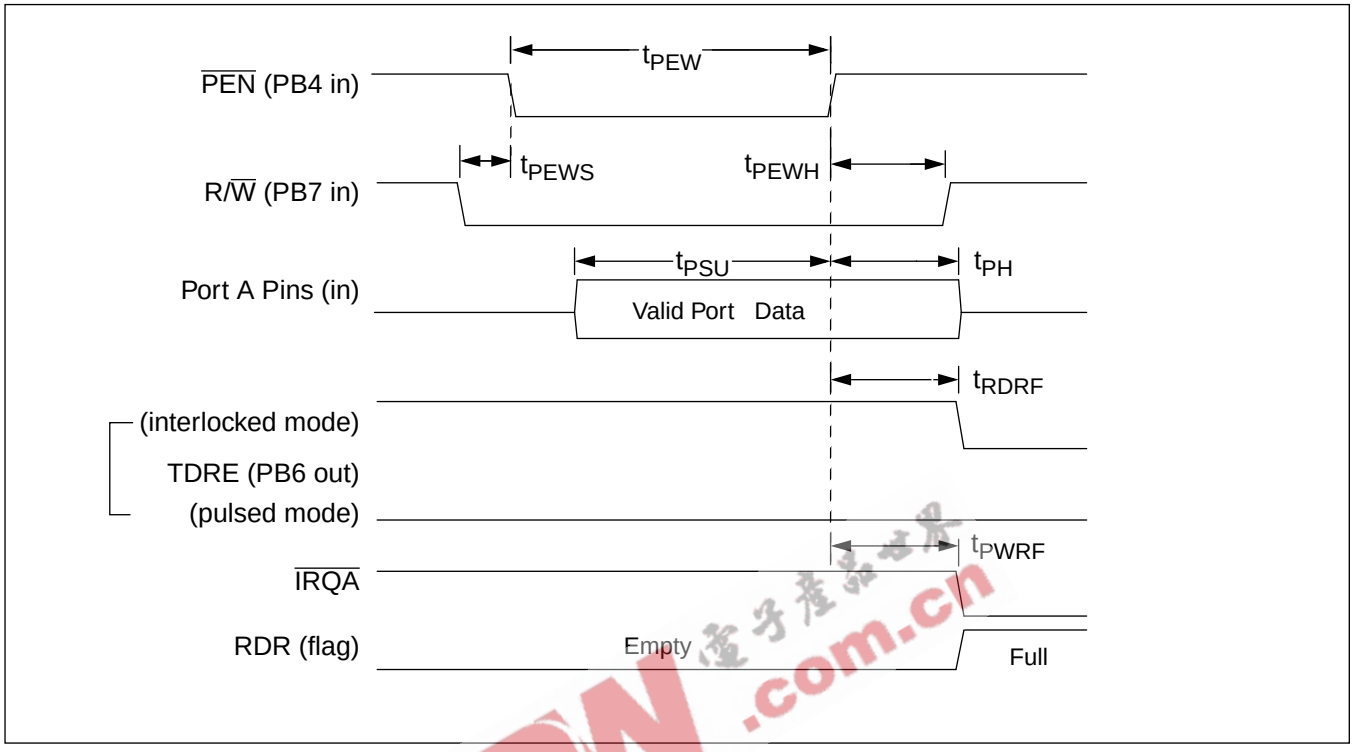
Output Mode - Parallel Read Data From Port A



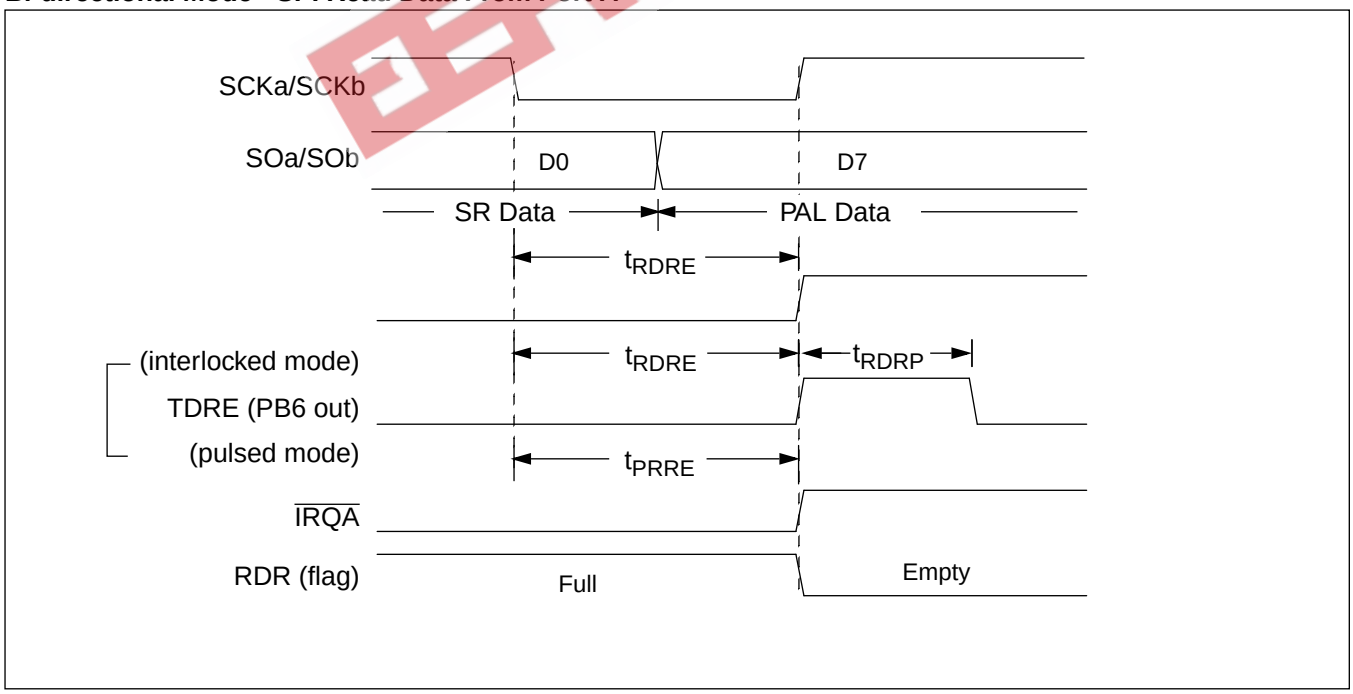
BI-DIRECTIONAL TIMING

Symbol	Parameter	Min	Max	Unit
t_{PSU}	Port Setup Time	50		nS
t_{PH}	Port Hold Time	50		nS
t_{PV}	Port Valid Time		100	nS
t_{RDRF}	RDR Full Time		100	nS
t_{RDRE}	RDR Empty Time		100	nS
t_{RDRP}	RDR Pulse Time	250	1000	nS
t_{PWRF}	Port Write RDR Full Time	250	800	nS
t_{PRRE}	Port Read RDR Empty Time		500	nS
t_{XREF}	XRE Full Time		250	nS
t_{XREE}	XRE Empty Time		100	nS
t_{XREP}	XRE Pulse Time	250	1000	nS
t_{PWXF}	Port Write XRE Full Set Time		500	nS
t_{PRXE}	Port Read XRE Empty Time	250	800	nS
t_{PEW}	Port Enable Write Time	150		nS
t_{PEPR}	Port Read Time		100	nS
t_{PEPD}	Port XRE Disable Time	0		ns
t_{PEWS}	R/$\overline{W}$ Setup Time	20		nS
t_{PEWH}	R/$\overline{W}$ Hold Time	0		nS
t_{PER}	Port Enable Read Time	150		nS

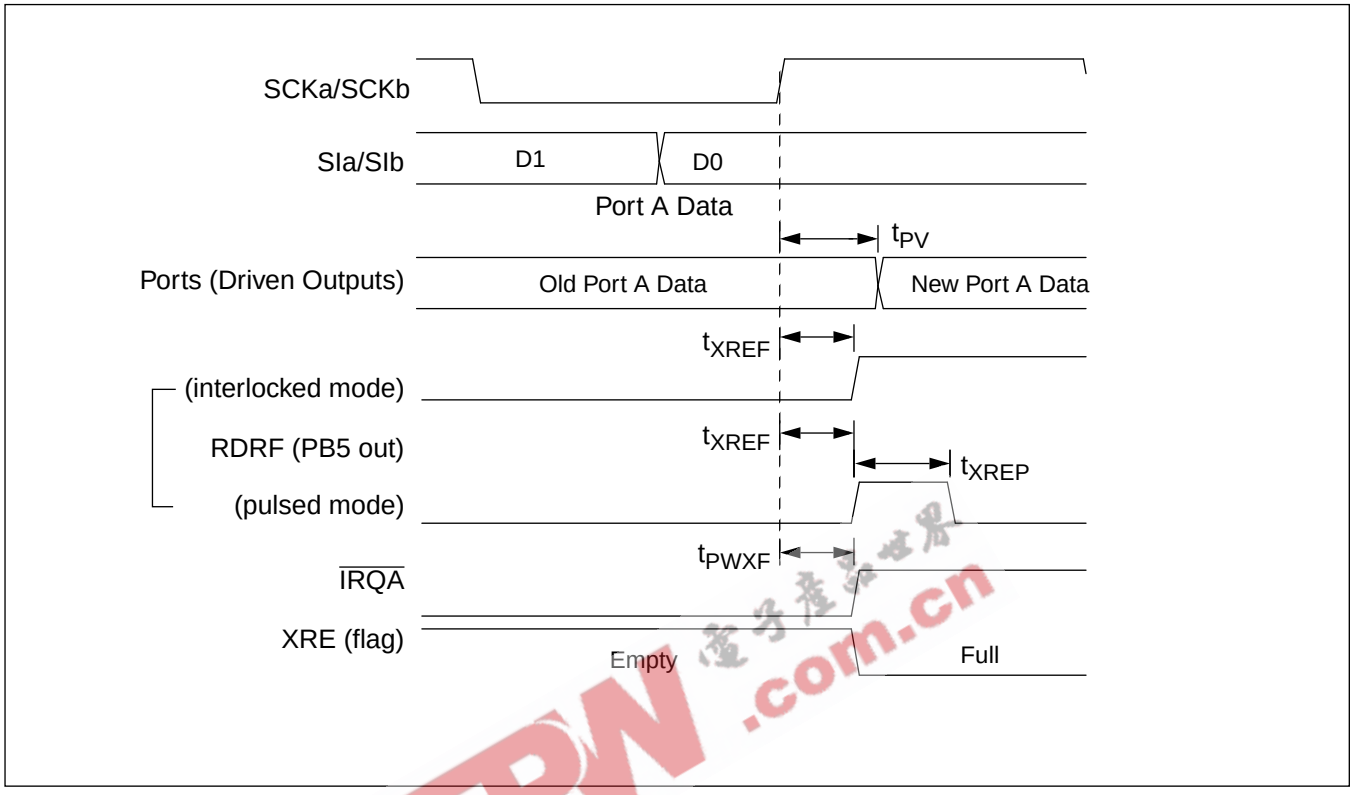
Bi-directional Mode - Parallel Write Data to Port A



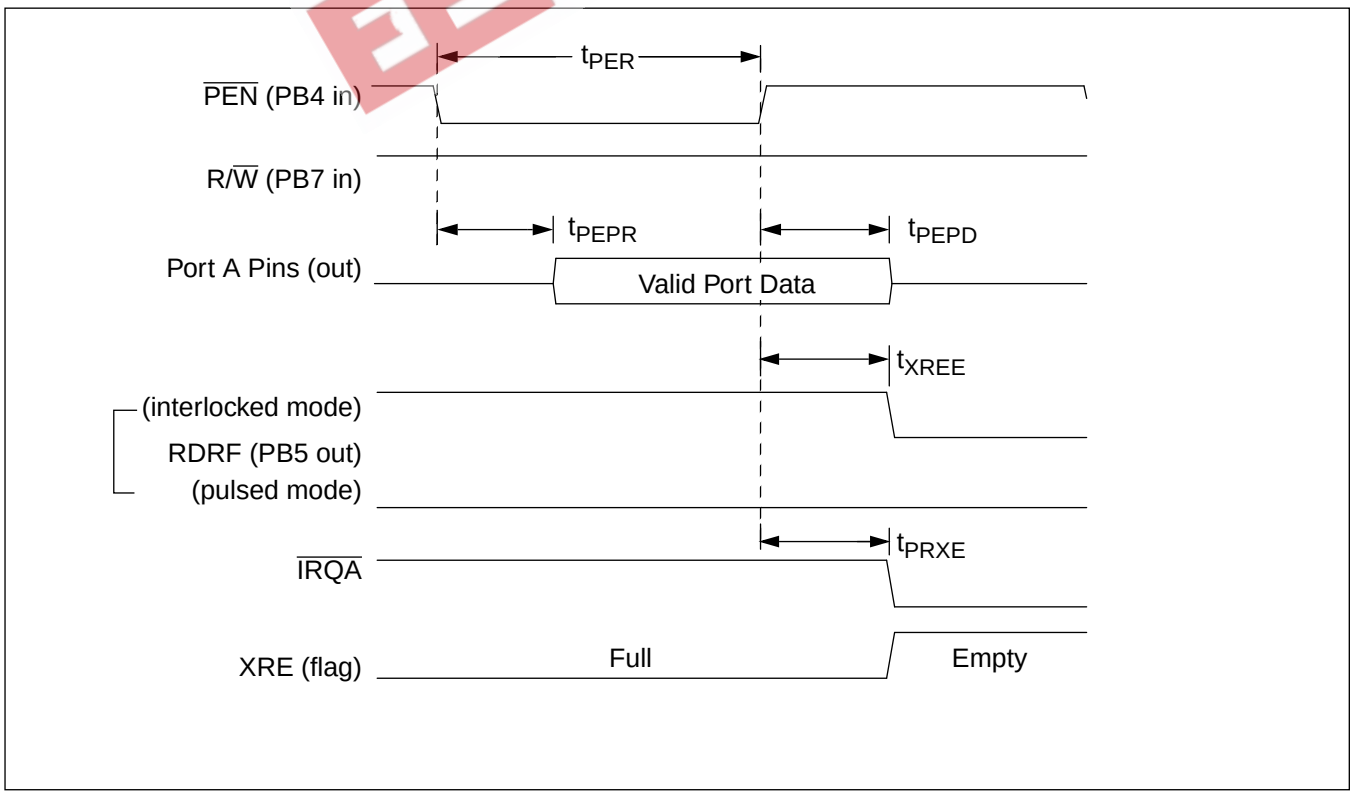
Bi-directional Mode - SPI Read Data From Port A



Bi-directional Mode - SPI Write Data to Port A



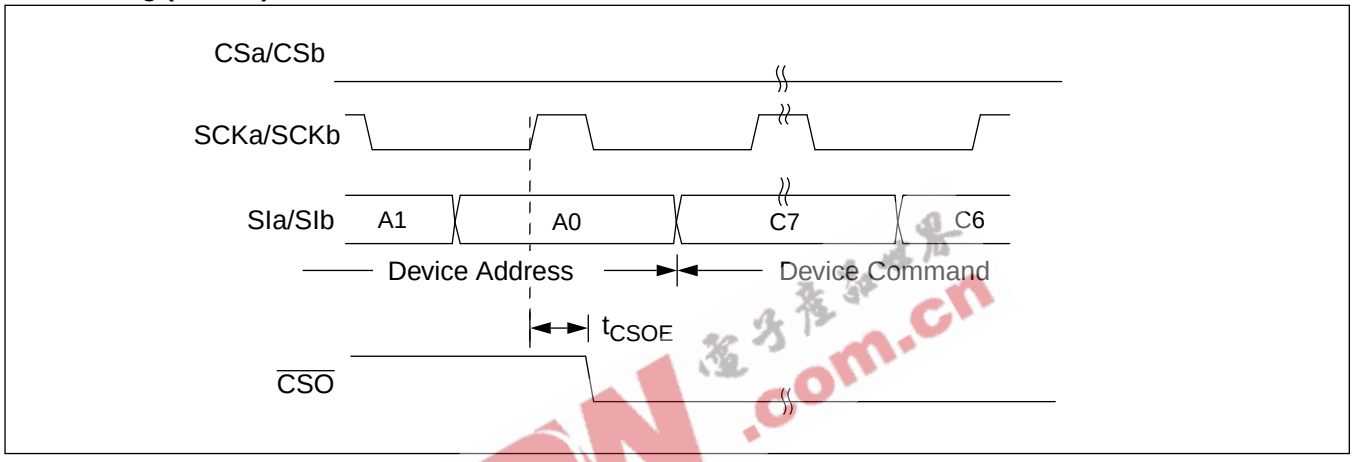
Bi-directional Mode - Parallel Read Data From Port A



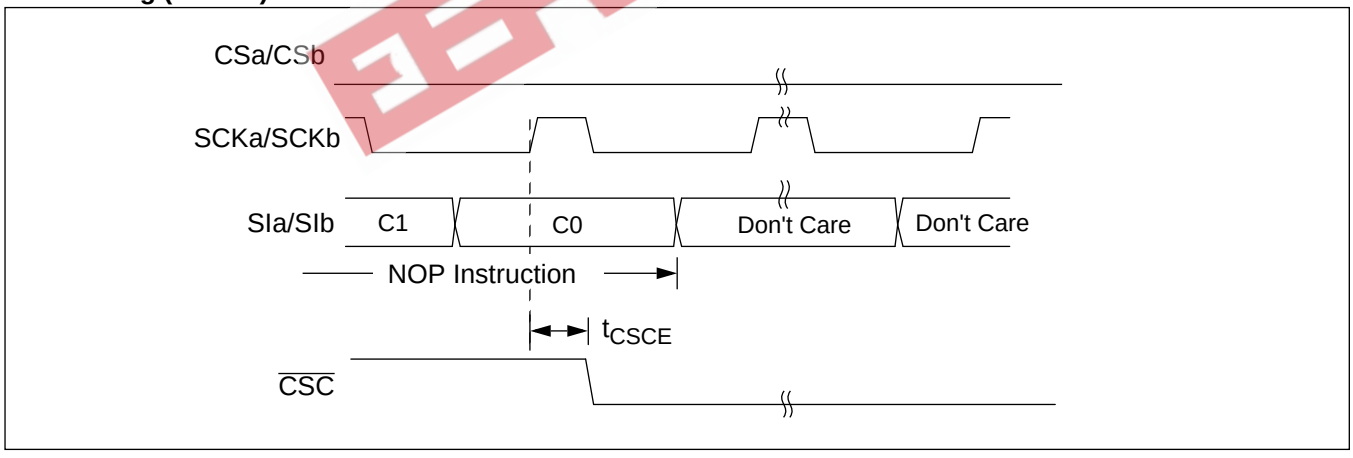
CSO/CSC TIMING

Symbol	Parameter	Min	Max	Unit
t_{CSOE}	Chip Select Output Enable time		200	nS
t_{CSCE}	Chip Select Cascade Enable time		200	nS
t_{CSOD}	Chip Select Output Disable time		100	nS
t_{CSCD}	Chip Select Cascade Disable time		100	nS

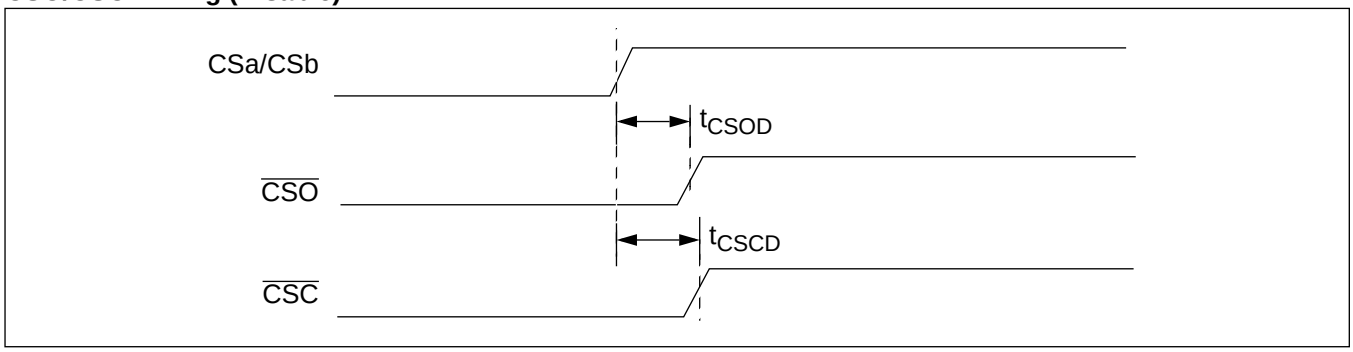
$\overline{CSO}$ Timing (Enable)



$\overline{CSC}$ Timing (Enable)

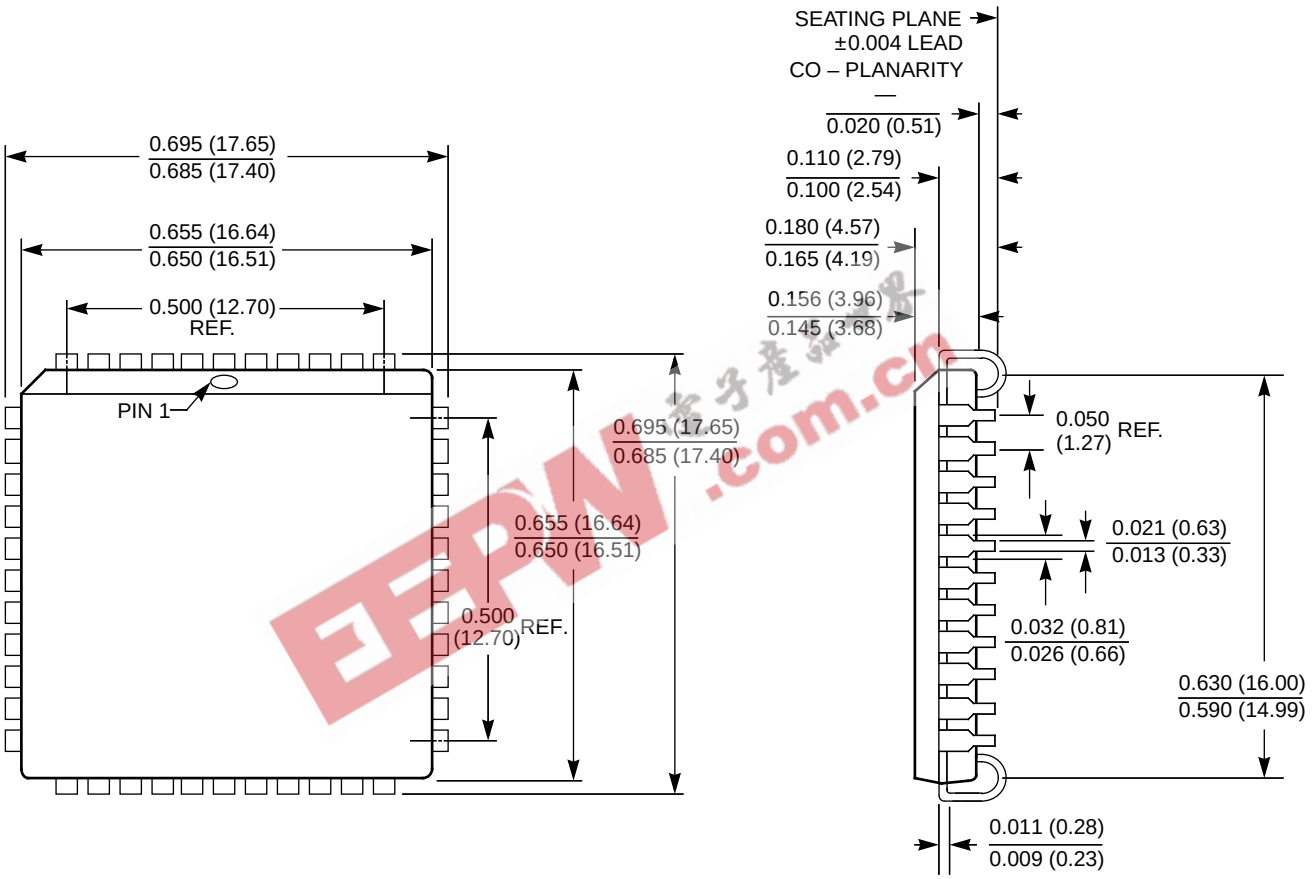


$\overline{CSO}$/$\overline{CSC}$ Timing (Disable)



PACKAGING INFORMATION

44-PIN PLASTIC LEADED CHIP CARRIER PACKAGE TYPE J

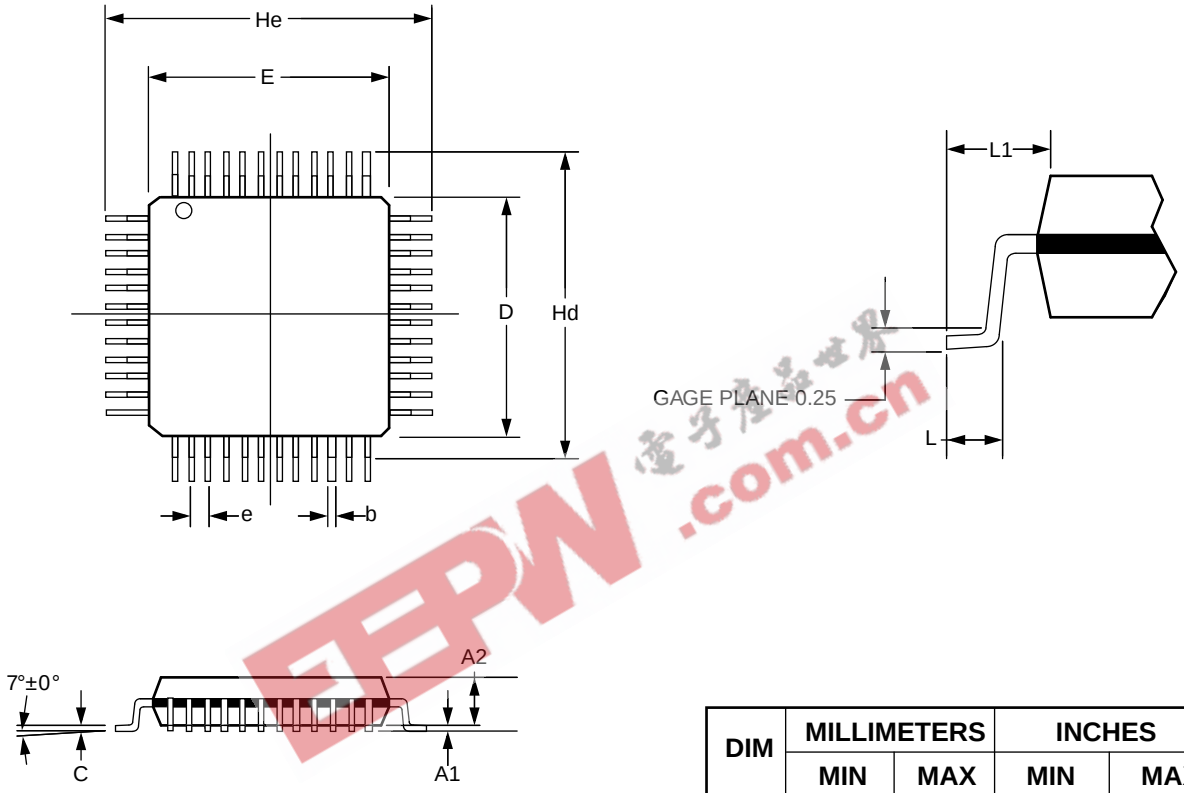


NOTES:
1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
2. DIMENSIONS WITH NO TOLERANCE FOR REFERENCE ONLY

3926 ILL F29.2

PACKAGING INFORMATION

48-LEAD THIN QUAD FLAT PACK (TQFP) PACKAGE TYPE L



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A_1	0.05	0.15	0.002	0.006
A_2	1.35	1.45	0.53	0.057
b	0.17	0.27	0.007	0.011
c	0.090	0.200	0.004	0.008
D	7.0 BSC		0.273 BSC	
E	7.0 BSC		0.273 BSC	
e	0.5 BSC		0.02 BSC	
Hd	9.0 BSC		0.35 BSC	
He	9.0 BSC		0.35 BSC	
L	0.45	0.75	0.018	0.030
L_1	1.00 TYP		0.039 TYP	

NOTES:
1. GAGE PLANE DIMENSION IS IN MM.
2. LEAD COPLANARITY SHALL BE 0.10MM [0.004] MAXIMUM.
3. MOLD FLASH NOT INCLUDED IN DIMENSIONS

7052 FM 23

ORDERING INFORMATION