Preliminary Information

This X84160/640/128 device has been acquired by IC MICROSYSTEMS from Xicor, Inc.

ICmic™ IC MICROSYSTEMS

16K/64K/128K X84160/640/128 MPS™ EEPROM

Advanced MPS™ Micro Port Saver EEPROM with Block Lock™ Protection

FEATURES

- **Up to 15MHz data transfer rate**
- **20ns Read Access Time**
- **Direct Interface to Microprocessors and Microcontrollers**
  - **—Eliminates I/O port requirements**
  - **—No interface glue logic required**
  - **—Eliminates need for parallel to serial converters**
- **Low Power CMOS**
  - **—1.8V–3.6V, 2.5V–5.5V and 5V ± 10% Versions**
  - **—Standby Current Less than 1µA**
  - **—Active Current Less than 1mA**
- **Byte or Page Write Capable**
  - **—32-Byte Page Write Mode**
- **New Programmable Block Lock™ Protection**
  - **—Software Write Protection**
  - **—Programmable Hardware Write Protection**
- **Block Lock (0, 1/4, 1/2, or all of the array)**
- **Typical Nonvolatile Write Cycle Time: 3ms**
- **High Reliability**
  - **—100,000 Endurance Cycles**
  - **—Guaranteed Data Retention: 100 Years**
- **Small Package Options**
  - **—8-Lead Mini-DIP Package**
  - **—8, 14-Lead SOIC Packages**
  - **—8, 20, 28-Lead TSSOP Packages**
  - **—8-Lead XBGA Packages**

DESCRIPTION

The µPort Saver memories need no serial ports or special hardware and connect to the processor memory bus. Replacing bytewide data memory, the µPort Saver uses bytewide memory control functions, takes a fraction of the board space and consumes much less power. Replacing serial memories, the µPort Saver provides all the serial benefits, such as low cost, low power, low voltage, and small package size while releasing I/Os for more important uses.

The µPort Saver memory outputs data within 20ns of an active read signal. This is less than the read access time of most hosts and provides “no-wait-state” operation. This prevents bottlenecks on the bus. With rates to 15MHz, the µPort Saver supplies data faster than required by most host read cycle specifications. This eliminates the need for software NOPs.

The µPort Saver memories communicate over one line of the data bus using a sequence of standard bus read and write operations. This “bit serial” interface allows the µPort Saver to work well in 8-bit, 16 bit, 32-bit, and 64-bit systems.

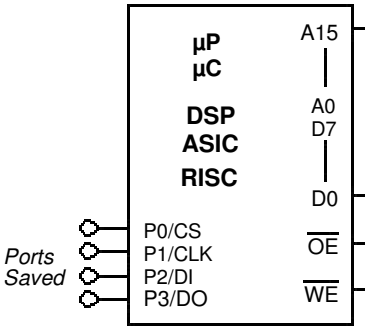
The X84160/640/128 provide additional data security features through Block Lock and programmable Hardware Write Protection. These allow some or all of the array to be write protected by software command or by hardware. System Configuration, Company ID, calibration information or other critical data can be secured against unexpected or inadvertent program operations, leaving the remainder of the memory available for the system or user access

A Write Protect ($\overline{WP}$) pin prevents inadvertent writes to the memory.

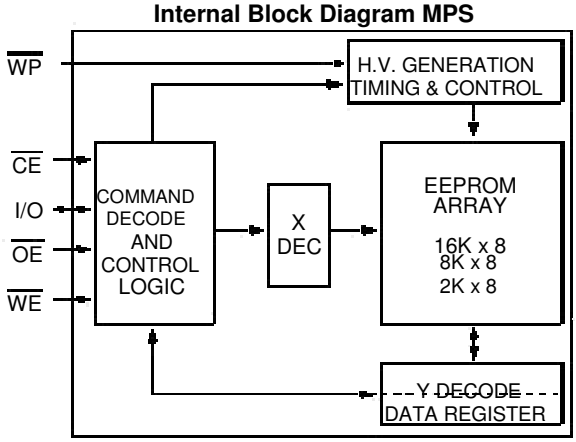
Xicor EEPROMs are designed and tested for applications requiring extended endurance. Inherent data retention is greater than 100 years.

BLOCK DIAGRAM

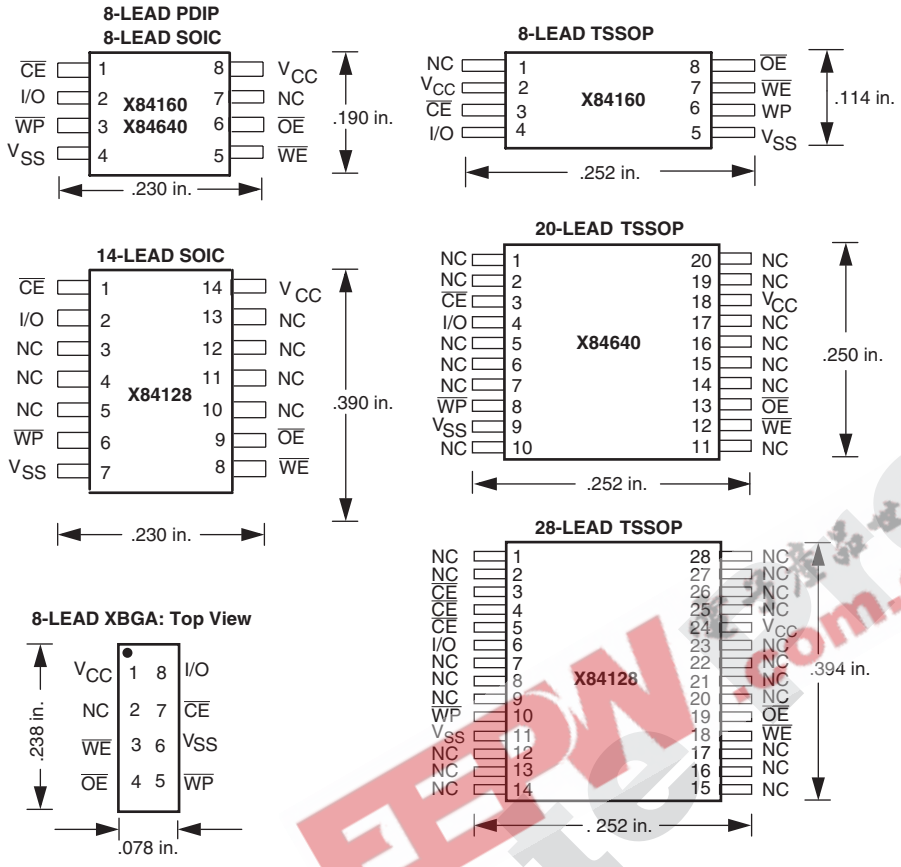
System Connection



Internal Block Diagram MPS



PIN CONFIGURATIONS: Drawings are to the same scale, actual package sizes are shown in inches:



PIN NAMES

I/O	Data Input/Output
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
$\overline{WP}$	Write Protect Input
V_{CC}	Supply Voltage
V_{SS}	Ground
NC	No Connect

PACKAGE SELECTION GUIDE

84160	8-Lead PDIP 8-Lead SOIC 8-Lead TSSOP
84640	8-Lead CSP/BGA 8-Lead PDIP 8-Lead SOIC 20-Lead TSSOP
84128	8-Lead CSP/BGA 8-Lead PDIP 14-Lead SOIC 28-Lead TSSOP

PIN DESCRIPTIONS

Chip Enable ($\overline{CE}$)

The Chip Enable input must be LOW to enable all read/write operations. When $\overline{CE}$ is HIGH, the chip is deselected, the I/O pin is in the high impedance state, and unless a nonvolatile write operation is underway, the device is in the standby power mode.

Output Enable ($\overline{OE}$)

The Output Enable input must be LOW to enable the output buffer and to read data from the device on the I/O line.

Write Enable ($\overline{WE}$)

The Write Enable input must be LOW to write either data or command sequences to the device.

Data In/Data Out (I/O)

Data and command sequences are serially written to or serially read from the device through the I/O pin.

Write Protect ($\overline{WP}$)

The Write Protect input controls the Hardware Write Protect feature. When $\overline{WP}$ is LOW and the nonvoltaile bit WPEN is “1”, nonvolatile writes of the X84160/640/128 control register is disabled, but the part otherwise functions normally. When $\overline{WP}$ is held HIGH, all functions, including nonvolatile write operate normally. $\overline{WP}$ going LOW while $\overline{CS}$ is still LOW will interrupt a write to the X84160/640/128 control register. If the internal Write cycle has already been initiated, $\overline{WP}$ going LOW will have no effect on write.

The $\overline{WP}$ pin function is blocked when the WPEN bit in the control register is “0”. This allows the user to install the X84160/640/128 in a system with $\overline{WP}$ pin grounded and still be able to write to the control register. The $\overline{WP}$ pin functions will be enabled when the WPEN bit is set “1”.

DEVICE OPERATION

The X84160/640/128 are serial EEPROMs designed to interface directly with most microprocessor buses. Standard $\overline{CE}$, $\overline{OE}$, and $\overline{WE}$ signals control the read and write operations, and a single I/O line is used to send and receive data and commands serially.

Data Timing

Data input on the I/O line is latched on the rising edge of either $\overline{WE}$ or $\overline{CE}$, whichever occurs first. Data output on the I/O line is active whenever both $\overline{OE}$ and $\overline{CE}$ are LOW. Care should be taken to ensure that $\overline{WE}$ and $\overline{OE}$ are never both LOW while $\overline{CE}$ is LOW.

Read Sequence

A read sequence consists of sending a 16-bit address followed by the reading of data serially. The address is written by issuing 16 separate write cycles ($\overline{WE}$ and $\overline{CE}$ LOW, $\overline{OE}$ HIGH) to the part without a read cycle between the write cycles. The address is sent serially, most significant bit first, over the I/O line. Note that this sequence is fully static, with no special timing restrictions, and the processor is free to perform other tasks on the bus whenever the device $\overline{CE}$ pin is HIGH. Once the 16 address bits are sent, a byte of data can be read on the I/O line by issuing 8 separate read cycles ($\overline{OE}$ and $\overline{CE}$ LOW, $\overline{WE}$ HIGH). At this point, writing a ‘1’ will terminate the read sequence and enter the low power standby state, otherwise the device will await further reads in the sequential read mode.

Sequential Read

The byte address is automatically incremented to the next higher address after each byte of data is read. The data stored in the memory at the next address can be read sequentially by continuing to issue read cycles. When the highest address in the array is reached, the address counter rolls over to address 0000h and reading may be continued indefinitely.

Reset Sequence

The reset sequence resets the device and sets an internal write enable latch. A reset sequence can be sent at any time by performing a read/write “0”/read operation (see Figs. 1 and 2). This breaks the multiple read or write cycle sequences that are normally used to read from or write to the part. The reset sequence can be used at any time to interrupt or end a sequential read or page load. As soon as the write “0” cycle is complete, the part is reset (unless a nonvolatile write cycle is in progress). The second read cycle in this sequence, and any further read cycles, will read a HIGH on the I/O pin until a valid read sequence (which includes the address) is issued. The reset sequence must be issued at the beginning of both read and write sequences to be sure the device initiates these operations properly.

Figure 1. Read Sequence

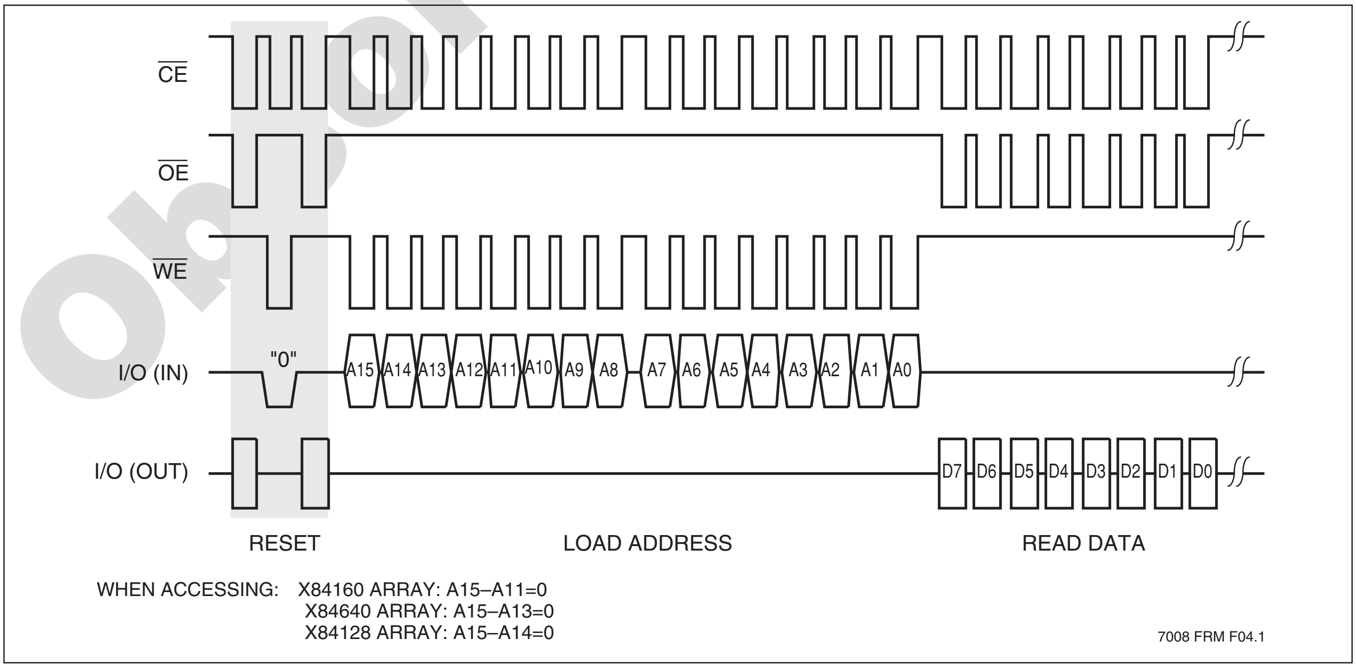
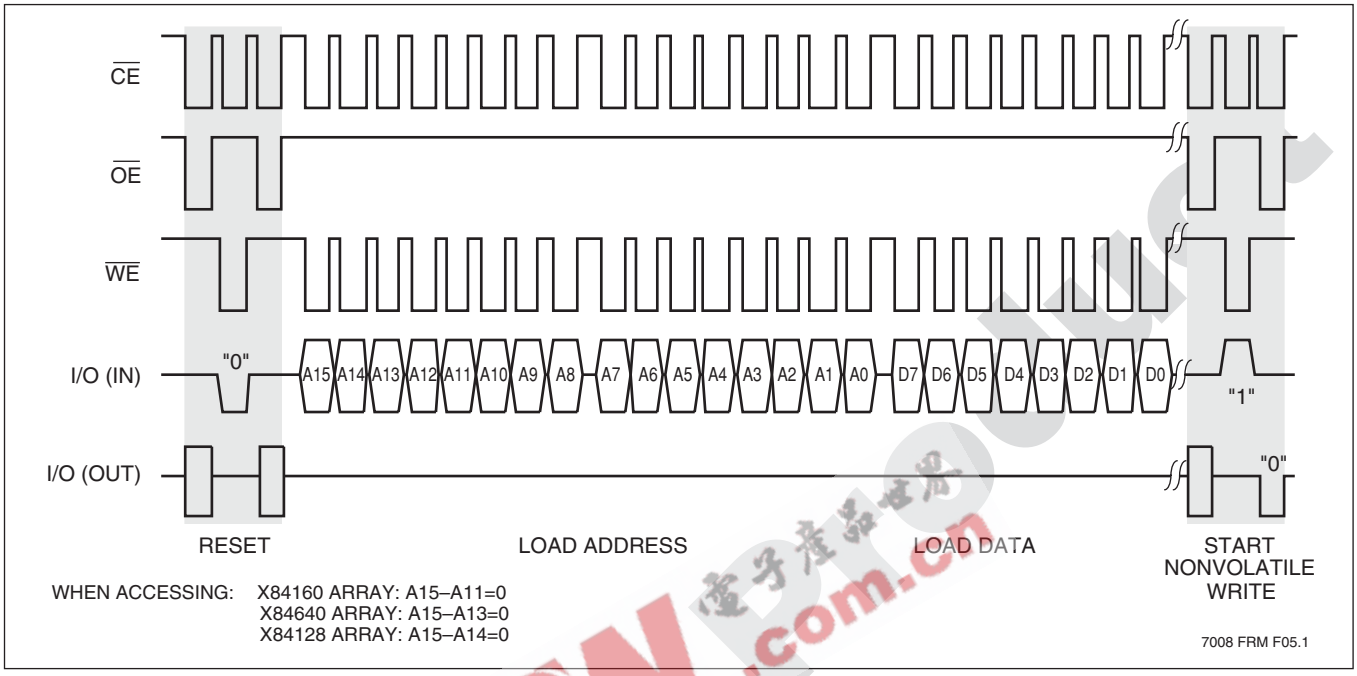


Figure 2: Write Sequence



Write Sequence

A nonvolatile write sequence consists of sending a reset sequence, a 16-bit address, up to 32 bytes of data, and then a special "start nonvolatile write cycle" command sequence.

The reset sequence is issued first (as described in the Reset Sequence section) to set an internal write enable latch. The address is written serially by issuing 16 separate write cycles ($\overline{WE}$ and $\overline{CE}$ LOW, $\overline{OE}$ HIGH) to the part without any read cycles between the writes. The address is sent serially, most significant bit first, on the I/O pin. Up to 32 bytes of data are written by issuing a multiple of 8 write cycles. Again, no read cycles are allowed between writes.

The nonvolatile write cycle is initiated by issuing a special read/write "1"/read sequence. The first read cycle ends the page load, then the write "1" followed by a read starts the nonvolatile write cycle. The device recognizes 32-byte pages (e.g., beginning at addresses XXXXXX00000 for X84160).

When sending data to the part, attempts to exceed the upper address of the page will result in the address counter "wrapping-around" to the first address on the page, where data loading can continue. For this reason, sending more than 256 consecutive data bits will result in overwriting previous data.

A nonvolatile write cycle will not start if a partial or incomplete write sequence is issued. The internal write enable latch is reset when the nonvolatile write cycle is completed and after an invalid write to prevent inadvertent writes. Note that this sequence is fully static, with no special timing restrictions. The processor is free to perform other tasks on the bus whenever the chip enable pin ($\overline{CE}$) is HIGH.

Nonvolatile Write Status

The status of a nonvolatile write cycle can be determined at any time by simply reading the state of the I/O pin on the device. This pin is read when $\overline{OE}$ and $\overline{CE}$ are LOW and $\overline{WE}$ is HIGH. During a nonvolatile write cycle the I/O pin is LOW. When the nonvolatile write cycle is complete, the I/O pin goes HIGH. A reset sequence can also be issued during a nonvolatile write cycle with the same result: I/O is LOW as long as a nonvolatile write cycle is in progress, and I/O is HIGH when the nonvolatile write cycle is done.

CONTROL REGISTER

The X84160/640/128 has one register that contains control bits for the devices. The control bits, WPEN, BP1, and BP0, are shown in Table 1. To read or change the contents of this register requires a one byte operation to address FFFFh.

A read from FFFFh returns the one byte contents of the control register unused bits return 0. Continued reads return undefined data. A write to address FFFFh changes the value of the bits. Unused bits are written as "0". Writing more than one byte to the control register is a violation and the operation will be aborted. After sending one byte to the control register, a start nonvolatile write cycle will latch in the new state.

Table 1

7	6	5	4	3	2	1	0
WPEN	0	0	0	BP1	BP0	0	0

WPEN: Write Protect Enable Bit

The Write-Protect-Enable (WPEN) bit is an enable bit for the $\overline{WP}$ pin.

Table 2

WPEN	$\overline{WP}$	Protected Blocks	Unprotected Blocks	Status Register
0	X	Protected	Writable	Writable
1	LOW	Protected	Writable	Protected
X	HIGH	Protected	Writable	Writable

The Write Protect ($\overline{WP}$) pin and the nonvolatile Write Protect Enable (WPEN) bit in the Status Register control the programmable hardware write protect feature. Hardware write protection is enabled when $\overline{WP}$ pin is LOW, and the WPEN bit is "1". Hardware write protection is disabled when either the $\overline{WP}$ pin is HIGH or the WPEN bit is "0". When the chip is hardware write protected, nonvolatile write is disabled to the Control Register, including the Block Protect bits and the WPEN bit itself, as well as the block-protected sections in the memory array. Only the sections of the memory array that are not block-protected can be written.

Note: When the $\overline{WP}$ pin is tied to V_{SS} and the WPEN bit is HIGH, the WPEN bit is write protected. It cannot be changed back to a "0", as long as the $\overline{WP}$ pin is held LOW.

BP1, BP0: Block Protect Bits

The Block Protect (BP0 and BP1) bits are nonvolatile and allow the user to select one of four levels of protection. The X84160/640/128 is divided into four segments. One, two, or all four of the segments may be protected. That is, the user may read the segments but will be unable to alter (write) data within the selected segments. The partitioning is controlled as illustrated in table 3 below.

Table 3. Block Lock Protection

Control Register Bits		Array Address Protected			
BP1	BP0	X84160	X84640	X84128	Array
0	0	None	None	None	
0	1	0600h–07FFh	1800h–1FFFh	3000h–3FFFh	upper 1/4
1	0	0400h–07FFh	1000h–1FFFh	2000h–3FFFh	upper 1/2
1	1	0000–07FFh	0000–1FFFh	0000h–3FFFh	Full Array (Not including the control register.)

Low Power Operation

The device enters an idle state, which draws minimal current when:

—an illegal sequence is entered. The following are the more common illegal sequences:

- Read/Write/Write—any time
- Read/Write ‘1’—When writing the address or writing data.
- Write ‘1’—when reading data
- Read/Read/Write ‘1’—after data is written to device, but before entering the NV write sequence.

—the device powers-up;

—a nonvolatile write operation completes.

While a sequential read is in progress, the device remains in an active state. This state draws more current than the idle state, but not as much as during a read itself. To go back to the lowest power condition, an invalid condition is created by writing a ‘1’ after the last bit of a read operation.

Write Protection

The following circuitry has been included to prevent inadvertent nonvolatile writes:

—The internal Write Enable latch is reset upon power-up.

—A reset sequence must be issued to set the internal write enable latch before starting a write sequence.

—A special “start nonvolatile write” command sequence is required to start a nonvolatile write cycle.

—The internal Write Enable latch is reset automatically at the end of a nonvolatile write cycle.

—The internal Write Enable latch is reset and remains reset as long as the $\overline{WP}$ pin is LOW, which blocks all nonvolatile write cycles.

—The internal Write Enable latch resets on an invalid write operation.

SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don’t Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

ABSOLUTE MAXIMUM RATINGS*

Temperature under Bias ..... –65°C to +135°C
Storage Temperature ..... –65°C to +150°C
Terminal Voltage with
Respect to V_{SS} .....–1V to +7V
DC Output Current..... 5mA
Lead Temperature (Soldering, 10 seconds).....300°C

*COMMENT

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	+70°C
Industrial	–40°C	+85°C
Military†	–55°C	+125°C

Notes: † Contact factory for Military availability

Supply Voltage	Limits
X84160/640/128	4.5V to 5.5V
X84160/640/128 – 2.5	2.5V to 5.5V
X84160/640/128 – 1.8	1.8V to 3.6V

D.C. OPERATING CHARACTERISTICS (V_{CC} = 5V ±10%)

(Over the recommended operating conditions, unless otherwise specified.)

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I_{CC1}	V_{CC} Supply Current (Read)		1	mA	$\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}, I/O = Open, $\overline{CE}$ clocking = V_{CC} x 0.1/V_{CC} x 0.9 @ 10 MHz
I_{CC2}	V_{CC} Supply Current (Write)		2	mA	I_{CC} During Nonvolatile Write Cycle All Inputs at CMOS Levels
I_{SB1}	V_{CC} Standby Current		1	µA	$\overline{CE}$ = V_{CC}, Other Inputs = V_{CC} or V_{SS}
I_{LI}	Input Leakage Current		10	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output Leakage Current		10	µA	V_{OUT} = V_{SS} to V_{CC}
V_{IL} (1)	Input LOW Voltage	–0.5	V_{CC} x 0.3	V	
V_{IH} (1)	Input HIGH Voltage	V_{CC} x 0.7	V_{CC} + 0.5	V	
V_{OL}	Output LOW Voltage		0.4	V	I_{OL} = 2.1mA
V_{OH}	Output HIGH Voltage	V_{CC} – 0.8		V	I_{OH} = –1mA

Notes: (1) V_{IL} Min. and V_{IH} Max. are for reference only and are not tested.

D.C. OPERATING CHARACTERISTICS (V_{CC} = 2.5V to 5.5V)

(Over the recommended operating conditions, unless otherwise specified.)

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I_{CC1}	V_{CC} Supply Current (Read)		300	µA	$\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}, I/O = Open, $\overline{CE}$ clocking = V_{CC} x 0.1/V_{CC} x 0.9 @ V_{CC} = 2.5, 5 MHz
I_{CC2}	V_{CC} Supply Current (Write)		2	mA	I_{CC} During Nonvolatile Write Cycle All Inputs at CMOS Levels
I_{SB1}	V_{CC} Standby Current		1	µA	$\overline{CE}$ = V_{CC}, Other Inputs = V_{CC} or V_{SS}
I_{LI}	Input Leakage Current		10	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output Leakage Current		10	µA	V_{OUT} = V_{SS} to V_{CC}
V_{IL}(1)	Input LOW Voltage	–0.5	V_{CC} x 0.3	V	
V_{IH}(1)	Input HIGH Voltage	V_{CC} x 0.7	V_{CC} + 0.5	V	
V_{OL}	Output LOW Voltage		0.4	V	I_{OL} = 1mA, V_{CC} = 3V
V_{OH}	Output HIGH Voltage	V_{CC} – 0.4		V	I_{OH} = –400µA, V_{CC} = 3V

D.C. OPERATING CHARACTERISTICS (V_{CC} = 1.8V to 3.6V)

(Over the recommended operating conditions, unless otherwise specified.)

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I_{CC1}	V_{CC} Supply Current (Read)		200	µA	$\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}, I/O = Open, $\overline{CE}$ clocking = V_{CC} x 0.1/V_{CC} x 0.9 @ V_{CC} = 1.8V, 4 MHz
I_{CC2}	V_{CC} Supply Current (Write)		1	mA	I_{CC} During Nonvolatile Write Cycle All Inputs at CMOS Levels
I_{SB1}	V_{CC} Standby Current		1	µA	$\overline{CE}$ = V_{CC}, Other Inputs = V_{CC} or V_{SS}
I_{LI}	Input Leakage Current		10	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output Leakage Current		10	µA	V_{OUT} = V_{SS} to V_{CC}
V_{IL}(1)	Input LOW Voltage	–0.5	V_{CC} x 0.3	V	
V_{IH}(1)	Input HIGH Voltage	V_{CC} x 0.7	V_{CC} + 0.5	V	
V_{OL}	Output LOW Voltage		0.4	V	I_{OL} = 0.5mA, V_{CC} = 2V
V_{OH}	Output HIGH Voltage	V_{CC} – 0.2		V	I_{OH} = –250µA, V_{CC} = 2V

Notes: (1) V_{IL} Min. and V_{IH} Max. are for reference only and are not tested.

CAPACITANCE

T_A = +25°C, f = 1MHz, V_{CC} = 5V

Symbol	Parameter	Max.	Units	Test Conditions
$C_{I/O}$(2)	Input/Output Capacitance	8	pF	$V_{I/O}$ = 0V
C_{IN}(2)	Input Capacitance	6	pF	V_{IN} = 0V

Notes: (2) Periodically sampled, but not 100% tested.

POWER-UP TIMING

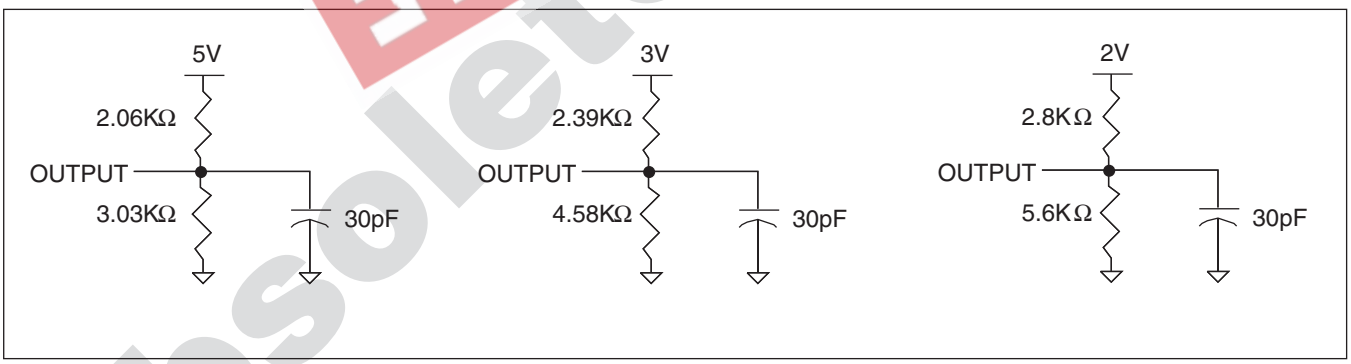
Symbol	Parameter	Max.	Units
t_{PUR}(3)	Power-up to Read Operation	2	ms
t_{PUW}(3)	Power-up to Write Operation	5	ms

Notes: (3) Time delays required from the time the V_{CC} is stable until the specific operation can be initiated. Periodically sampled, but not 100% tested.

A.C. CONDITIONS OF TEST

Input Pulse Levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input Rise and Fall Times	5ns
Input and Output Timing Levels	V_{CC} x 0.5

EQUIVALENT A.C. LOAD CIRCUITS



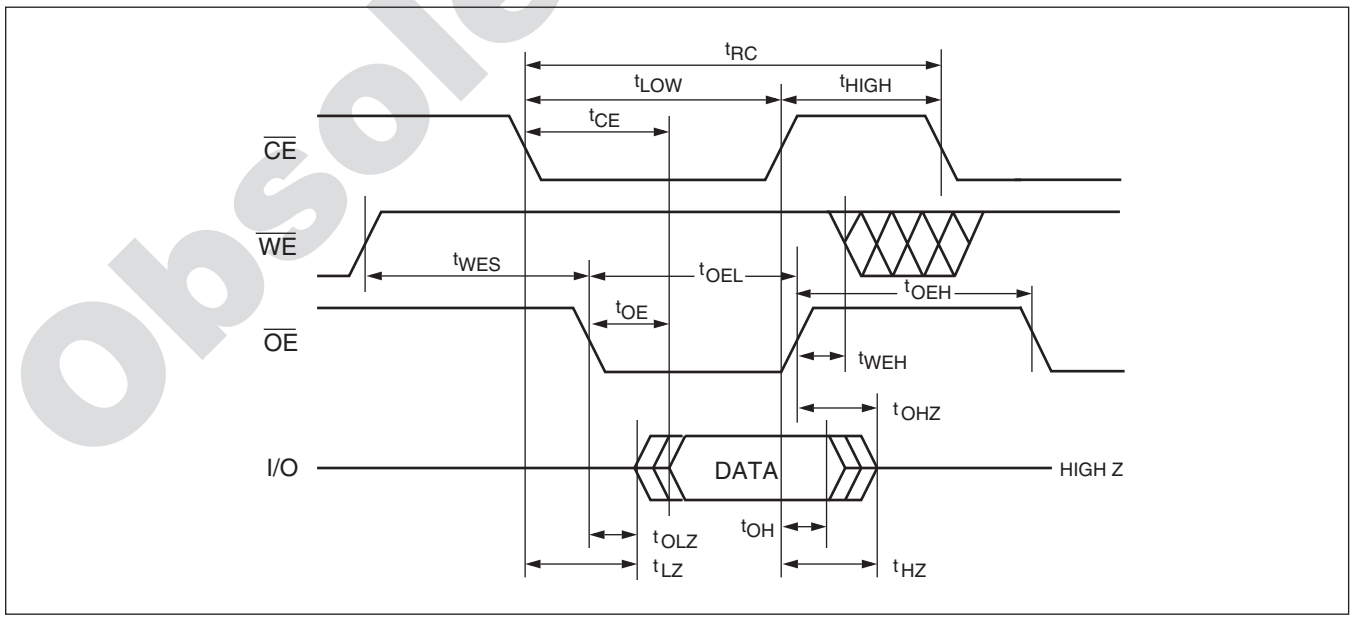
A.C. CHARACTERISTICS

(Over the recommended operating conditions, unless otherwise specified.)

Read Cycle Limits – X84160/640/128

Symbol	Parameter	V_{CC} = 4.5V – 5.5V		V_{CC} = 2.5V – 5.5V		V_{CC} = 1.8V – 3.6V		Units
		Min.	Max	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	70		125		250		ns
t_{CE}	$\overline{CE}$ Access Time		20		25		70	ns
t_{OE}	$\overline{OE}$ Access Time		20		25		70	ns
t_{OEL}	$\overline{OE}$ Pulse Width	20		35		70		ns
t_{OEH}	$\overline{OE}$ High Recovery Time	50		90		180		ns
t_{LOW}	$\overline{CE}$ LOW Time	20		35		70		ns
t_{HIGH}	$\overline{CE}$ HIGH Time	50		90		180		ns
t_{LZ}(4)	$\overline{CE}$ LOW to Output In Low Z	0		0		0		ns
t_{HZ}(4)	$\overline{CE}$ HIGH to Output In High Z	0	15	0	25	0	30	ns
t_{OLZ}(4)	$\overline{OE}$ LOW to Output In Low Z	0		0		0		ns
t_{OHZ}(4)	$\overline{OE}$ HIGH to Output In High Z	0	15	0	25	0	30	ns
t_{OH}	Output Hold from $\overline{CE}$ or $\overline{OE}$ HIGH	0		0		0		ns
t_{WES}	$\overline{WE}$ HIGH Setup Time	25		25		25		ns
t_{WEH}	$\overline{WE}$ HIGH Hold Time	25		25		25		ns

Notes: (4) Periodically sampled, but not 100% tested. t_{HZ} and t_{OHZ} are measured from the point where $\overline{CE}$ or $\overline{OE}$ goes HIGH (whichever occurs first) to the time when I/O is no longer being driven into a 5pF load.



Write Cycle Limits – X84160/640/128

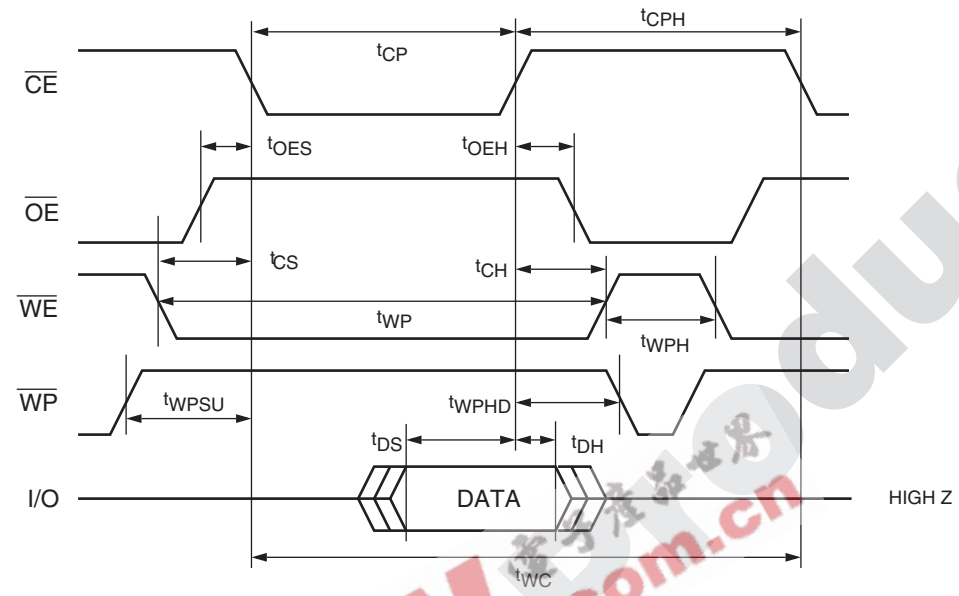
Symbol	Parameter	V_{CC} = 4.5V – 5.5V		V_{CC} = 2.5V – 5.5V		V_{CC} = 1.8V – 3.6V		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{NVWC}(5)	Nonvolatile Write Cycle Time		5		5		5	ms
t_{WC}	Write Cycle Time	70		125		250		ns
t_{WP}	$\overline{WE}$ Pulse Width	20		35		50		ns
t_{WPH}	$\overline{WE}$ HIGH Recovery Time	50		90		180		ns
t_{CS}	Write Setup Time	0		0		0		ns
t_{CH}	Write Hold Time	0		0		0		ns
t_{CP}	$\overline{CE}$ Pulse Width	20		35		70		ns
t_{CPH}	$\overline{CE}$ HIGH Recovery Time	50		90		180		ns
t_{OES}	$\overline{OE}$ HIGH Setup Time	25		25		50		ns
t_{OEH}	$\overline{OE}$ HIGH Hold Time	25		25		50		ns
t_{DS}(6)	Data Setup Time	12		20		30		ns
t_{DH}(6)	Data Hold Time	5		5		5		ns
t_{WPSU}(7)	$\overline{WP}$ HIGH Setup	100		100		150		ns
t_{WPHD}(7)	$\overline{WP}$ HIGH Hold	100		100		150		ns

Notes: (5) t_{NVWC} is the time from the falling edge of $\overline{OE}$ or $\overline{CE}$ (whichever occurs last) of the second read cycle in the “start nonvolatile write cycle” sequence until the self-timed, internal nonvolatile write cycle is completed.

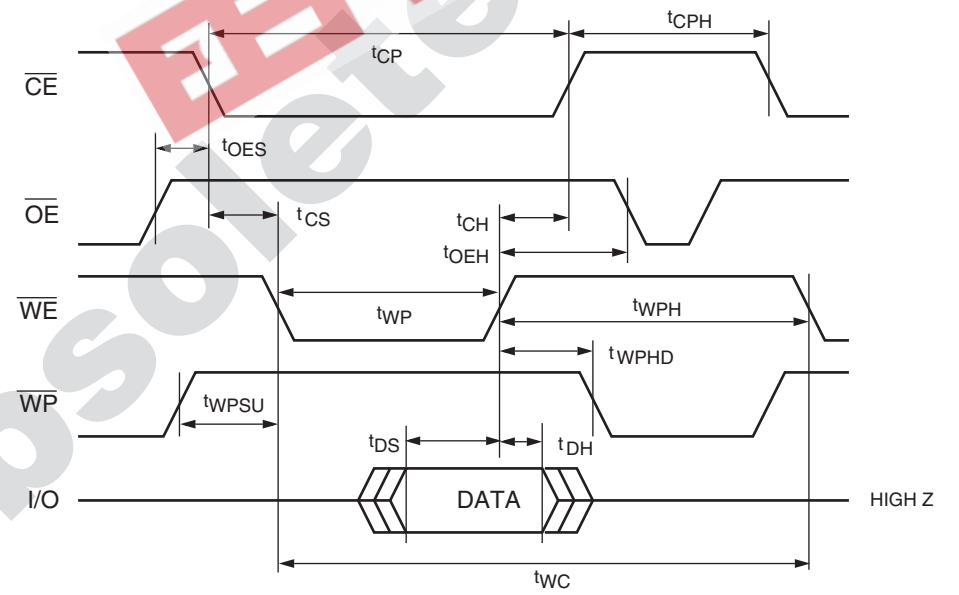
(6) Data is latched into the X84160/640/128 on the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs first.

(7) Periodically sampled, but not 100% tested.

$\overline{CE}$ Controlled Write Cycle

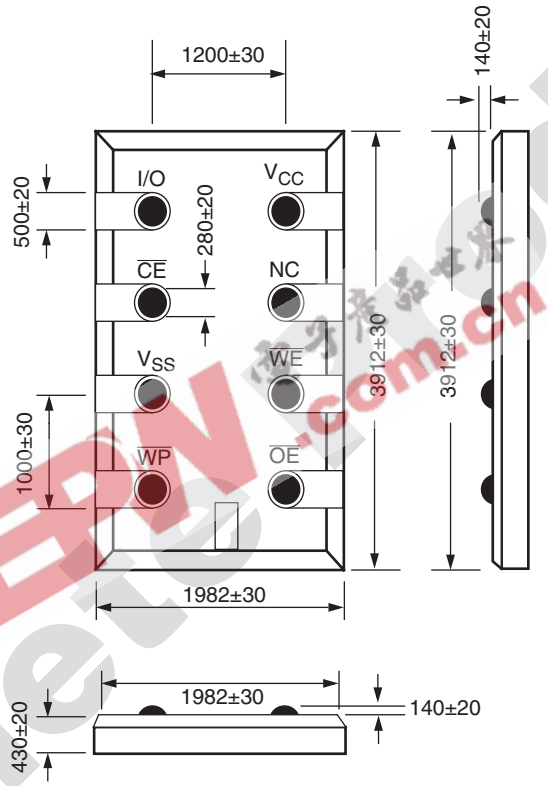


$\overline{WE}$ Controlled Write Cycle



8-LEAD XBGA TYPE

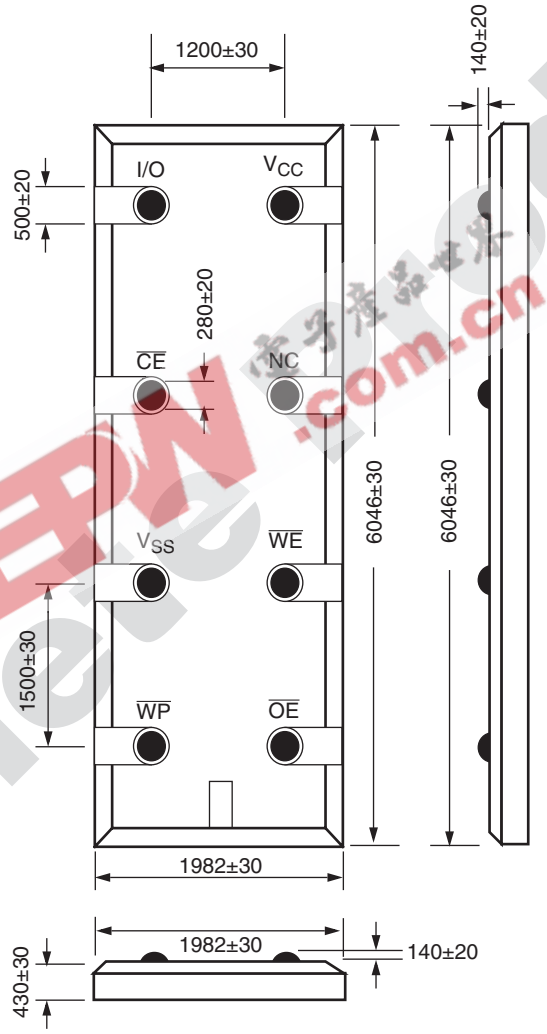
X84640Z: Bottom View



NOTE: ALL DIMENSIONS IN µM
ALL DIMENSIONS ARE TYPICAL VALUES

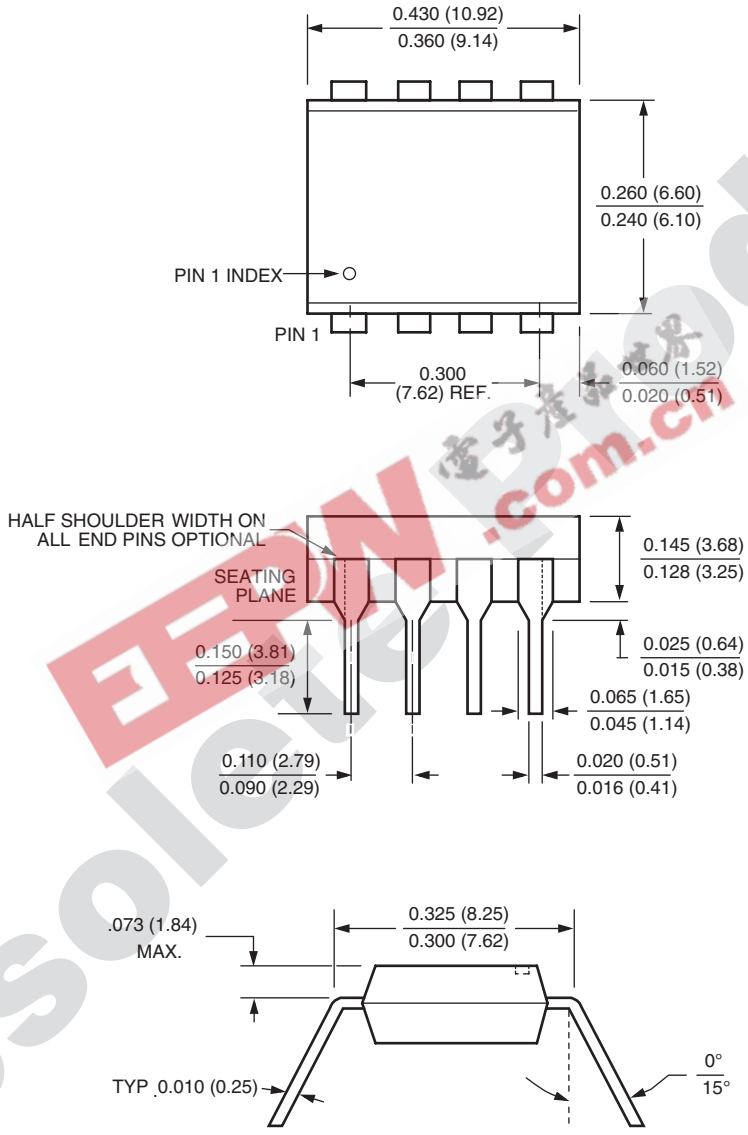
8-LEAD XBGA TYPE

X84128: Bottom View



NOTE: ALL DIMENSIONS IN µM
ALL DIMENSIONS ARE TYPICAL VALUES

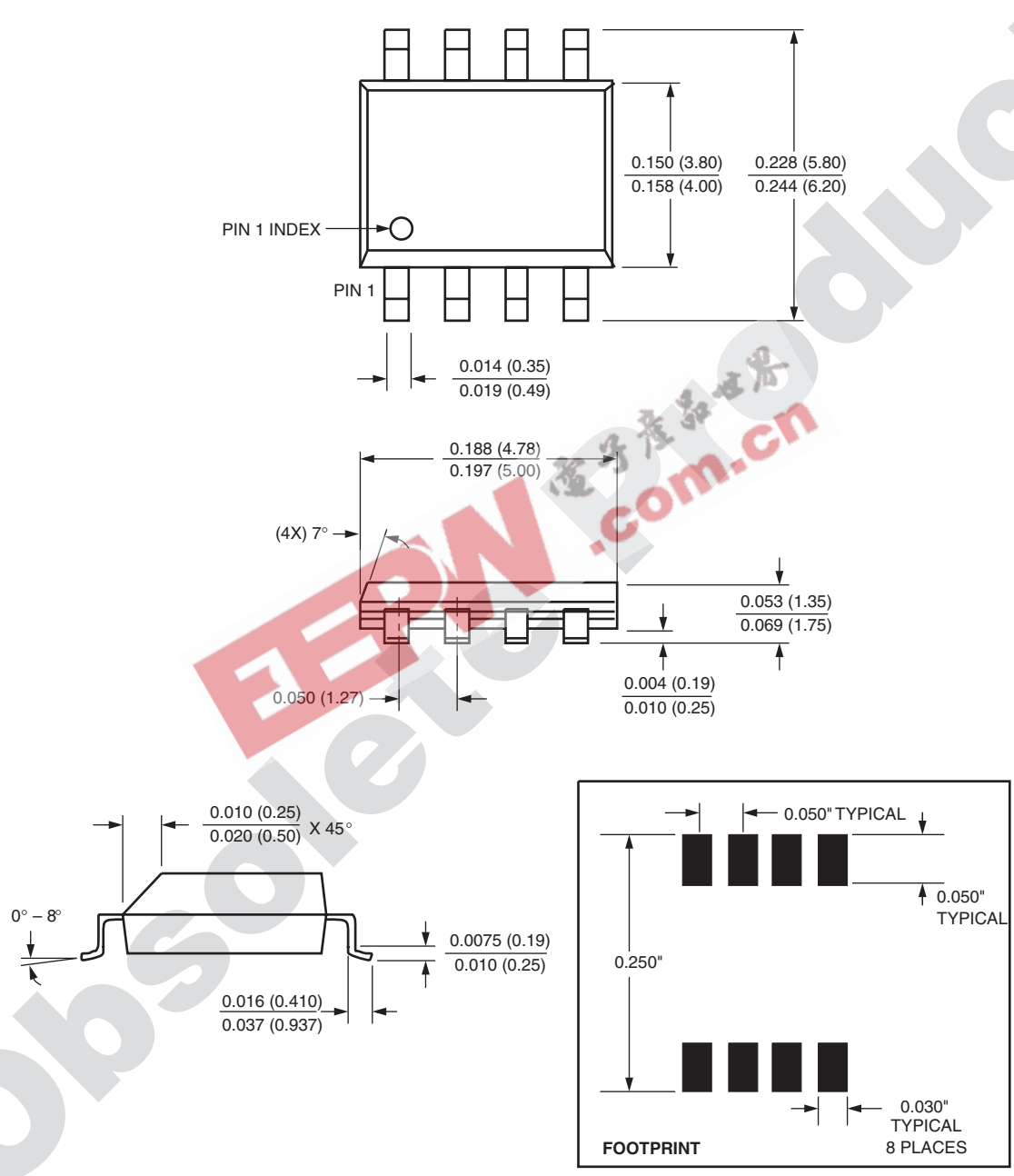
8-LEAD PLASTIC DUAL IN-LINE PACKAGE TYPE P



NOTE:

1. **ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)**
2. **PACKAGE DIMENSIONS EXCLUDE MOLDING FLASH**

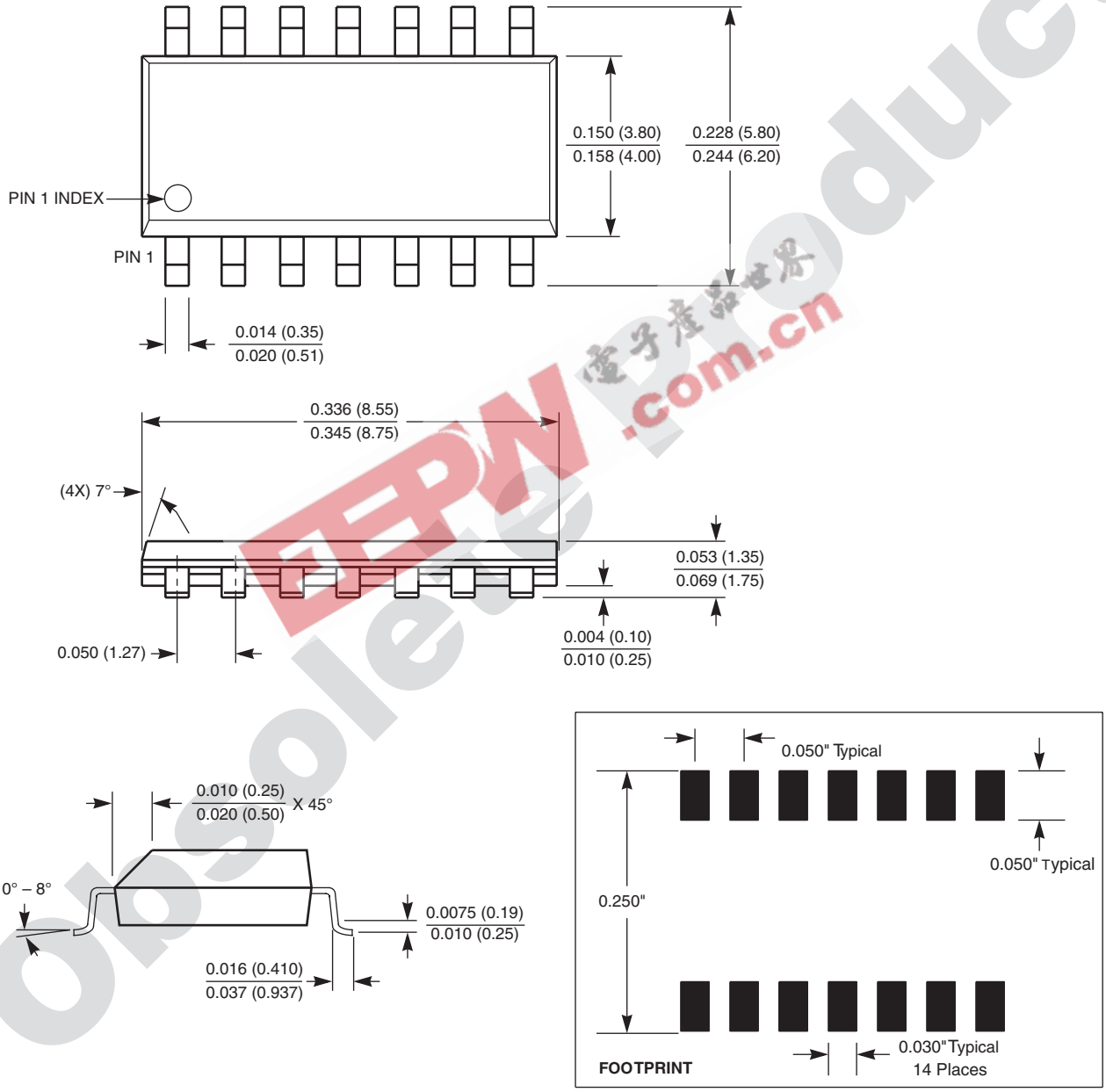
8-LEAD PLASTIC SMALL OUTLINE GULL WING PACKAGE TYPE S



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

PACKAGING INFORMATION

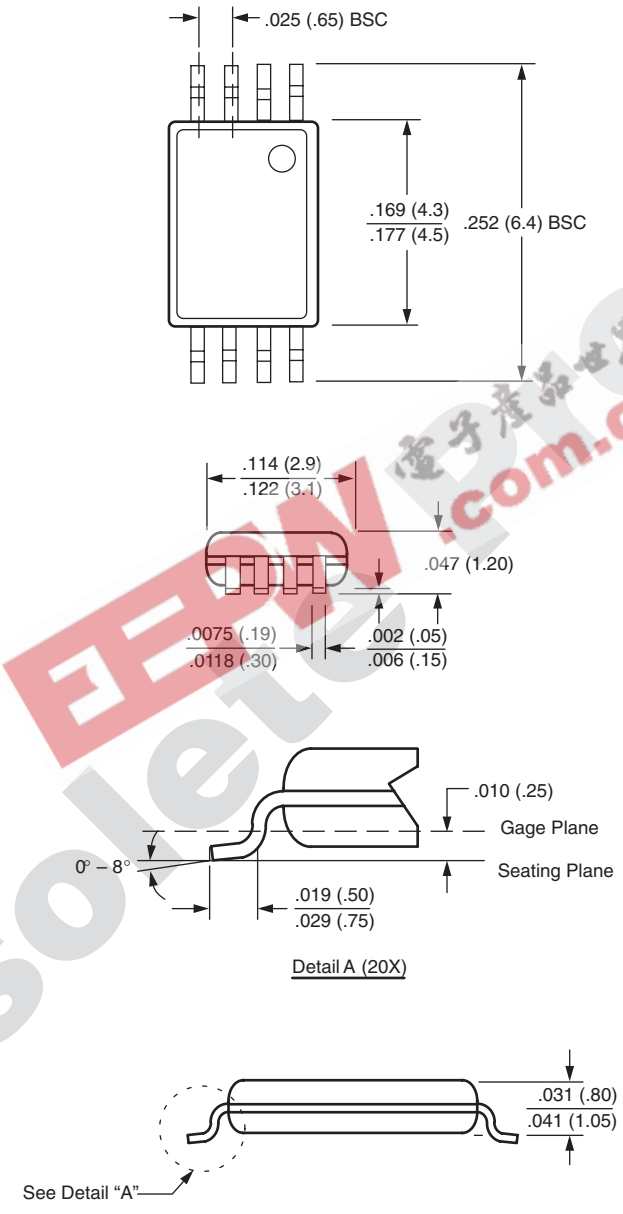
14-LEAD PLASTIC SMALL OUTLINE GULL WING PACKAGE TYPE S



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

PACKAGING INFORMATION

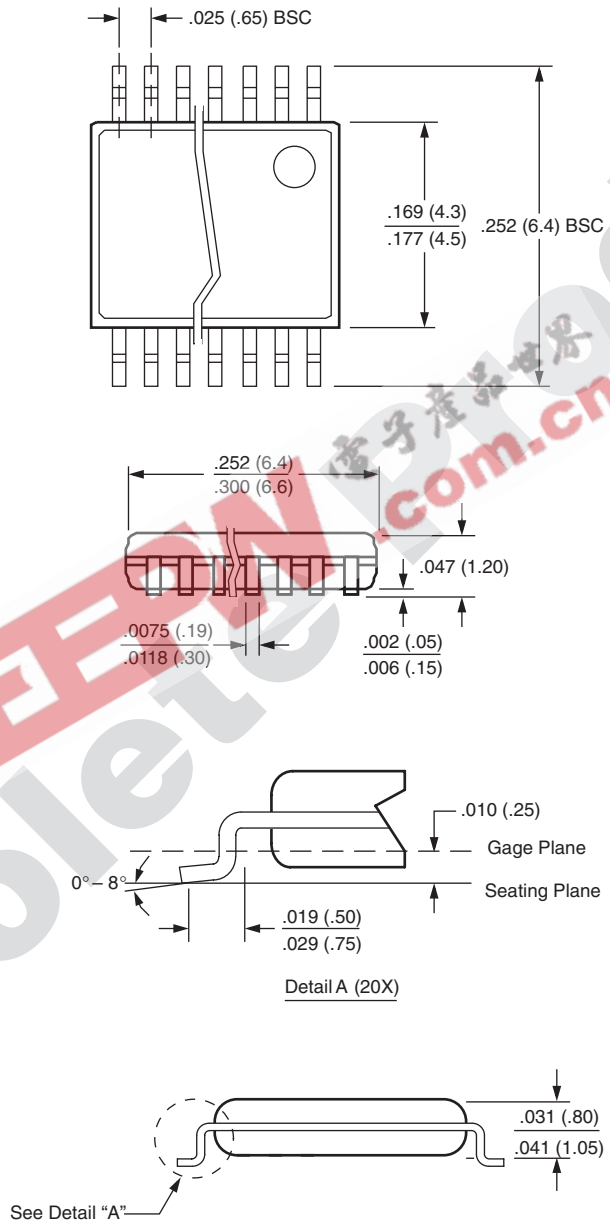
8-LEAD PLASTIC, TSSOP, PACKAGE TYPE V



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

PACKAGING INFORMATION

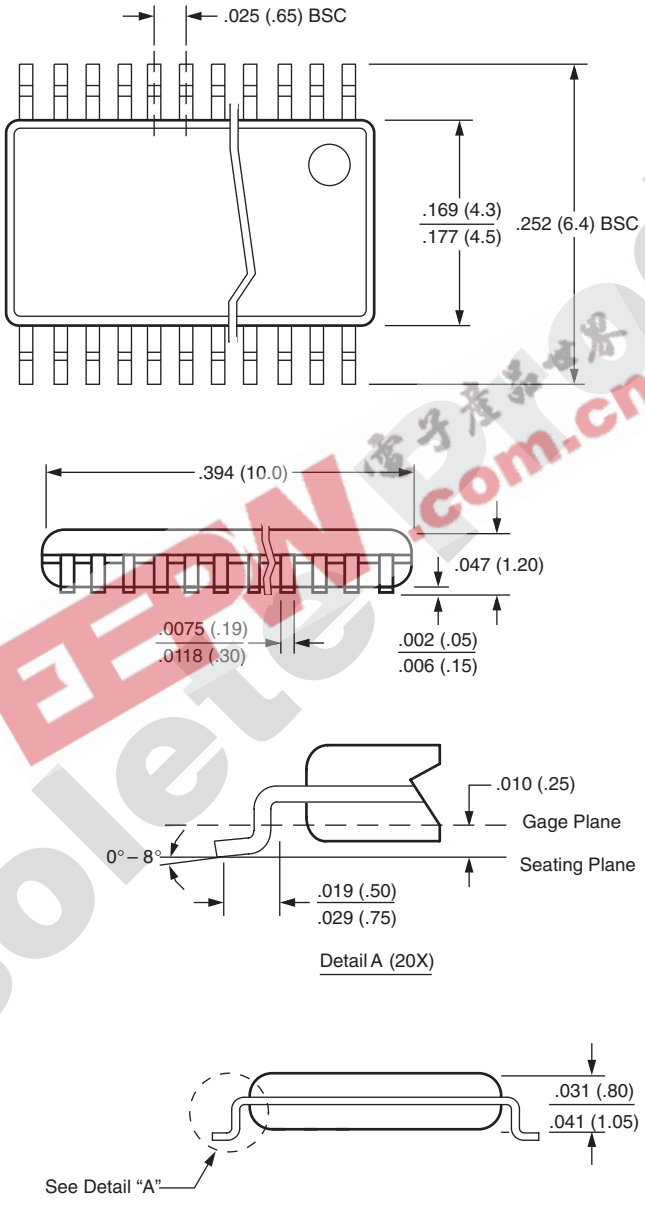
20-LEAD PLASTIC, TSSOP PACKAGE TYPE V



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

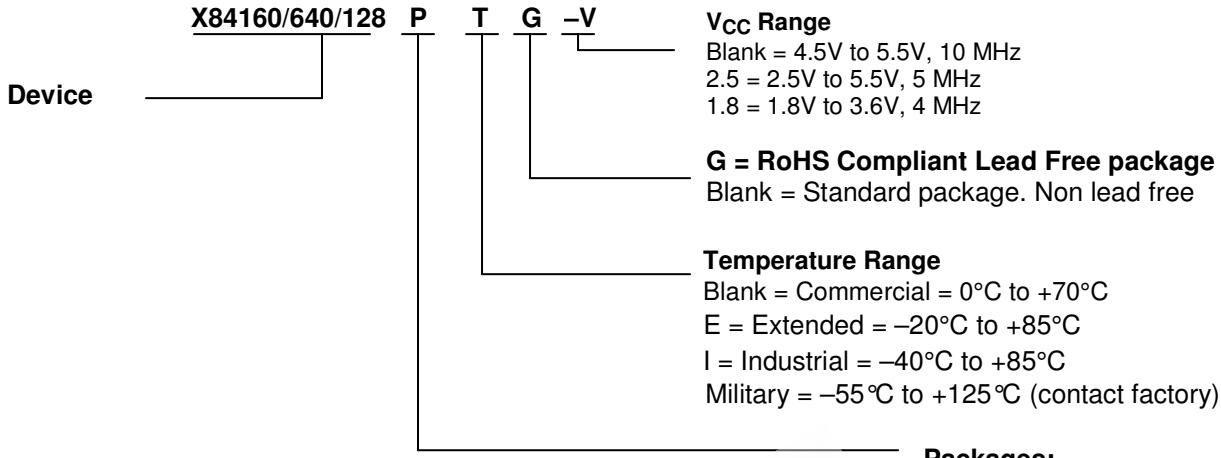
PACKAGING INFORMATION

28-LEAD PLASTIC, TSSOP PACKAGE TYPE V



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

ORDERING INFORMATION



Packages:

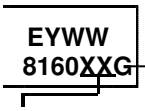
X84160
P = 8-Lead PDIP
S8 = 8-Lead SOIC
V8 = 8-Lead TSSOP

X84640
P = 8-Lead PDIP
S8 = 8-Lead SOIC
V20 = 20-Lead TSSOP
Z = 8-Lead XBGA

X84128
P = 8-Lead PDIP
S14 = 14-Lead SOIC
V28 = 28-Lead TSSOP
Z = 8-Lead XBGA

*PART MARK CONVENTION

8-Lead TSSOP



AG = 1.8 to 3.6V, 0 to +70°C
AH = 1.8 to 3.6V, -40 to +85°C
F = 2.5 to 5.5V, 0 to +70°C
G = 2.5 to 5.5V, -40 to +85°C
Blank = 4.5 to 5.5V, 0 to +70°C
I = 4.5 to 5.5V, -40 to +85°C

8-Lead SOIC/PDIP

AG = 1.8 to 3.6V, 0 to +70°C
AH = 1.8 to 3.6V, -40 to +85°C
F = 2.5 to 5.5V, 0 to +70°C
G = 2.5 to 5.5V, -40 to +85°C
Blank = 4.5 to 5.5V, 0 to +70°C
I = 4.5 to 5.5V, -40 to +85°C

8-Lead XBGA PACKAGE

Complete Part Number	Top Mark
X84640ZE-2.5	XAP
X84640ZI-2.5	XAR
X84128ZE-2.5	XAN
X84128 ZI-2.5	XAO

*All parts and package types not included will receive standard marking.

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.