YAMAHA LSI

YSS231

GE

Graphic Equalizer

■OUTLINE

The YSS231 is an LSI which performs filtering required by equalizers, etc. It is capable of implementing functions such as de-emphasis, sound multiplex processing, voice cancel, and equalizing.

Filtering through digital signal processing, this LSI can obtain various filtering characteristics by entering coefficient values from the microprocessor.

■FEATURES

- Processing digital data with a sampling frequency of 32k to 48kHz.
- Two operation modes to meet the usage required.
- The center frequency, gain, and Q for the equalizer can be set at your option.
- High-speed multiplier, 24 bit data × 18 bit coefficient value = 30 bit data.
- The digital input/output format of 16 bits or 18 bits is selectable in stereo mode.
- Zero cross mute function which permits selection of four kinds of border value levels.
- Easy setting of commands and coefficient values by the microprocessor interface.
- Master clock of 256fs or 384fs.
- 5V or 3.3V single power supply, Si-gate CMOS process.
- This package is

  16-pin plastic DIP (YSS231-D)

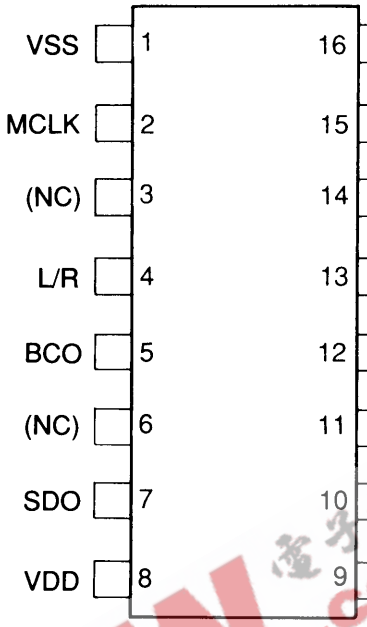
  16-pin plastic SOP (YSS231-M)

  20-pin plastic SSOP (YSS231-E)

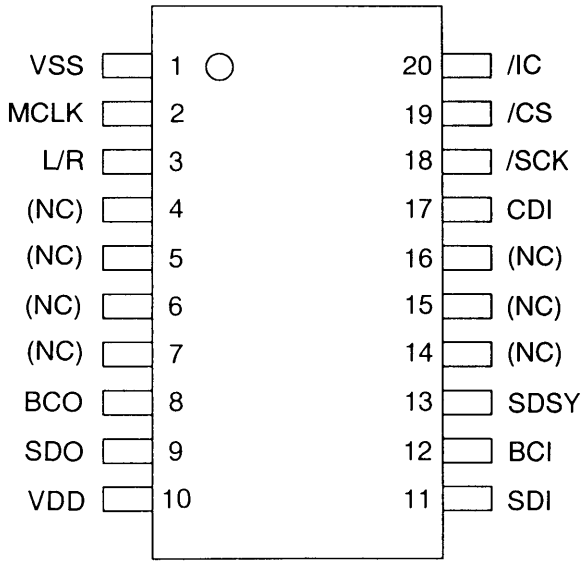
YAMAHA CORPORATION

YSS231 CATALOG
CATALOG No. : -LSI 4SS231A3
1995. 12

■PIN CONFIGURATION



<Top View Common to 16-pin DIP and 16-pin SOP>

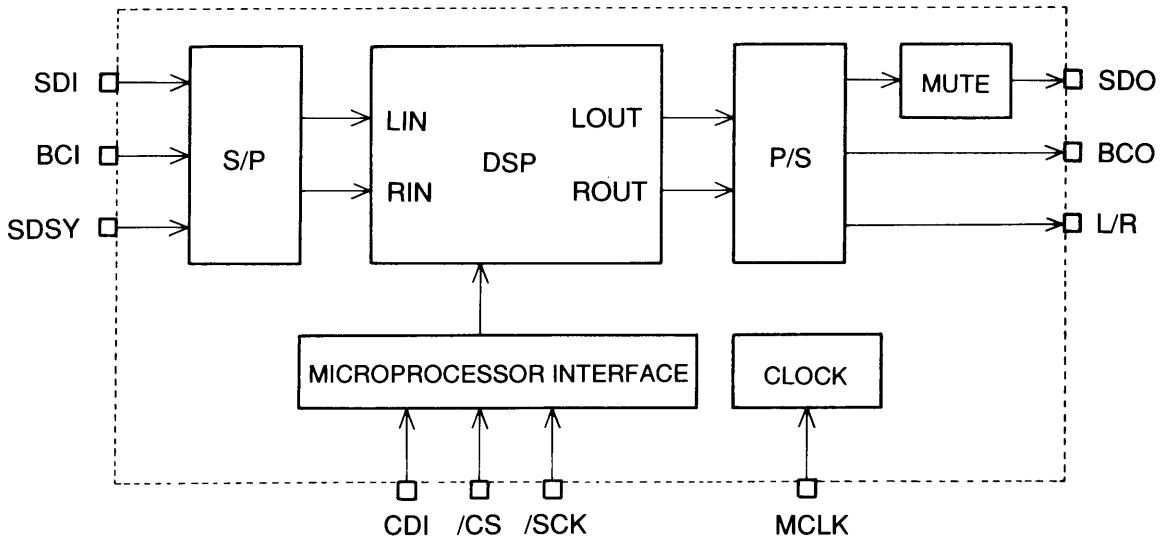


<20pin SSOP Top View>

■PIN FUNCTION

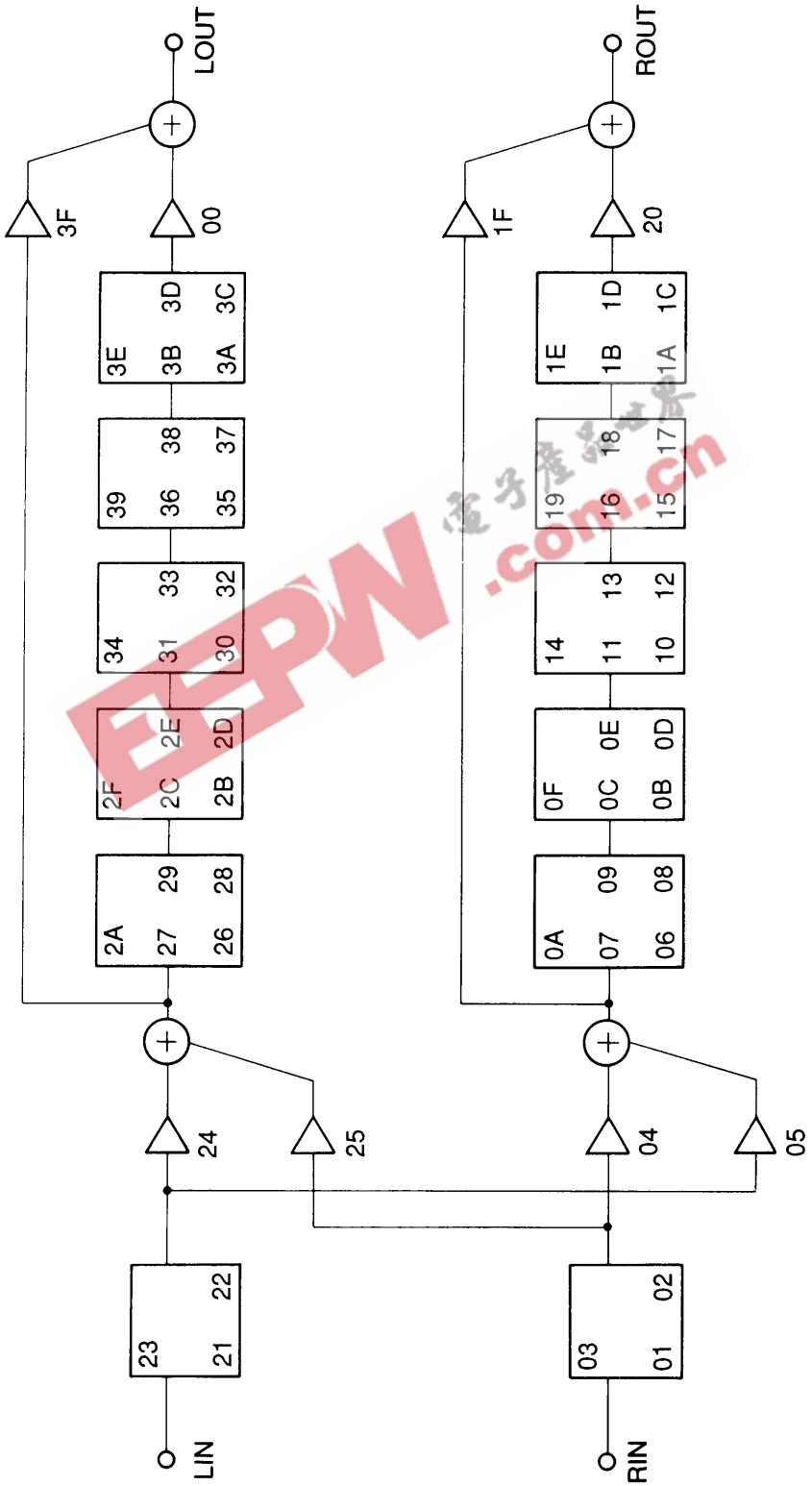
No.		Name	I/O	Function
DIP,SOP	SSOP			
1	1	VSS	-	Ground
2	2	MCLK	I	Clock input
4	3	L/R	O	Digital audio signal output Word clock
5	8	BCO	O	Digital audio signal output Bit clock
7	9	SDO	O	Digital audio signal output Serial clock
8	10	VDD	-	Power supply
9	11	SDI	I	Digital audio signal input Serial data
10	12	BCI	I	Digital audio signal input Bit clock
12	13	SDSY	I	Digital audio signal input Word clock
13	17	CDI	I	Microprocessor interface Serial data
14	18	/SCK	I	Microprocessor interface Serial clock
15	19	/CS	I	Microprocessor interface Chip select
16	20	/IC	I	Initial clear input

■BLOCK DIAGRAM

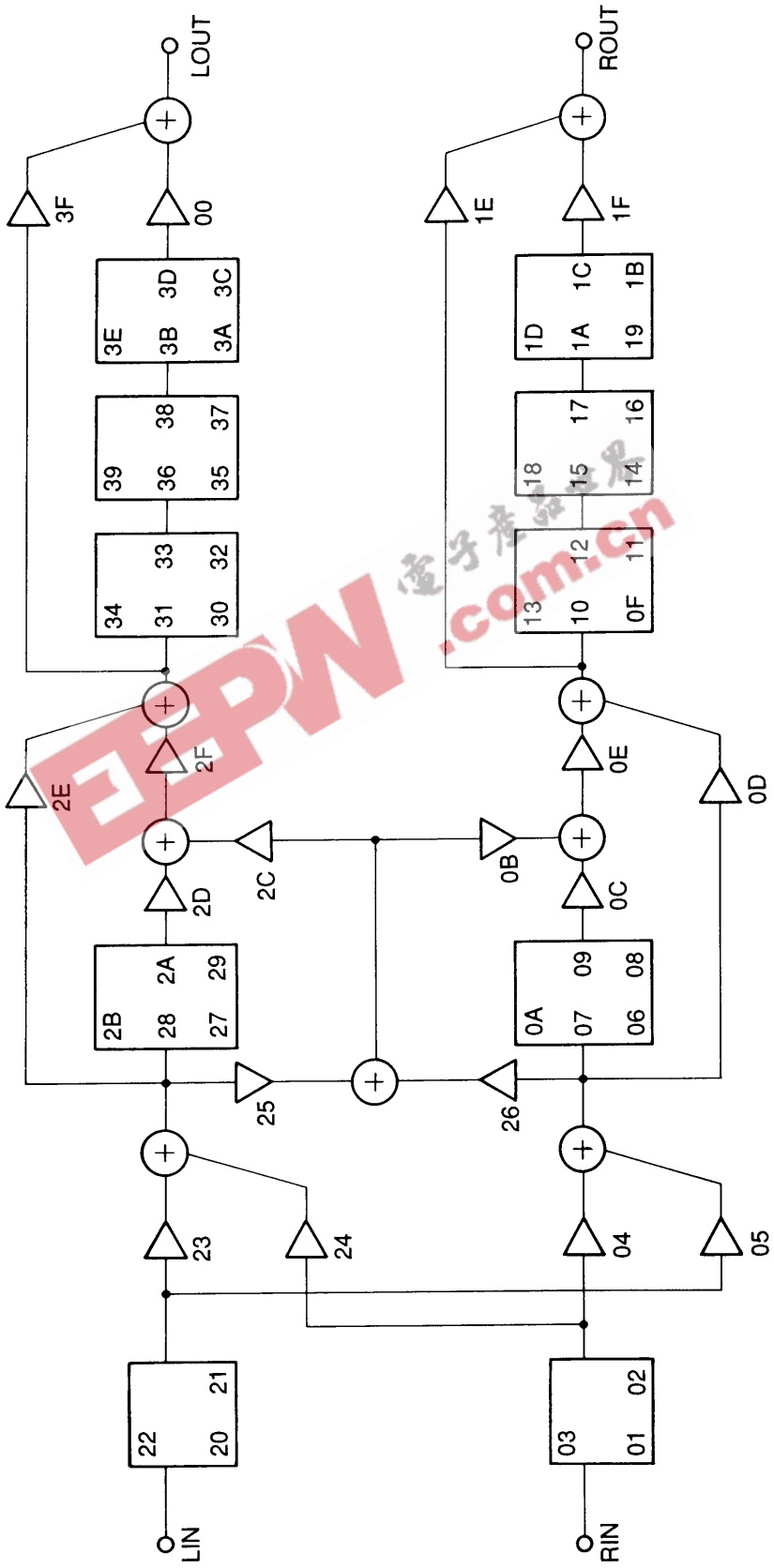


■SIGNAL FLOW DIAGRAM

1. Mode 1 (De-emphasis + Sound Multiplex Processing + 5-band Equalizer)



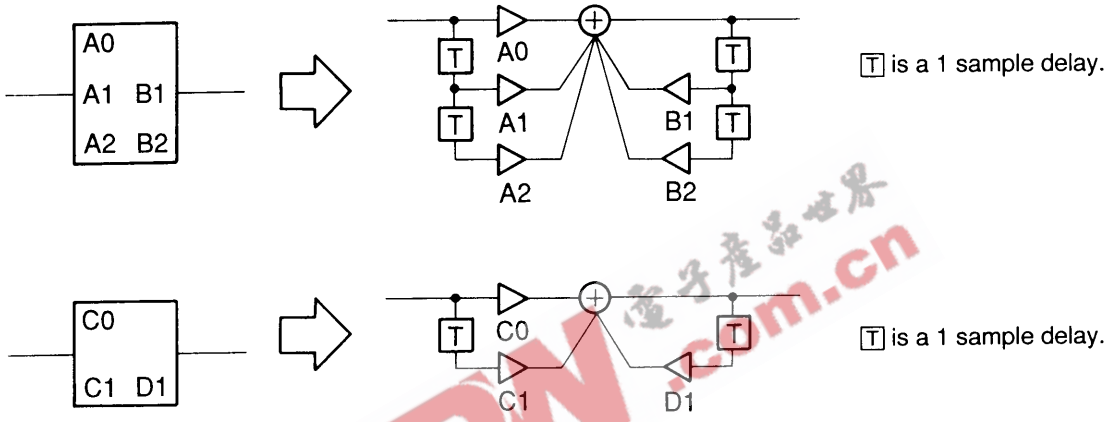
2. Mode 2 (De-emphasis + Sound Multiplex Processing + Voice Cancel + 3-band Equalizer)



3. Notes on Signal Flow Diagram

● IIR Filter

In the signal flow diagram, a 2nd order IIR filter is represented as a box with five coefficient addresses, and a 1st order IIR filter as a box with three coefficient addresses.



IMPORTANT:

After setting the coefficients, the YSS231 quadruples the coefficient values of coefficient addresses A0 and A2 of the 2nd order IIR filter and also doubles the coefficient values of A1, B1, and B2. Therefore, the coefficients of A0 and A2 must be divided by four, and the coefficients of A1, B1, and B2 by two, before entering the coefficients from the microprocessor.

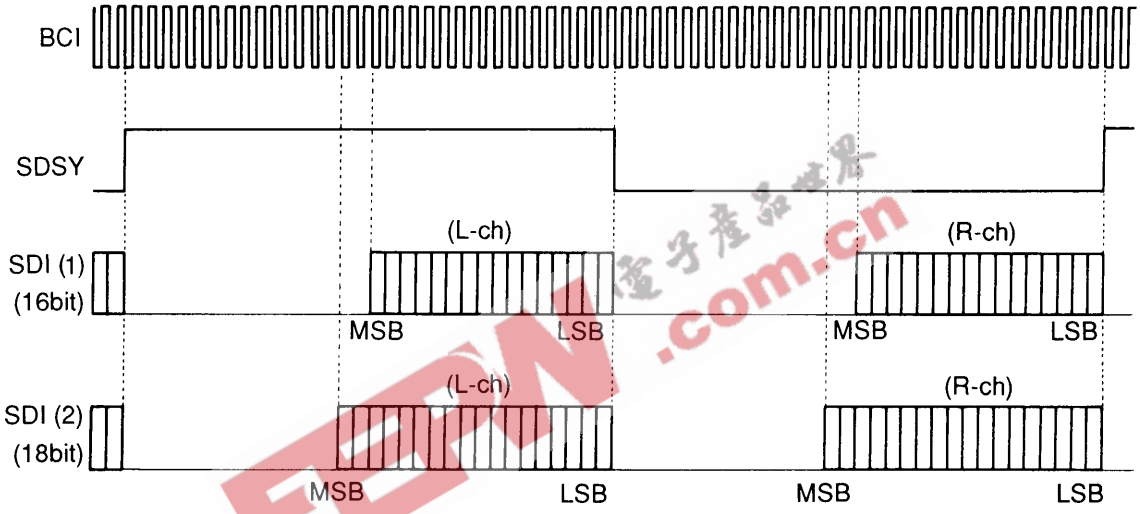
■FUNCTION DESCRIPTION

1. Master clock MCLK

An external clock of 384fs or 256fs is inputted through the MCLK terminal.
After /IC raise, CLK bit of the OPR register is set "0", and master clock moves 384fs. If 256fs is used at MCLK frequency, set "1" to CLK bit of OPR register after /IC raise.

2. Data input/output SDI, BCI, SDSY, SDO, BCO, L/R

Digital audio signal input format



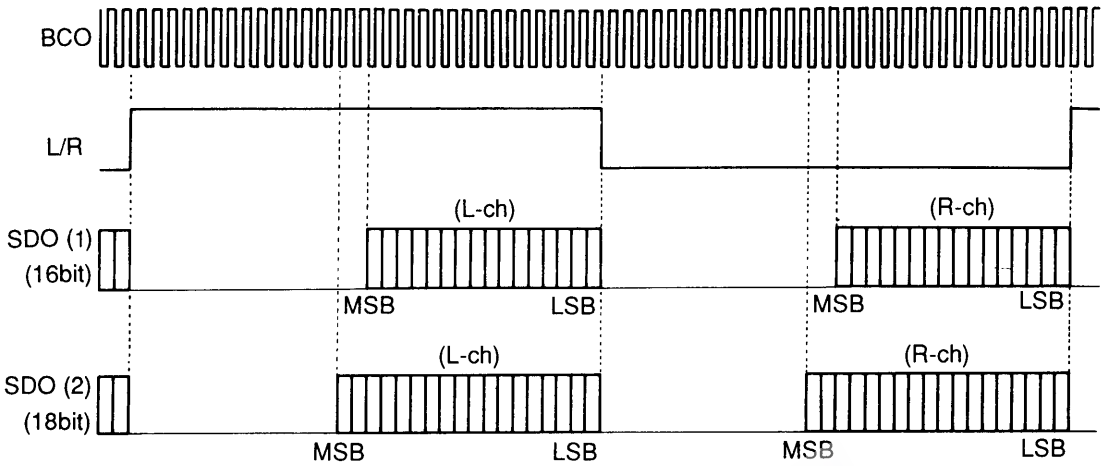
Each format data for digital audio signal is input to the BCI, SDSY and SDI terminal.

From power on to down, input the signal of sampling frequency to the SDSY terminal.
If one cycle of SDSY is shifted 1/32fs or more to sampling frequency, internal coefficient data is destroyed. When this condition happened, set the coefficient register again.

From power on to down, input the clock frequency of decided range to the BCI terminal.
When the input data is 16 bit (OPR register, IN bit = "0"), the frequency range of the BCI is 32fs~192fs, and the when 18 bit (OPR register, IN bit "1"), 36fs~192fs.

The digital audio signal input 16 or 18 bit to the SDI terminal. Set to IN bit of OPR register by the microprocessor.

Digital audio signal output format



Each format data for digital audio signal is output from the BCO, L/R and SDO terminal.

The digital audio signal output 16 or 18 bit to the SDO terminal. Set to OUT bit of OPR register by the mocroprocessor.

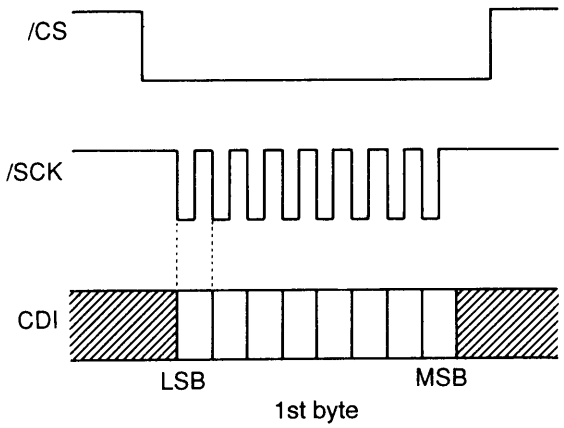
3. Initial clear /IC

This LSI requires initial clear when the power is turned on.
The time taken for initial clear is at least 5/fs (fs: sampling frequency). The preservation of coefficient values is not guaranteed after initial clear.

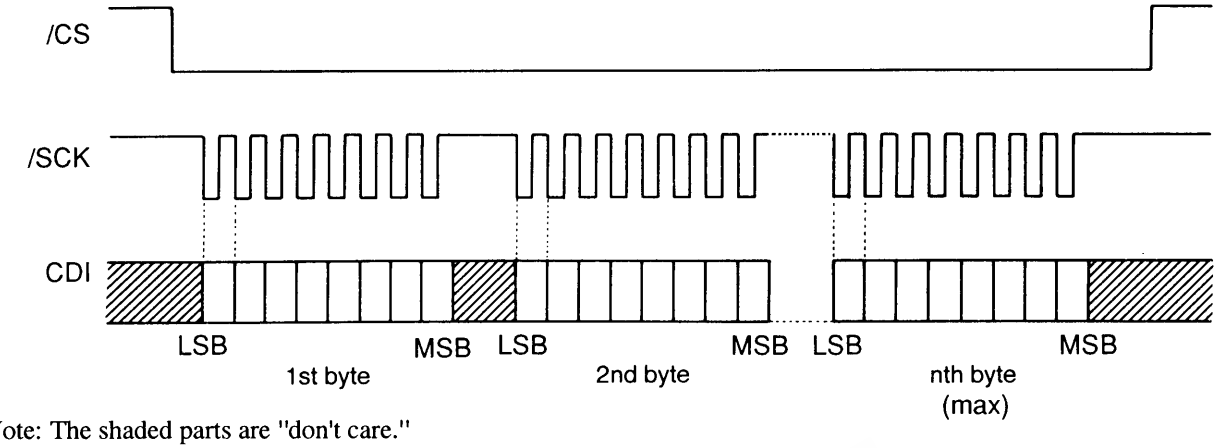
4. Microprocessor interface CDI, /SCK, /CS

4.1 Command write timing

● 1-byte command



● 4- to 16-byte command



Note: The shaded parts are "don't care."

4.2 Command map

Commands each are classified by the upper 2 bits of the first byte.

Command	Name	No. of bytes	Function
00XXXXXX	OPR	1	Operation control register
01XXXXXX	TEST	1	Test register (Do not write usually)
10XXXXXX	MUTE	1	Mute control register
11XXXXXX	ADRS	4～16	Write the coefficient values of each filter, etc. by 4 to 16 bytes.*

*Note: Up to five coefficient values can be transferred at a time.

4.3 Explanation of commands

(a) OPR (Operation control register)

MSB	B6	B5	B4	B3	B2	B1	LSB
0	0	TEST	MUTE	PROG	OUT	IN	CLK

Note: B5 to LSB are set to "0" at initial clear.

● TEST: For LSI test
Usually set to "0".

● MUTE: Mute setting
0 = Mute ON
1 = Mute OFF

● PROG: Selection of operation mode
0 = Mode 1
1 = Mode 2

● OUT: Selection of output bit
0 = 16 bits
1 = 18 bits

● IN: Selection of input bit
0 = 16 bits
1 = 18 bits

● CLK: Selection of master clock
0 = 384 fs
1 = 256 fs

(b) MUTE (Mute control register)

MSB	B6	B5	B4	B3	B2	B1	LSB
1	0	LVL2	LVL1	D3	D2	D1	D0

Note: B5 to LSB are set to "0" at initial clear.

● LVL2, LVL1: Mute border value

Muting takes place when the audio data drops below each border value.
Muting is performed independently for each of L and R.

B5	B4	Border value
LVL2	LVL1	
0	0	−30dB
0	1	−36dB
1	0	−42dB
1	1	−48dB

● D3, D2, D1, D0: Maximum time taken before muting

Muting is performed forcibly if the audio data does not drop below the border value programmed by LVL2 or LVL1 even if the mute function is turned ON.
Mute time = (D3 * 8 + D2 * 4 + D1 * 2 + D0) * 2048 * (sampling cycle)
Muting takes place immediately when D3 = D2 = D1 = D0 = 0.

(c) ADRS

Maximum 5 coefficient values can be transferred at one time. When 2 or more coefficient values is transferred at one time, the coefficient values should be transferred from the lower address.

When transferring n (1 to 5) coefficient value(s) at a time, (3＊n＋1) bytes should be transferred with the first byte at the top, as shown below.

MSB	B6	B5	B4	B3	B2	B1	LSB
1	1	0	0	0	0	0	0

1st byte

MSB	B6	B5	B4	B3	B2	B1	LSB
D1	D0	A5	A4	A3	A2	A1	A0

2nd byte
(5th byte)
(8th byte)
(11th byte)
(14th byte)

MSB	B6	B5	B4	B3	B2	B1	LSB
D9	D8	D7	D6	D5	D4	D3	D2

3rd byte
(6th byte)
(9th byte)
(12th byte)
(15th byte)

MSB	B6	B5	B4	B3	B2	B1	LSB
D17	D16	D15	D14	D13	D12	D11	D10

4th byte
(7th byte)
(10th byte)
(13th byte)
(16th byte)

● A5～A0：Coefficient address

The coefficient address is set by the lower 6 bits of (3n-1)th byte.
The filter for equalizing consists of the 2nd order IIR filter. And it is necessary to set 5 coefficient values for one filter.
The filter for de-emphasis consists of the 1st order IIR filter. And it is necessary to set 3 coefficient values for one filter.

● D17～D0：Coefficient value

The coefficient value is set from D17 to D0 formed by 18 bits and 2's complement.
D17 is the sign bit.

$$\text{Coefficient value} = (-1) \times D17 + \sum_{n=0}^{16} Dn \times 2^{n-17}$$

■ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Power supply voltage	V_{DD}	-0.3～7.0	V
Input voltage	V_I	-0.3～V_{DD}+0.3	V
Operating temperature	T_{op}	-40～85	℃
Storage temperature	T_{stg}	-50～125	℃

2. Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	V_{DD}	3.0	5.0	5.5	V
Operating temperature	T_{op}	0	25	70	℃

3. DC Characteristics

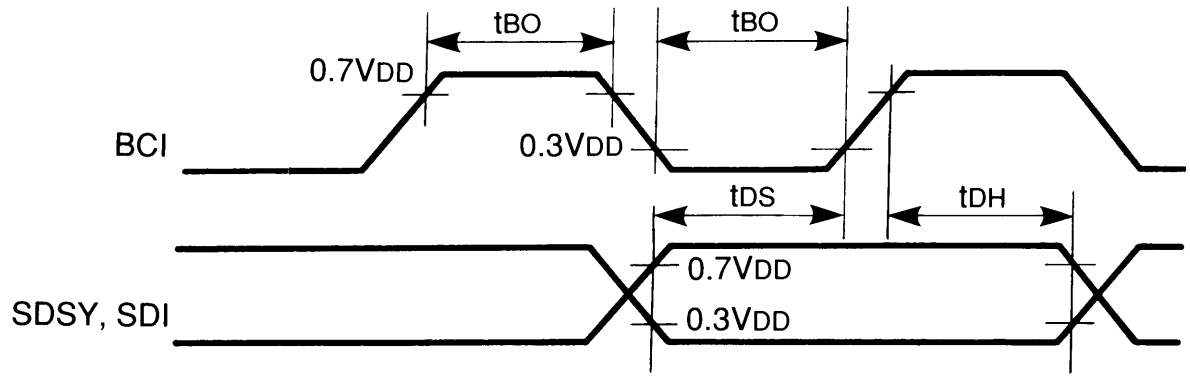
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input voltage H level	V_{IH}		0.7V_{DD}			V
Input voltage L level	V_{IL}				0.3V_{DD}	V
Output voltage H level	V_{OH}	I_{OH}=0.25mA	0.8V_{DD}			V
Output voltage L level	V_{OL}	I_{OL}=1.0mA			0.4	V
Input leakage current	I_{LI}		-10		10	μA
Power dissipation	P_D	V_{DD}=5.0V		20	70	mW
		V_{DD}=3.3V		10	30	

4. AC Characteristics

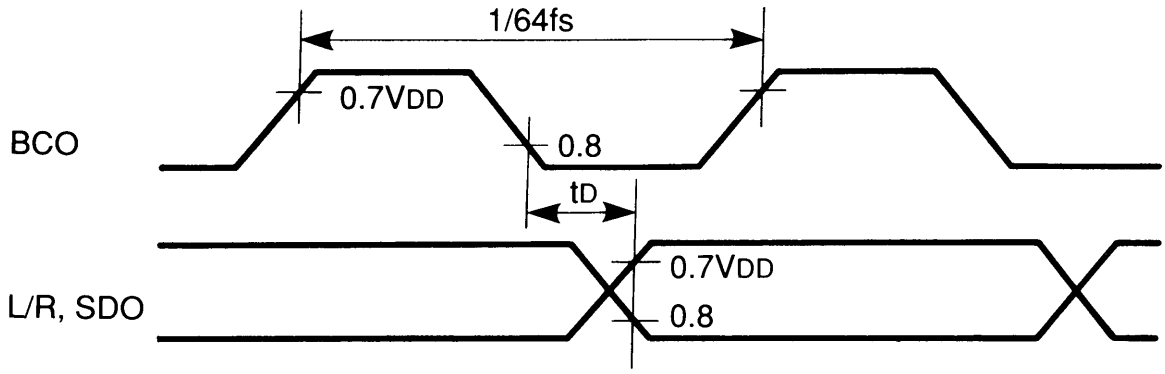
	Parameter	Symbol	Min.	Typ.	Max.	Unit
MCLK	Input frequency	f_{C1} (*1)	8.0		12.5	MHz
		f_{C2} (*2)	12.0		18.5	MHz
	Duty	R_C	40	50	60	%
BCI	ON/OFF time	t_{BO}	40			ns
SDSY, SDI	Setup time	t_{DS}	20			ns
	Hold time	t_{DH}	20			ns
L/R, SD0	Acess time	t_D	-40		40	ns
/CS	Setup time (1)	t_{CS1} (*3)	1/100fs			s
	Setup time (2)	t_{CS2} (*4)	1/65fs			s
	H level time	t_{HT}	131/64fs			s
/SCK	ON/OFF time (1)	t_{SO1} (*3)	1/50fs			s
	ON/OFF time (2)	t_{SO2} (*4)	1/32fs			s
	Transition time (1)	t_{CT1} (*3)			1/64fs	s
	Transition time (2)	t_{CT2} (*4)			1/42fs	s
CDI	Setup time (1)	t_{SS1} (*3)	1/100fs			s
	Setup time (2)	t_{SS2} (*4)	1/65fs			s
	Hold time (1)	t_{SH1} (*3)	1/100fs			s
	Hold time (2)	t_{SH2} (*4)	1/65fs			s
/IC	Pulse width	t_{ICW}	5/fs			s

(*1) While master clock is 256fs.
(*2) While master clock is 384fs.
(*3) Nomally operation.
(*4) The characteristics while the "1" is set to LSB in OPR register on the master clock 256fs operation.

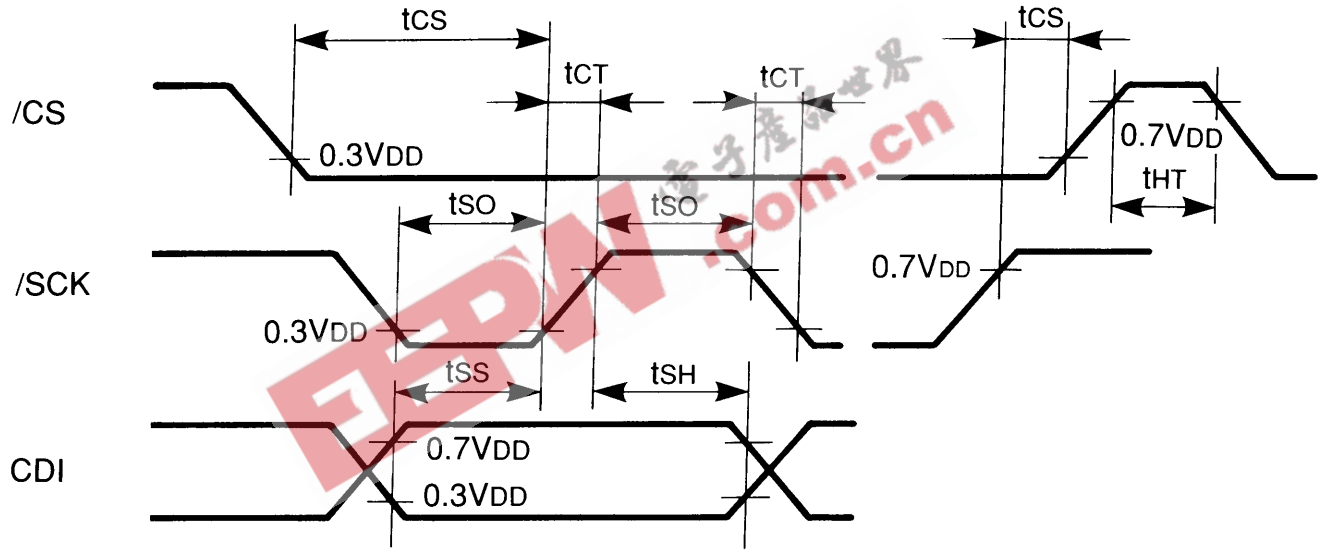
● Audio data input timing



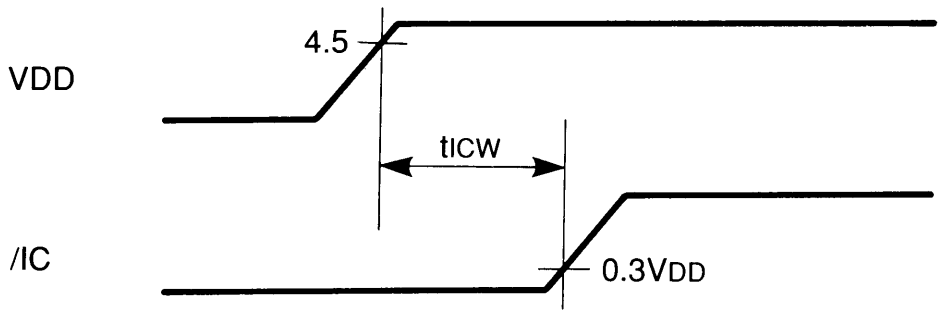
● Audio data output timing



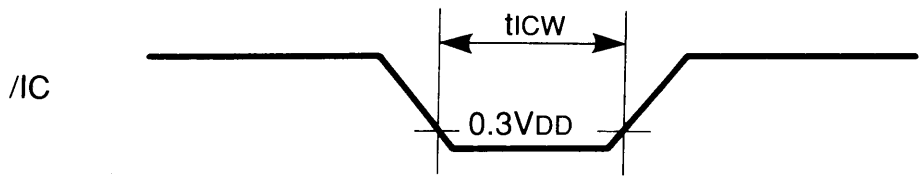
● Microprocessor interface timing



● Initial clear timing (At power on)

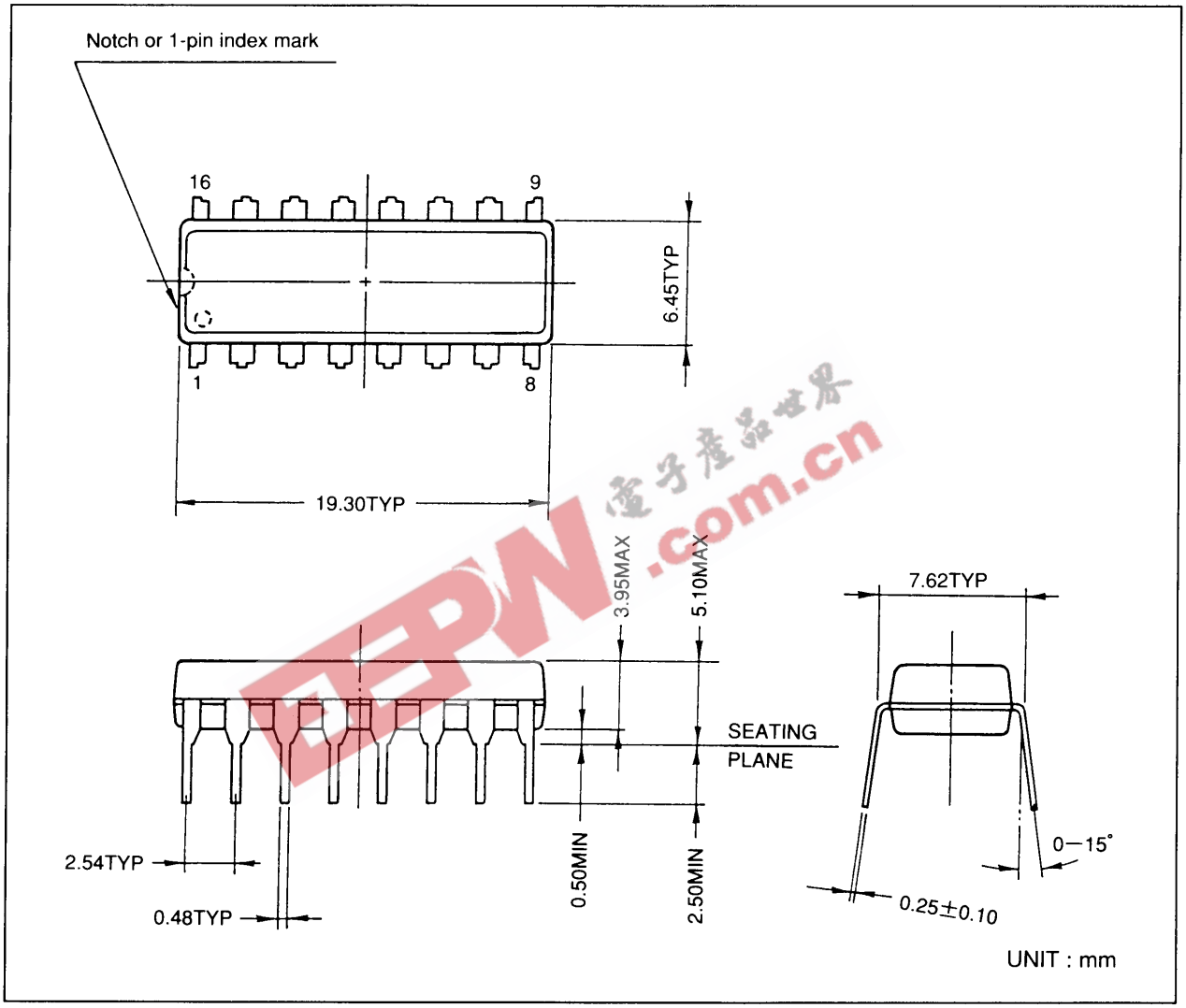


● Initial clear timing (normally)



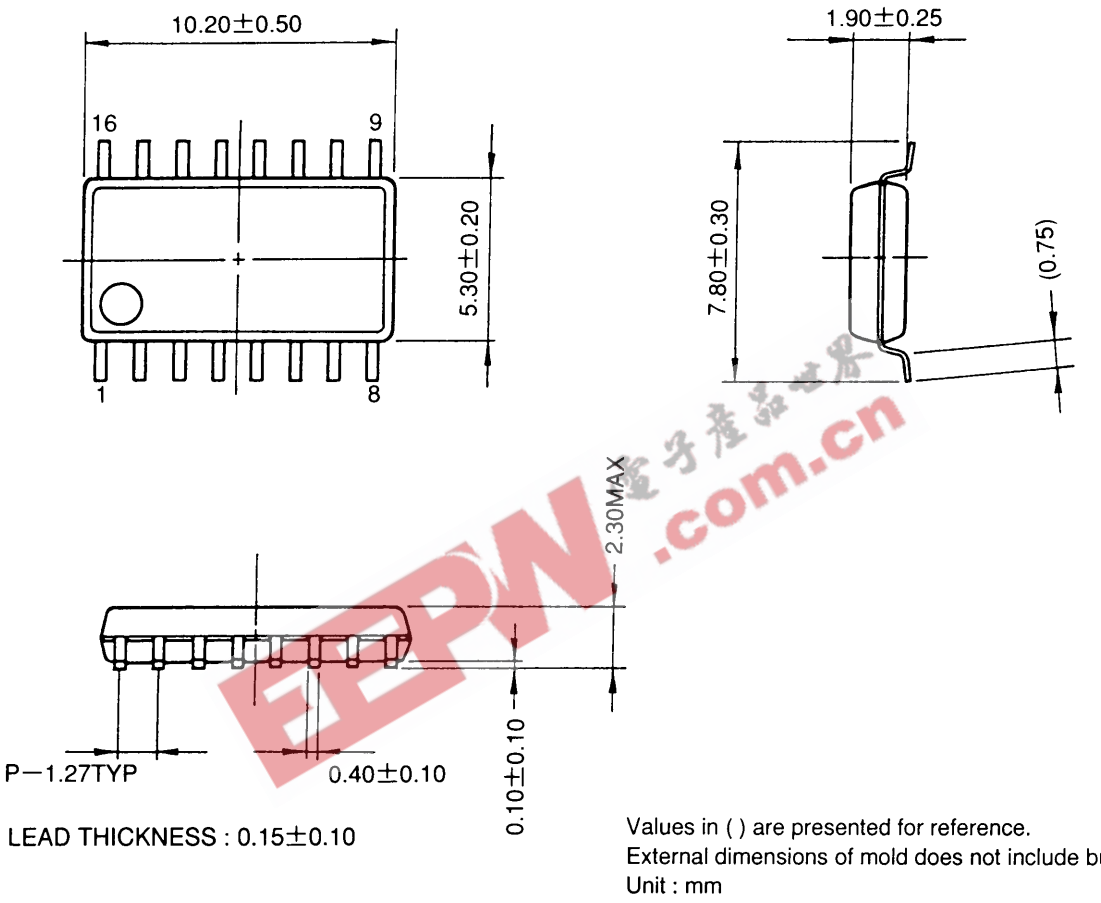
■EXTERNAL DIMENSIONS

●YSS 231-D



■EXTERNAL DIMENSIONS

●YSS 231-M

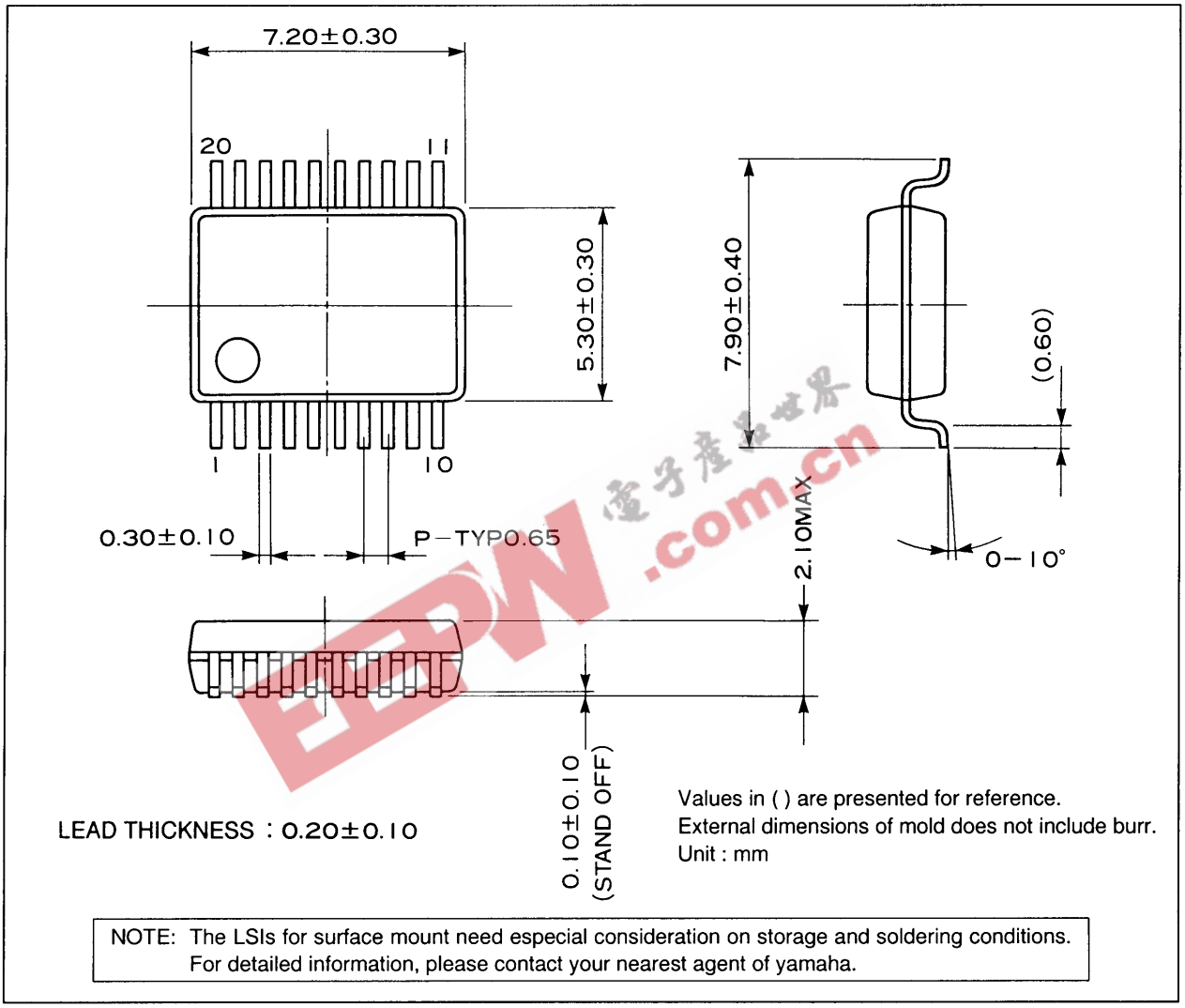


Values in ( ) are presented for reference.
External dimensions of mold does not include burr.
Unit : mm

NOTE: The LSIs for surface mount need especial consideration on storage and soldering conditions.
For detailed information, please contact your nearest agent of yamaha.

■EXTERNAL DIMENSIONS

●YSS 231-E



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