YAMAHA® LSI

YTD418

APPLICATION MANUAL

IDNPHS

User Network Interface for ISDN Basic Access

YAMAHA

YTD418 APPLICATION MANUAL
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Chapter 1

INTRODUCTION

1.1 General Description

The YTD418 is an analog driver/receiver-less version of the YM7405B with the ISDN Basic Rate user-network interface function (digital four-wire time-division full-duplex operation). Therefore it is suitable for connecting a DSU which has TTL level signaling interface.
In only one chip, the YTD418 supports Layer 1 (physical layer) control function described in ITU-T Recommendation I.430 and fully supports Layer 2 (LAP-D protocol) described in ITU-T Recommendations Q.920 and Q.921.
The YTD418 also includes the Layer 3 processor interface function in an 80-pin QFP package and has great advantage for mounting and functional designing of Base Station (BS) of the Personal Handy phone System (PHS) or other terminal equipment (TE) which has a built-in DSU.
With connecting an external driver/receiver, the YTD418 allows complete Layer 1 function described in ITU-T Recommendation I.430.

1.2 Features

1. Layer 1

   - Supports Layer 1 control function described in ITU-T Recommendation I.430 [1992 edition] and TTC Standard JT-I430 [1993 edition] (default)
     - TTL interface, 192 kbps transmission
     - Interface structure : 2B+D (B=64 kbps、D=16 kbps)
     - Frame assembling and disassembling function
     - Collision control (built-in random number (Ri) reset), priority control (built-in retransmission control), and state transition control
   - Supports ETSI ETS 300 012 [April 1992] operation mode (Refer to "YTD418 APPLICATION NOTE")
   - Leased line capability (JT-I430-a)
   - B channel I/O clock selection function
     - Internal clock mode

       Inputs/outputs the B channel data with a 64kHz internal clock
     - External clock mode

       Inputs/outputs the B channel data with a 128kHz to 2048kHz external clock

- B channel selection function
  - Internal clock mode
    Selects/switches B channel I/O pins
  - External clock mode (PCM Highway mode)
    Selects/switches B channel time slots
- Multiframing capability
  - Q channel access
  - S channel access
- Loop-back test function (for test and maintenance)
  - Three kinds of loop-back mode (Loop-back 1 to 3)
- INFO 1 transmission monitor pin
- SLEEP monitor pin
- I.430 transmission frame phase adjustment function

2. Layer 2

   - Compatible with ITU-T Recommendation Q.920 and Q.921 [1992 edition] and TTC Standard JT-Q920 and JT-Q921 [1993 edition] (default)
     - HDLC frame control (Flag control, FCS generation/checking, automatic zero insertion/deletion, abort pattern transmission/detection, etc.)
     - LAP-D status control (sequence control, flow control, SAPI control)
     - Built-in timer for time-out check.
   - Supports ETSI ETS 300 125 [September 1991] operation mode (Refer to "YTD418 APPLICATION NOTE")
   - Multi-link capability (circuit switching, packet switching)
   - Automatic assigned TEI/non-automatic assigned TEI (VC/PVC) capability
   - XID frame support

3. Layer 3 interface function

   - Connectable to 8-bit or 16-bit microprocessor (8086 family, Z80 family, 6800 family, 68000 family)
   - Data transfer method : DMA transfer
   - Primitive logical interface

4. Power-down mode (low-power operation)

5. CMOS technology with single +5 volt supply

6. 80-pin QFP

7. YM7405B software compatible

Note: For "YTD418 APPLICATION NOTE", please contact Yamaha.

Chapter 2

BLOCK DIAGRAM

2.1 User Network Interface Block Diagram

The YTD418 is the most suitable LSI for the PHS Base Station or TE which has a built-in DSU. Since the YTD418 contains all Layer 1, Layer 2 functions for the ISDN terminal equipments, they can be optimally configured by adding a small number of circuits including layer 3 control processor and analog driver/receiver if necessary.
The block diagram of the user network interface with the YTD418 is shown in Figure 2.1.

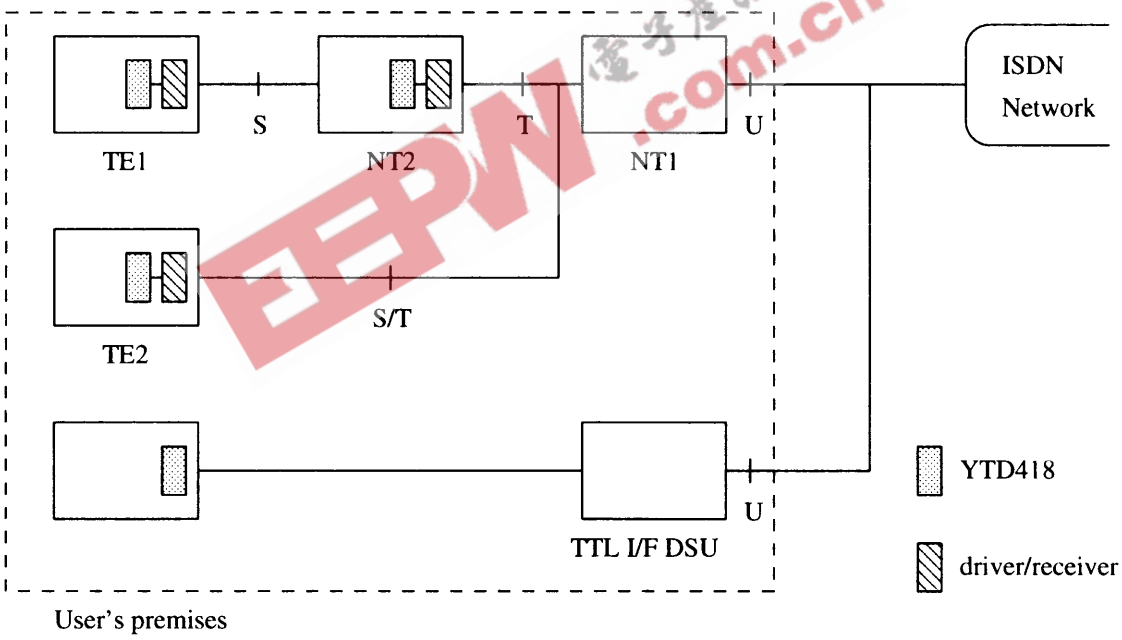


Figure 2.1: User-network interface block diagram

2.2 YTD418 Peripheral LSI Interface Block Diagram

The YTD418 peripheral LSI interface block diagram is shown in Figure 2.2.

2.3 YTD418 Internal Block Diagram

The YTD418 internal block diagram is shown in Figure 2.3. The function of each block is described in Chapter 4.

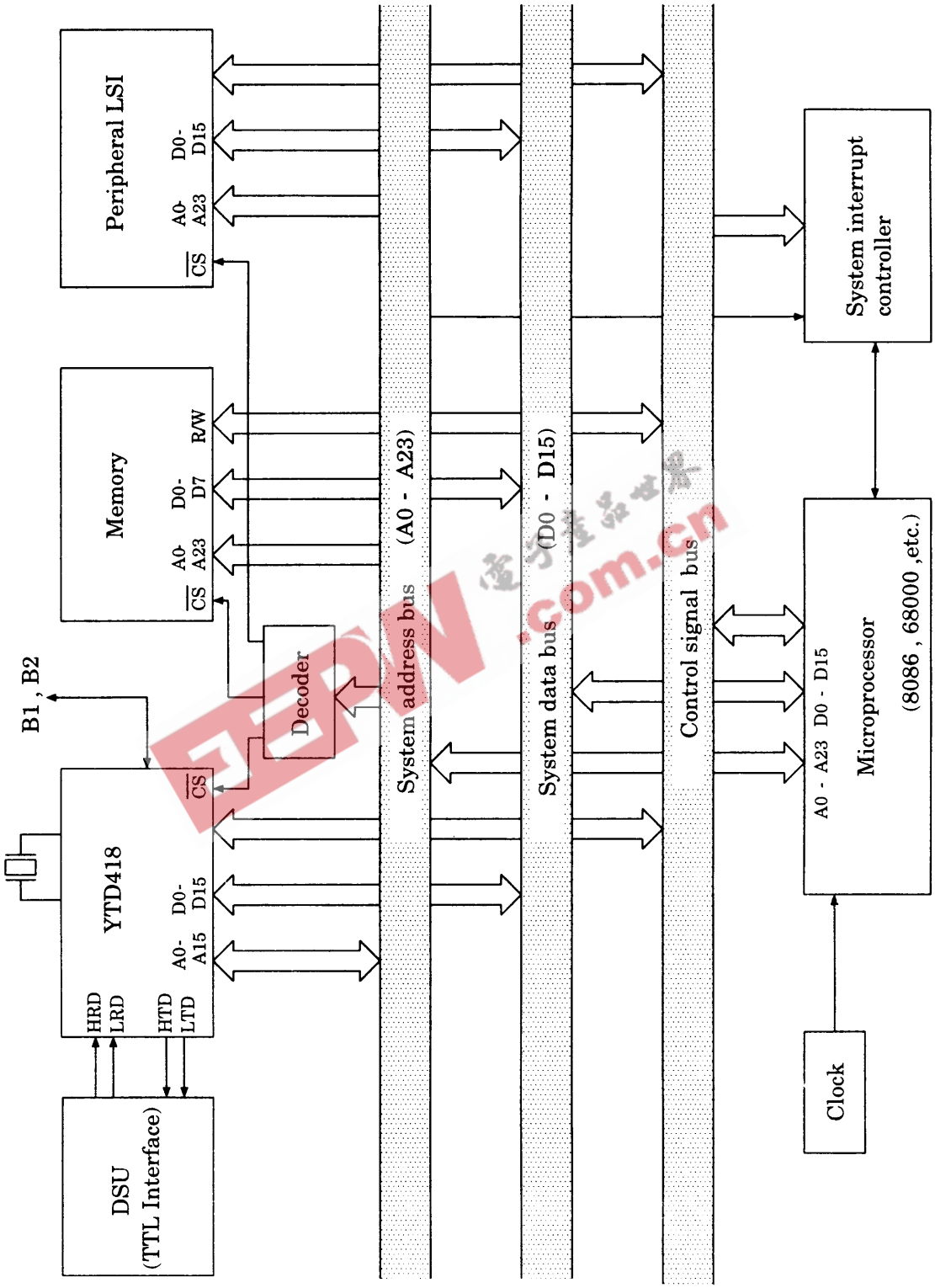


Figure 2.2: YTD418-peripheral LSI interface block diagram

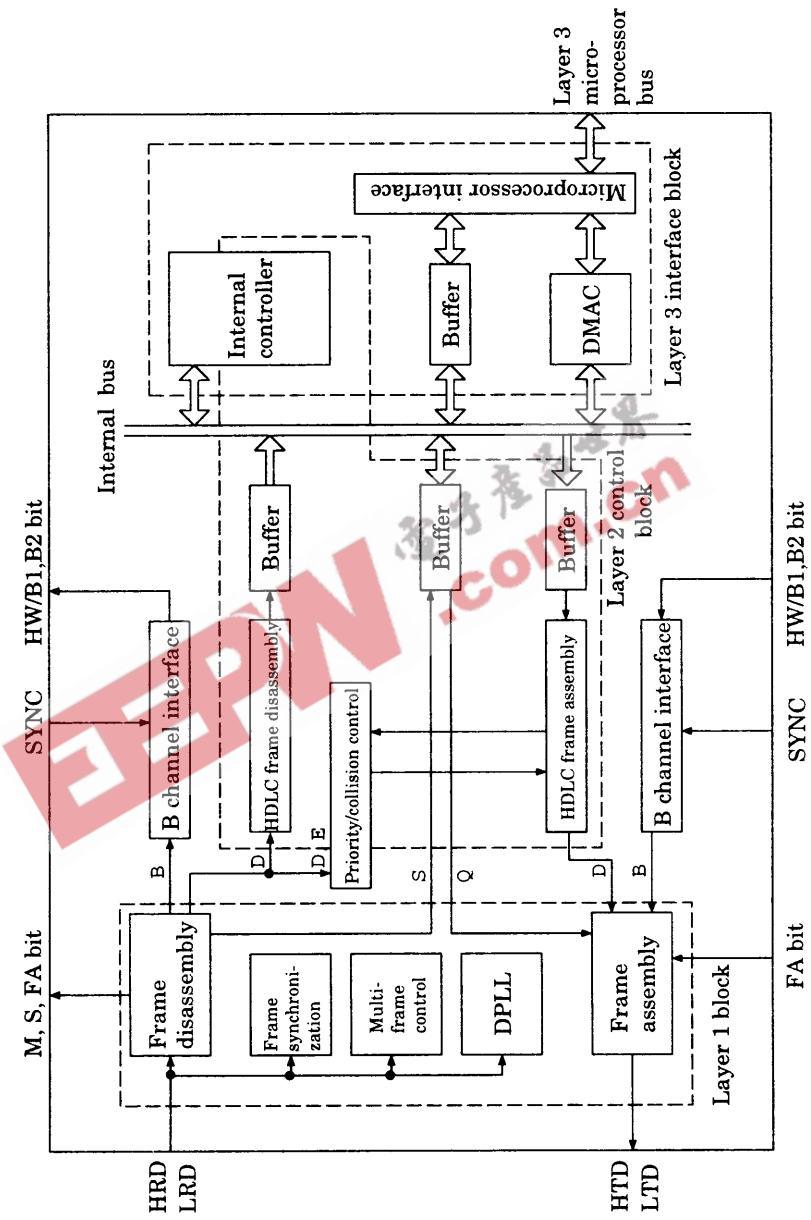


Figure 2.3: YTD418 internal block diagram

Chapter 3

PIN DESCRIPTIONS

3.1 Pin Assignments

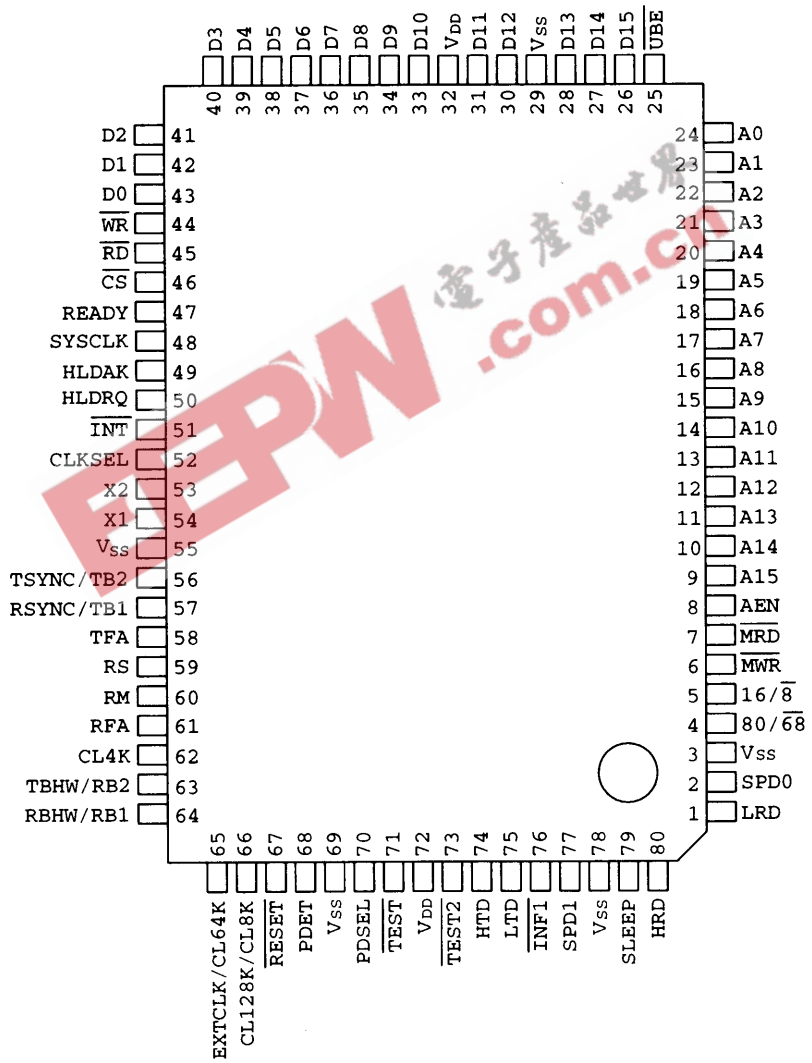


Figure 3.1: YTD418-F (80-pin QFP) pin assignment [Top View]

3.2 Pin Functions

3.2.1 Common Section

Pin No.	Pin Name	I/O	Function	Remarks
32,72	VDD	PWR	+5V power supply (±5%)	
3,29,55,69,78	VSS	GND	ground	
54	X1	IN	Connected to 12.288 MHz crystal oscillator. External clock can be input instead of crystal.	Refer to page 98
53	X2	OUT	Connected to 12.288 MHz crystal oscillator.	
67	$\overline{\text{RESET}}$	IN	System reset input (reset when LOW). Over 250 μs LOW input sets all internal registers, flags, counters, etc. to default value.	
71	$\overline{\text{TEST}}$	IN	Test mode input. Usually fixed at HIGH.	Pull-up resistor
73	$\overline{\text{TEST2}}$	IN	Test mode input. Usually fixed at HIGH.	
70	PDSEL	IN	Power supply detection mode selection.	
68	PDET	IN	Power supply detection from DSU.	Pull-down resistor
79	SLEEP	OUT	Sleep monitor. During the YTD418 is in the sleep state, this pin outputs HIGH.	

3.2.2 DSU Interface Section

Pin No.	Pin Name	I/O	Function	Remarks
80	HRD	IN	Receive Data (Positive) Input data from a TTL level interface DSU.	
1	LRD	IN	Receive Data (Negative) Input data from a TTL level interface DSU.	
74	HTD	OUT (O.D.)	Transmit Data (Positive) Output data to a TTL level interface DSU.	Open drain
75	HLD	OUT (O.D.)	Transmit Data (Negative) Output data to a TTL level interface DSU.	Open drain
76	$\overline{\text{INF1}}$	OUT (O.D.)	INFO 1 monitor During the YTD418 transmits INFO 1 signal, this pin outputs LOW.	Open drain
2	SPD0	IN	Transmission frame phase adjustment 0 This pin adjusts the HTD/LTD output timing with respect to the HRD/LRD input.	
77	SPD1	IN	Transmission frame phase adjustment 1 This pin adjusts the HTD/LTD output timing with respect to the HRD/LRD input.	

3.2.3 Layer 1 and 2 Control Section

Pin No.	Pin Name	I/O	Function	Remarks
52	CLKSEL	IN	Selects internal/external clock mode for B channel data transmit/receive. HIGH or open : Internal clock mode LOW : External clock mode	Pull-up resistor

[Internal clock mode] CLKSEL pin — "HIGH" or open.

Pin No.	Pin Name	I/O	Function	Remarks
† 64	RB1	OUT	Receive B channel data output pin Used in internal clock mode. Internal register REG1 selects the B channel to be connected. Data rate: 64 kbps	
† 63	RB2	OUT		
59	RS	OUT	S bit data output pin	
61	RFA	OUT	FA bit data output pin	
60	RM	OUT	M bit data output pin	
† 57	TB1	IN	Transmit B channel data input pin Used in internal clock mode. Internal register REG1 selects the B channel to be connected. Data rate: 64 kbps	Pull-up resistor
† 56	TB2	IN		
58	TFA	IN	FA bit data input pin Used only when TFA pin enabled mode (REG0, D4 = "1"). Connects to RFA pin when TFA pin enabled mode is selected and multiframing is not used. (See page 32)	Pull-up resistor
† 65	CL64K	OUT	Outputs 64 kHz clock synchronized with CL8K. Used to generate the bit timing of RB1, RB2, TB1 and TB2.	
† 66	CL8K	OUT	Outputs 8 kHz clock extracted from the receive data. Used to generate the first bit timing of RB1, RB2, TB1 and TB2.	
62	CL4K	OUT	Outputs the 4 kHz frame synchronization signal extracted from the receive data. Used for multiframing.	

† Changes as shown on next page in external clock mode (when "LOW" selected at CLKSEL pin).

[External clock mode] CLKSEL pin — "LOW"

Pin No.	Pin Name	I/O	Function	Remarks
64	RBHW	OUT (O.D.)	In the external mode, outputs the receive B channel data synchronized with EXTCLK.	Open drain
63	TBHW	IN	In the external mode, inputs the transmit B channel data synchronized with EXTCLK.	
59	RS	OUT	S bit data output pin	
61	RFA	OUT	FA bit data output pin	
60	RM	OUT	M bit data output pin	
57	RSYNC	IN	In the external clock mode, inputs the 8 kHz synchronization pulse for the receive B channel data.	Pull-up resistor
56	TSYNC	IN	In the external clock mode, inputs the 8 kHz synchronization pulse for the transmit B channel data.	Pull-up resistor
58	TFA	IN	FA bit data input pin Used only when TFA pin enabled mode (REG0, D4 = "1"). Connects to RFA pin when TFA pin enabled mode is selected and multiframing is not used. (See page 32)	Pull-up resistor
65	EXTCLK	IN	In the external clock mode, inputs the clock for B channel data transmit/receive. Operates at 128 kHz to 2048 kHz.	
66	CL128K	OUT	In the external clock mode, outputs the 128 kHz clock extracted from the receive data. Used to synchronize RSYNC, TSYNC and EXTCLK.	
62	CL4K	OUT	Outputs the 4 kHz frame synchronization signal extracted from the receive data. Used for multiframing.	

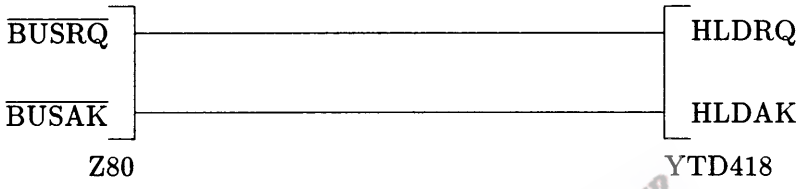
3.2.4 Layer 3 Interface Section

<table>
<tr><th>Pin No.</th><th>Pin Name</th><th>I/O</th><th>Function</th><th>Remarks</th></tr>
<tr><td>9-23</td><td>A15-A1</td><td>IN/OUT</td><td>During program I/O transfer with Layer 3 microprocessor, accept addresses for I/O register and primitive selection. In the DMA mode, these pins output the DMA addresses.</td><td></td></tr>
<tr><td>26-28
30,31
33-43</td><td>D15-D0</td><td>IN/OUT</td><td>8-bit bidirectional data bus (D0-D7) during program I/O transfer with Layer 3 microprocessor. In the DMA mode, these pins become 16-bit bidirectional data bus.</td><td>When using an 8-bit MPU, pins D8-D15 must be pulled high.</td></tr>
<tr><td>25</td><td>$\overline{\text{UBE}}$</td><td>IN/OUT</td><td>Becomes input at program I/O transfer with Layer 3 microprocessor. Only D0-D7 are valid data. In the DMA mode, the signal output from this pin depends on the value input at the 16/$\overline{8}$ pin.
• In the 8-bit data bus mode (16/$\overline{8}$= “L”), $\overline{\text{UBE}}$ always outputs A0.
• In the 16-bit data bus mode (16/$\overline{8}$= “H”), this pin indicates which pins (D0-D7 or D8-D15) contain valid data.
<table>
<tr><th>$\overline{\text{UBE}}$</th><th>A0</th><th>D0-D7</th><th>D8-D15</th></tr>
<tr><td>L</td><td>H</td><td></td><td>√</td></tr>
<tr><td>H</td><td>L</td><td>√</td><td></td></tr>
</table></td><td>When using an 8-bit MPU, this pin must be pulled high.</td></tr>
<tr><td>24</td><td>A0
($\overline{\text{LBE}}$)</td><td>IN/OUT</td><td>Indicates address A0 when the Layer 3 microprocessor I/O accesses to the YTD418 during program I/O transfer (input) with the Layer 3 microprocessor.
In the DMA mode (output), this pin indicates memory access address A0. See $\overline{\text{UBE}}$.</td><td></td></tr>
<tr><td>44</td><td>$\overline{\text{WR}}$</td><td>IN</td><td>Indicates that the Layer 3 microprocessor is in a write cycle. When a 6800/68000 is used, this pin connects to the R/$\overline{\text{W}}$ signal.</td><td></td></tr>
<tr><td>45</td><td>$\overline{\text{RD}}$</td><td>IN</td><td>Indicates that the Layer 3 microprocessor is in a read cycle. When a 68000 is used, this pin connects to the $\overline{\text{AS}}$ signal. When a 6800 is used, this pin connects to the $\overline{\text{E}}$ signal.</td><td></td></tr>
</table>

<table>
<tr><th>Pin No.</th><th>Pin Name</th><th>I/O</th><th>Function</th><th>Remarks</th></tr>
<tr><td>46</td><td>$\overline{CS}$</td><td>IN</td><td>This signal selects the YTD418 when the Layer 3 microprocessor sets the control information for I/O and DMA transfer.</td><td></td></tr>
<tr><td>47</td><td>READY</td><td>IN</td><td>This signal is used to widen the $\overline{MRD}$ and $\overline{MWR}$ signals output by the YTD418 during DMA transfer when the YTD418 is used with low-speed memory. While the READY signal is LOW, the $\overline{MRD}$ and $\overline{MWR}$ signals remain active low level.</td><td></td></tr>
<tr><td>51</td><td>$\overline{INT}$</td><td>OUT (O.D.)</td><td>Interrupt signal from the YTD418 to the Layer 3 microprocessor.</td><td>Open drain</td></tr>
<tr><td>6</td><td>$\overline{MWR}$</td><td>OUT</td><td>Indicates that the YTD418 is in a write cycle when data is transferred in the DMA mode. At program I/O transfer with the Layer 3 microprocessor, the output of this pin becomes high impedance.</td><td></td></tr>
<tr><td>7</td><td>$\overline{MRD}$</td><td>OUT</td><td>Indicates that the YTD418 is in a read cycle when data is transferred in the DMA mode. At program I/O transfer with the Layer 3 microprocessor, the output of this pin becomes high impedance.</td><td></td></tr>
<tr><td>8</td><td>AEN</td><td>OUT</td><td>When data is transferred in the DMA mode, this pin enables the address and outputs it to the system address bus. It is used to disable other system bus drivers.</td><td></td></tr>
<tr><td>49</td><td>HLDAK</td><td>IN</td><td>Inputs the response signal permitting DMA from the Layer 3 microprocessor.</td><td></td></tr>
<tr><td>50</td><td>HLDRQ</td><td>OUT</td><td>Outputs the signal requesting DMA to the Layer 3 microprocessor.</td><td></td></tr>
<tr><td>4</td><td>80/$\overline{68}$</td><td>IN</td><td rowspan="2">Sets the type of Layer 3 microprocessor.
<table><tr><th>80/$\overline{68}$</th><th>16/$\overline{8}$</th><th>MPU type</th></tr><tr><td>H</td><td>H</td><td>8086 family (default)</td></tr><tr><td>L</td><td>H</td><td>68000 family</td></tr><tr><td>H</td><td>L</td><td>Z80 family</td></tr><tr><td>L</td><td>L</td><td>6800 family</td></tr></table></td><td rowspan="2">Pull-up resistor</td></tr>
<tr><td>5</td><td>16/$\overline{8}$</td><td>IN</td></tr>
<tr><td>48</td><td>SYSCLK</td><td>IN</td><td>Inputs the Layer 3 microprocessor system clock. Operated by 2 to 10 MHz clock signal.</td><td>Pull-up resistor</td></tr>
</table>

Note With the YTD418, the Z80 is assumed to be the 80 series 8-bit microprocessor. Therefore, when an 80C188, μPD70208, or other 8086 family 8-bit microprocessor is used with the YTD418, use the YTD418 with inverters because their HLDRQ and HLDAK pins condition is the opposite of the negative logic of Z80. (See page 24.)

- Example of Z80 connection



- Example of 80C188 or μPD70208 connection

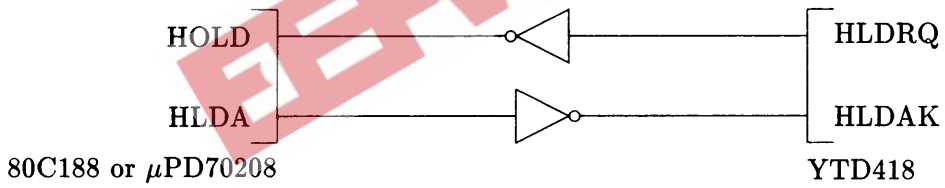


Figure 3.2: Example of the 80 series 8-bit microprocessor connection

Chapter 4

FUNCTIONS

4.1 Layer 1 Control Block

With external driver/receiver, the layer 1 control block allows the layer 1 function conforming to ITU-T Recommendation I.430.
Since the YTD418 inputs and outputs the TTL level signal instead of AMI signal, it can be directly connected to a DSU which has the TTL level signaling interface.
The YTD418 provides the I/O pins and I/O registers which will enable or disable the multiframing control circuits in the YTD418.
Three types of loopback functions are also provided for test and maintenance.

4.2 Priority/Collision Control Block

The priority/collision control block supports the ITU-T Recommendation I.430 priority mechanism and collision detection. The signaling information is given priority over other types of information (data) by selecting the high priority class. Furthermore, there are two priority within each priority class to give all competing TEs a fair access.
This block also monitors the E bit, and counts the number of consecutive binary "1". When the counter is equal to, or exceeds, the value set by priority control, it assumes that access is possible and starts the D channel information transmission.
While transmitting D channel information, it monitors the received E bit and compares it with the last transmitted D bit. If they do not match, this block stops transmission immediately and returns to the D channel monitoring state. Layer 2 and layer 3 do not need to set data again for retransmission.
For reliable check on multiple TEI assignment, a register to reset the random number generator used for the Reference number(Ri) of the TEI management procedure is also provided.

4.3 Layer 2 Control Block

The layer 2 control block implements all the layer 2 functions conforming to ITU-T Recommendation Q.920 and Q.921.
This block supports the HDLC frame formatting, the SAPI and TEI address control, the LAP-D sequence control and flow control, etc.
More specifically, when the YTD418 accepts the data link establishment request from the host processor (Layer 3) in order to initiate call or accept an incoming call, the YTD418 activates the layer 1, initiates the TEI assignment procedure (if necessary), and after that, establishes the data link and enters the multiple-frame-established state. After the call clearing, in accordance with the data link release request from the host processor, the YTD418 releases the data link and holds the assigned TEI value. The automatic assigned TEI value is removed on receipt of Identity remove message from the network, on occurrence of TEI identity verify procedure failure, etc.
Since both automatic and non-automatic TEI assignment are supported, VC (Virtual Call) / PVC (Permanent Virtual Call) can be implemented at packet switching.

4.4 Layer 3 Interface Block

The layer 3 interface block allows the microprocessor which implements the layer 3 functions described in ITU-T Recommendation Q.931 to access to the YTD418.
All control, status, data registers can be accessed directly by the microprocessor.
An 8086 or 68000 family 16-bit microprocessor, or Z80 or 6800 family 8-bit microprocessor, from 2MHz to 10MHz can be used with the YTD418. In any case, data is transferred in byte units.
There are two types of transfer methods, DMA transfer and program I/O transfer, as follows:

- The program I/O transfer is used to transmit or receive the primitives between layer 2 and layer 3 (i.e. between the YTD418 and the host processor). As a rule, the general syntax of each primitive is compatible with ITU-T Recommendation Q.921.
- The DMA transfer is used to transmit or receive the information (I) fields (layer 3 messages) and is controlled by the YTD418 internal DMA controller. Therefore, the host processor must specify the pointer and length of the layer 3 message data set in the external DMA buffer for the YTD418.

4.5 Power Down Function

To prevent extra power consumption while not in use, the YTD418 has a power down mode (low power consumption mode).

Chapter 7

ELECTRICAL CHARACTERISTICS

7.1 Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{DD}	−0.3	+7.0	V
Input Voltage	V_{IN}	−0.3	V_{DD}+0.3	V
Operating Temperature Range	T_{OP}	−20	+70	℃
Storage Temperature Range	T_{ST}	−50	+125	℃

(Based on V_{SS}=0.0V)

7.2 Recommended Operating Conditions

Supply Voltage	5V±5% (Based on V_{SS}=0.0V)
Operating Temperature Range	−20 – 70 ℃

7.3 DC Characteristics

(V_{DD}=5V±5%, T_{OP}=−20 - 70 ℃)

Parameter		Symbol	Min.	Typ.	Max.	Units
High-Level Input Voltage (CMOS)	**(Note 1)**	V_{IH}	$0.9V_{DD}$			V
Low-Level Input Voltage (CMOS)	**(Note 1)**	V_{IL}			$0.1V_{DD}$	V
High-Level Input Voltage (TTL)	**(Note 2)**	V_{IH}	2.2			V
Low-Level Input Voltage (TTL)	**(Note 2)**	V_{IL}			0.8	V
High-Level Output Voltage (CMOS)	**(Note 3)**	V_{OH}	$V_{DD}-0.4$			V
Low-Level Output Voltage (CMOS)	**(Note 4)**	V_{OL}			$V_{SS}+0.4$	V
High-Level Output Voltage (TTL)	**(Note 5)**	V_{OH}	2.7			V
Low-Level Output Voltage (TTL)	**(Note 5)**	V_{OL}			0.4	V
Low-Level Output Voltage (Open-D)	**(Note 6)**	V_{OL}			0.4	V
Leakage Current		I_L	−10		10	μA
Off-State Leakage Current	**(Note 7)**	I_{LZ}	−10		10	μA
Power Supply Current	**(Note 8)**	I_{DD}		15		mA

Note 1: With respect to X1 pin.

Note 2: With respect to other pins.

Note 3: Test Condition : $|I_{OH}| < 10\mu A$

Note 4: Test Condition : $|I_{OL}| < 10\mu A$

Note 5: $\overline{MWR}$, $\overline{MRD}$, A15–A0, $\overline{UBE}$, D15–D0 and HLDRQ pins.
Test Conditions : I_{OH} = −0.6mA, I_{OL}=1.2mA
RS, RM, RFA, RB1, RB2, CL64K, CL8K, CL4K, AEN and SLEEP pins
Test Conditions : I_{OH} = −0.2mA, I_{OL}=0.4mA

Note 6: $\overline{INT}$, HTD and LTD pins Test Conditions : I_{OL}=1.2mA
$\overline{INF1}$ pin Test Conditions : I_{OL}=3mA
RBHW pin Test Conditions : R_L=500Ω I_{OL}=0.8mA

Note 7: With respect to cases where D0–D15, A0–A15 and $\overline{UBE}$ pins are in the input state and where $\overline{MWR}$ and $\overline{MRD}$ pins are in Hi-Z state.

Note 8: Tested in active state.

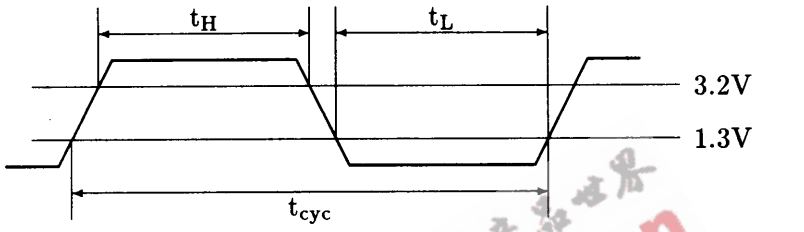
7.4 AC Characteristics

(V_{DD}=5V±5%、T_{OP}=−20 – 70 ℃)

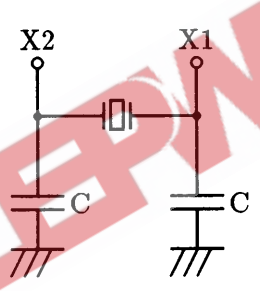
7.4.1 Clocks

1. Main Clock (External Input or Crystal Oscillation)

Parameter	Symbol	Min.	Typ.	Max.	Units
Main Clock Frequency	f_M		12.288		MHz
Clock Duty	t_{DUTY}	40	50	60	%



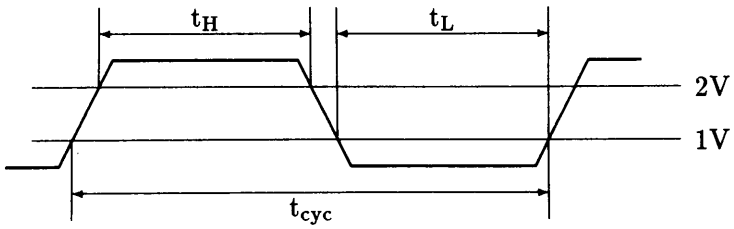
$t_{DUTY}=\frac{t_H}{t_{cyc}}$ or $\frac{t_L}{t_{cyc}}$



C=15–30pF

2. System Clock

Parameter	Symbol	Min.	Typ.	Max.	Units
System Clock Frequency	f_{sy}	2.0		10	MHz
Clock Duty	t_{DUTY}	33	50	61	%



$t_{DUTY}=\frac{t_H}{t_{cyc}}$ or $\frac{t_L}{t_{cyc}}$

7.4.2 Microprocessor Interface

1. In case of Bus Master (DMAC) (C_L=100pF)

Parameter	Symbol	Min.	Typ.	Max.	Units
HLDRQ Delay Time	t_{DHRQ}			100	ns
HLDAK Setup Time	t_{SHAK}	10			ns
HLDAK Hold Time	t_{HHAK}	0			ns
AEN HIGH Delay Time	t_{DANH}			100	ns
AEN LOW Delay Time	t_{DANL}			100	ns
Hi-Z to DRIVEN Time	t_{HZD}			70	ns
DRIVEN to Hi-Z Time	t_{DHZ}			100	ns
A15–A0, $\overline{UBE}$ Setup Time	t_{AS}		1		t_{sy}
A15–A0, $\overline{UBE}$ Hold Time	t_{AH}	$1t_{sy} - 50$			ns
$\overline{MWR}$, $\overline{MRD}$ Delay Time	t_{DM}			50	ns
$\overline{MWR}$, $\overline{MRD}$ Low Time	t_{ML}	$2t_{sy} - 30$			ns
READY Setup Time	t_{RS}	10			ns
READY Hold Time	t_{RH}	50			ns
Data Delay Time (WRITE)	t_{DDW}			80	ns
Data Hold Time (WRITE)	t_{DHW}		1		t_{sy}
Data Setup Time (READ)	t_{DSR}	40			ns
Data Hold Time (READ)	t_{DHR}	10			ns

Note: $t_{sy} = \frac{1}{f_{sy}}$ means the cycle of system clock.

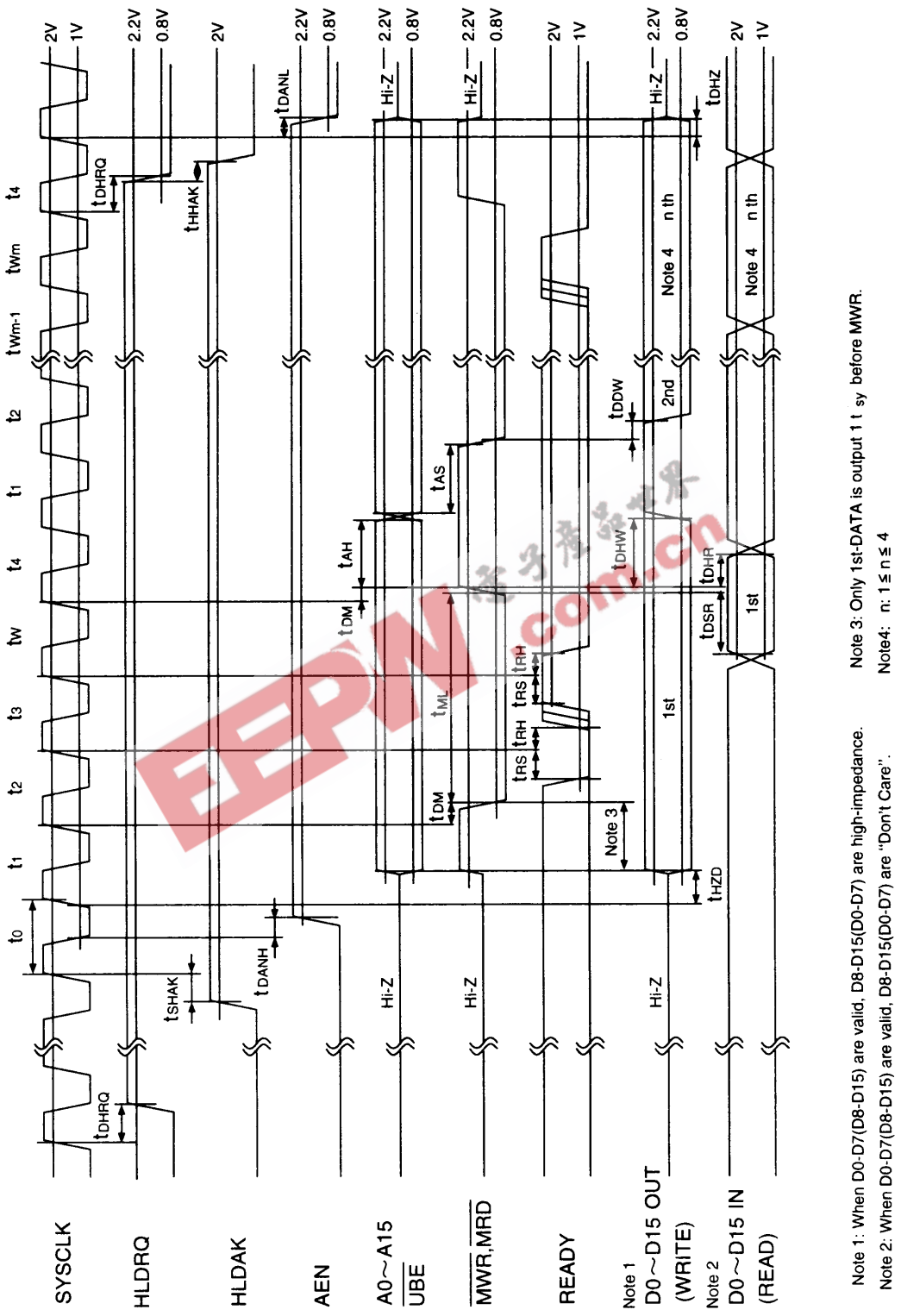


Figure 7.1: Microprocessor Interface in case of Bus Master

2. In case of Bus Slave (I/O Registers) (C_L=100pF)

⟨ **80 family microprocessor** ⟩

Parameter		Symbol	Min.	Max.	Units
Read/Write On Time	**(Note 1)**	t_{WL}	120		ns
Read/Write Off Time (1)		t_{WH1}	100		ns
Read/Write Off Time (2)	**(Note 2)**	t_{WH2}	3		t_{sy}
Read/Write Rise or Fall Time		t_r, t_f		30	ns
Address Setup Time		t_{AS}	15		ns
Address Hold Time		t_{AH}	10		ns
Data Setup Time		t_{DS}	40		ns
Data Hold Time		t_{DH}	10		ns
Data Delay Time		t_{DD}		60	ns

Note 1: Write On Time means the time at which both $\overline{WR}$ and $\overline{CS}$ are "L".
Read On Time means the time at which both $\overline{RD}$ and $\overline{CS}$ are "L".

Note 2: t_{sy} means the cycle of system clock.
t_{WH2} means a READ cycle of Status Data(REG 6) or a WRITE cycle of Command Data(REG 5) or a READ cycle of Send/Receive Status(REG 4) from Status Data or Command Data.

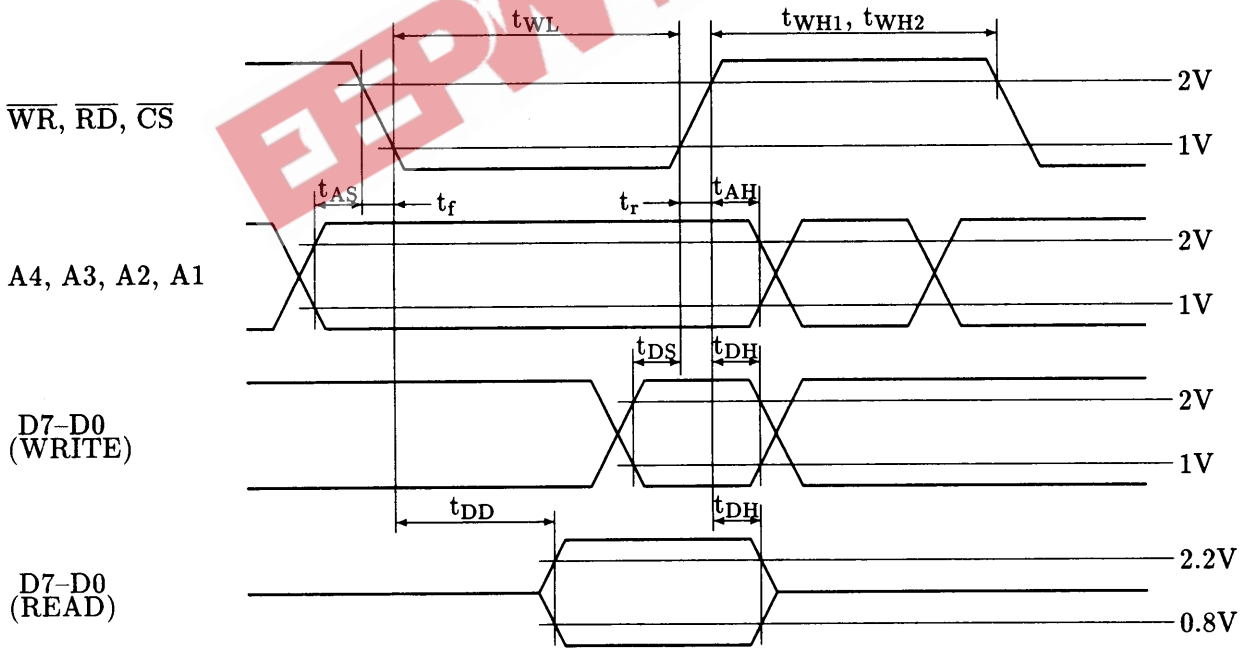


Figure 7.2: 80 family microprocessor

⟨ **68 family microprocessor** ⟩

Parameter		Symbol	Min.	Max.	Units
Read/Write On Time	**(Note 1)**	t_{WL}	120		ns
Read/Write Off Time (1)		t_{WH1}	100		ns
Read/Write Off Time (2)	**(Note 2)**	t_{WH2}	3		t_{sy}
Read/Write Rise or Fall Time		t_r, t_f		30	ns
Address Setup Time		t_{AS}	15		ns
Address Hold Time		t_{AH}	10		ns
Data Setup Time		t_{DS}	40		ns
Data Hold Time		t_{DH}	10		ns
Data Delay Time		t_{DD}		60	ns

Note 1: Write On Time means the time at which all of $\overline{AS}$ ($\overline{E}$), $\overline{CS}$ and R/$\overline{W}$ are "L".
Read On Time means the time at which both $\overline{AS}$ ($\overline{E}$) and $\overline{CS}$ are "L", and R/$\overline{W}$ is "H". (See Note 3 on next page)

Note 2: t_{sy} means the cycle of system clock.
t_{WH2} means a READ cycle of Status Data(REG 6) or a WRITE cycle of Command Data REG 5) or a READ cycle of Send/Receive Status(REG 4) from Status Data or Command Data.

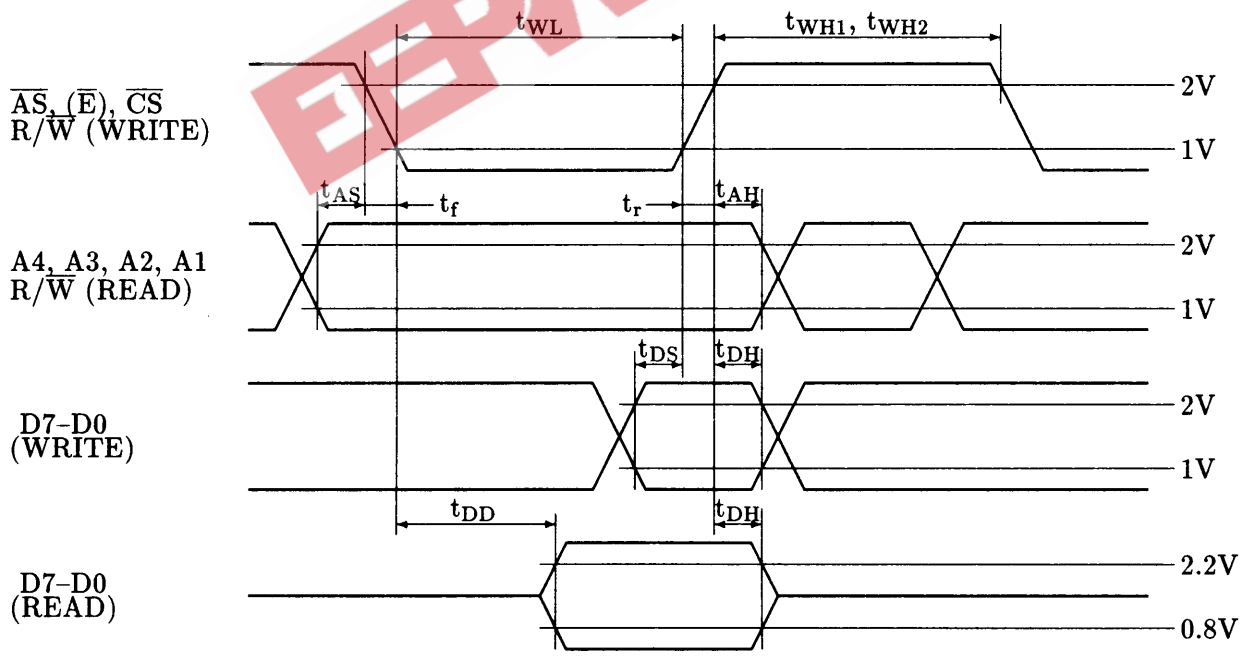
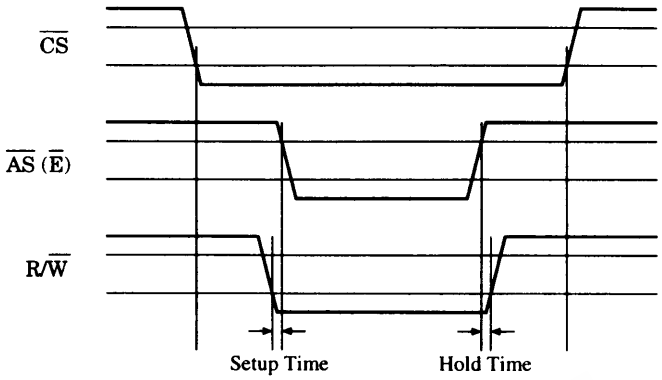


Figure 7.3: 68 family microprocessor

Note 3 Keep at least 10 ns R/$\overline{W}$ Setup Time and R/$\overline{W}$ Hold Time befor and after the time at which both $\overline{AS}$($\overline{E}$) and $\overline{CS}$ are "L", in order to avoid incorrect register reading.



7.4.3 DSU Interface

(C_L=100pF)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Receive Pulse High-Level Period	t_{HRW}		4.95	5.21	5.46	μs
F bit Transmission Delay Time	t_{RTD}	**Note 1**		10.41		μs
Transmit Pulse Hi-Z Period	t_{HTW}	**Note 2**	4.85	5.21	5.57	μs
Hi-Z to DRIVEN Time	t_{THZD}				50	ns
Transmit Pulse Phase Adjustment Time	t_{TPD}	SPD1= "H",SPD0= "H"		650		ns
		SPD1= "H",SPD0= "L"		325		ns
		SPD1= "L",SPD0= "H"		165		ns
		SPD1= "L",SPD0= "L"		0		ns
Timing Extract Jitter	j_{TT}		-7		+7	%

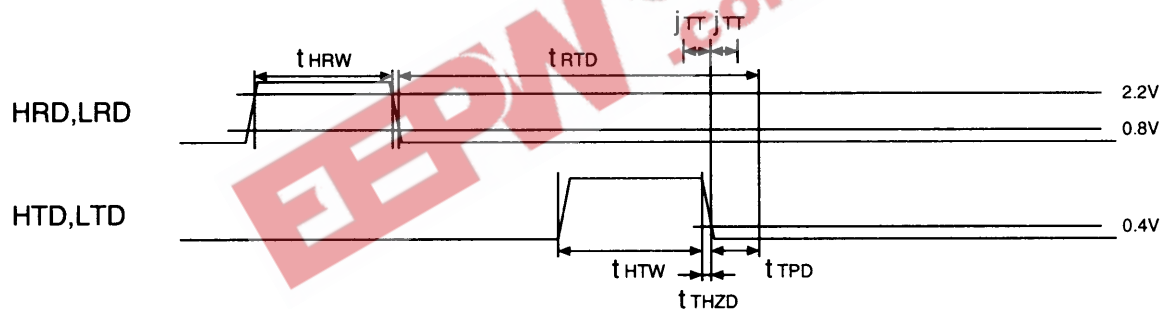


Figure 7.4: DSU Interface

Note 1 : The F bit position transmitted from a TE towards the NT shall be delayed, nominally, by two bit periods with respect to the F bit of the received frame.

Note 2 : Since the YTD418 leaves HTD and LTD pins open drain, it is prescribed by Hi-Z period.

7.4.4 B Channel Interface (Internal Clock Mode)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Units
CL64K Output Frequency	f_{CL64K}	f_X=12.288MHz		64		kHz
CL8K Synchronizing Frequency	f_{CL8K}	f_X=12.288MHz		8		kHz
Clock Phase Difference	t_{CD}	f_X=12.288MHz			6	ns
Receive Bch Data Output Delay Time	t_{BD}				200	ns
Send Bch Data Setup Time	t_{BS}		70			ns
Send Bch Data Hold Time	t_{BH}		10			ns

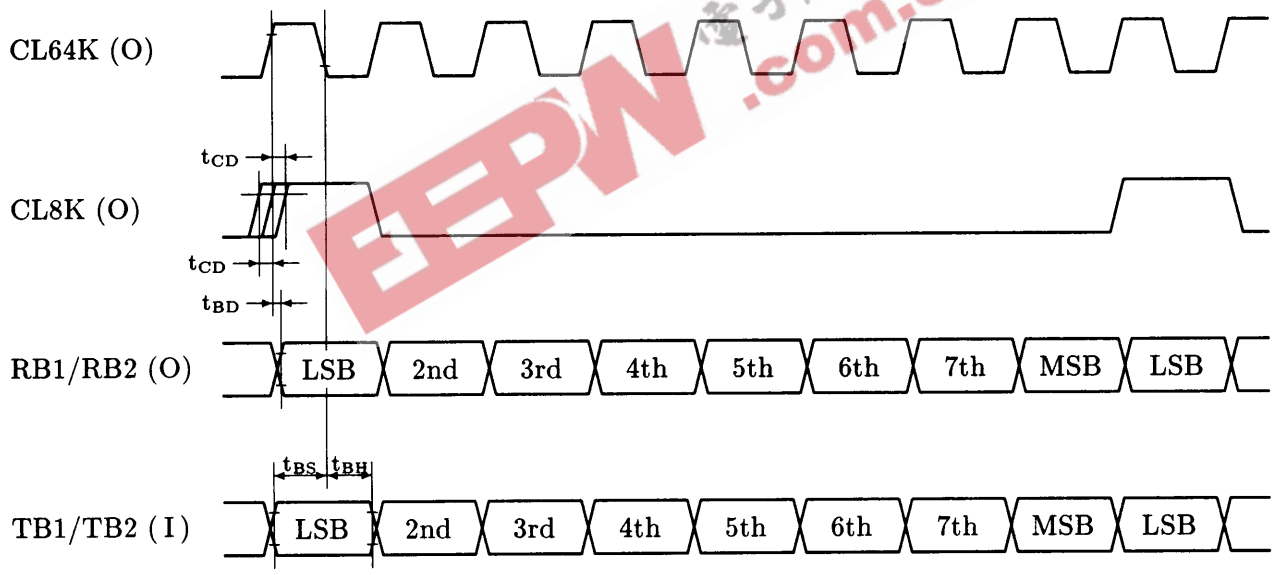


Figure 7.5: B Channel Input/Output Timing (Internal Clock Mode)

7.4.5 B Channel Interface (External Clock Mode)

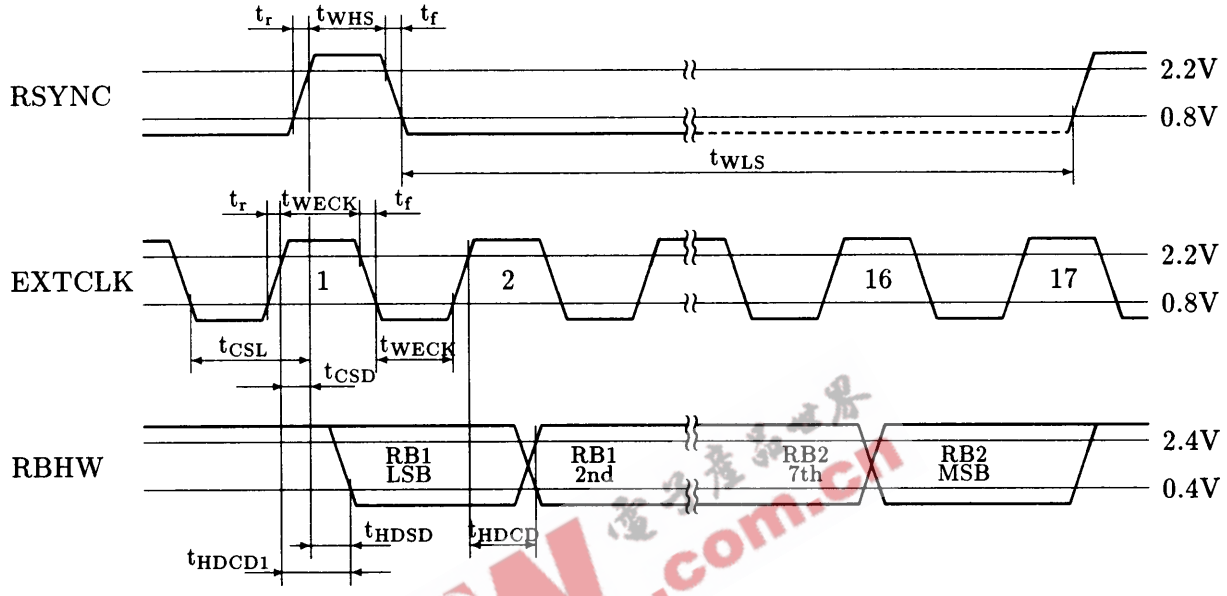
Test Condition: t_r , t_f = 5ns

Parameter	Symbol	Min.	typ.	Max.	Units
Clock Frequency	f_{ECK}	128		2048	kHz
Clock Cycle Period	t_{WECK}	200			ns
SYNC Frequency	f_{SYNC}		8		kHz
SYNC High-Level Period	t_{WHS}	200			ns
SYNC Low-Level Period	t_{WLS}	8			μs
Digital Input Rise Time	t_r			50	ns
Digital Input Fall Time	t_f			50	ns
SYNC Timing to Clock	t_{CSL}	40			ns
	t_{CSD}			100	ns
Data Output Delay Time to Clock **(Note 1, 2)**	t_{HDCD1}			170	ns
Data Output Delay Time To SYNC **(Note 1, 2)**	t_{HDSD}			170	ns
Data Output Delay Time **(Note 1)**	t_{HDCD}			180	ns
Data Input Setup Time	t_{HDS}	65			ns
Data Input Hold Time	t_{HDH}	120			ns

Note 1: Load Condition for Data Output Delay Time R_L = 500 Ω, C_L = 165pF, I_{OL} = 0.8mA, I_{OH} = −150μA

Note 2: Based on later point EXTCLK or SYNC.

[Receive Data Timing]



[Send Data Timing]

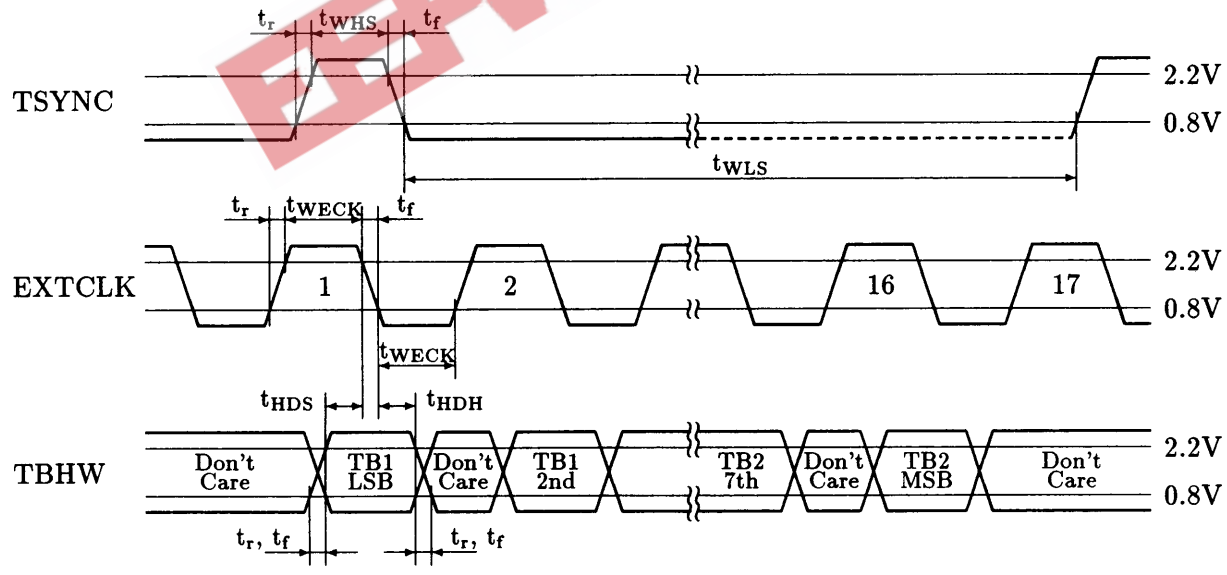


Figure 7.6: B Channel Input/Output Timing (External Clock Mode)

7.4.6 Bit Interface for Multiframing

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Units
CL4K Output Frequency	f_{CL4K}	f_X=12.288MHz		4		kHz
Received FA bit Output Delay Time	t_{FD}			66.6		μs
Received M bit Output Delay Time	t_{MD}			130.2		μs
Received S bit Output Delay Time	t_{SD}			187.5		μs
Send FA bit Hold Time	t_{FH}	to the CL4K Clock Rise point	67.7			μs

Note: Multiframing Bits are set to each bit timing of the frame structure at the S/T reference point.

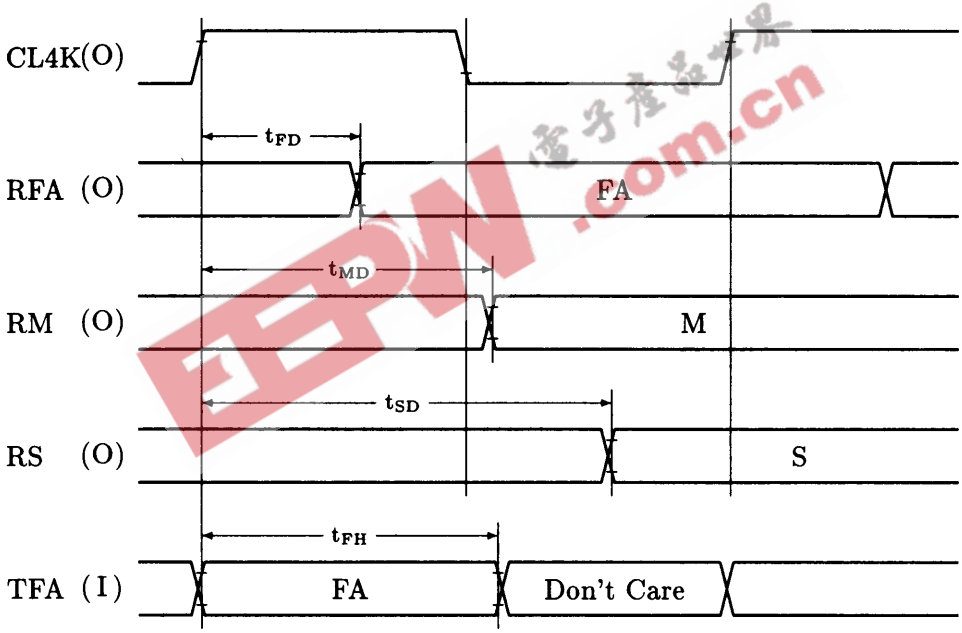
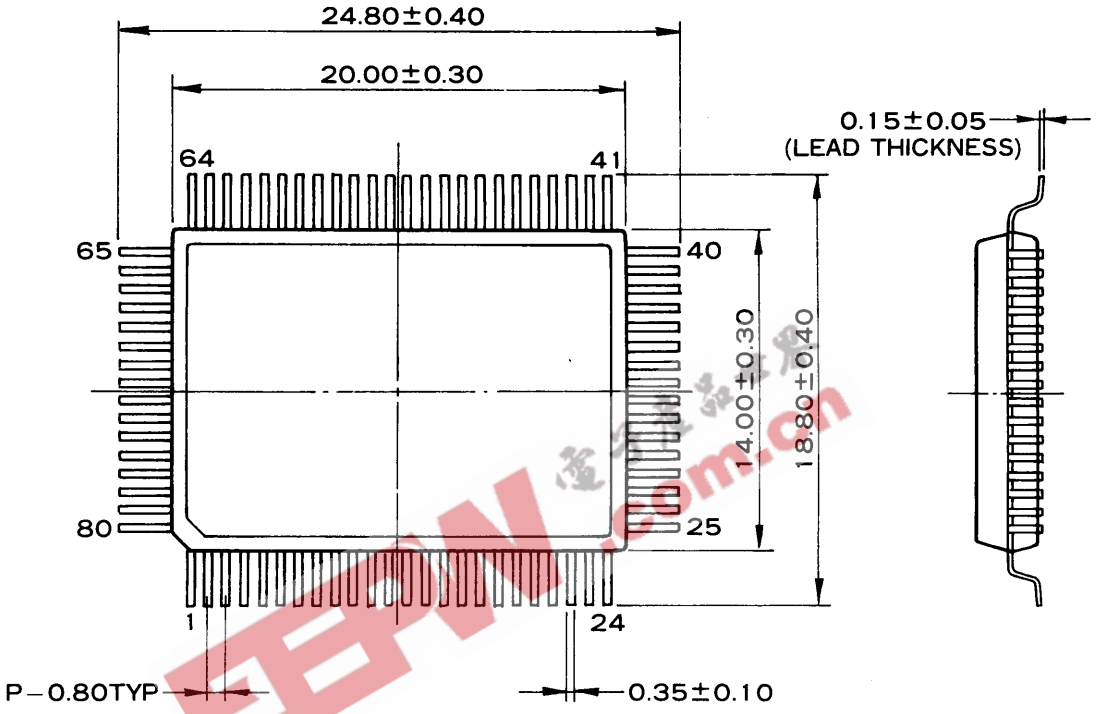


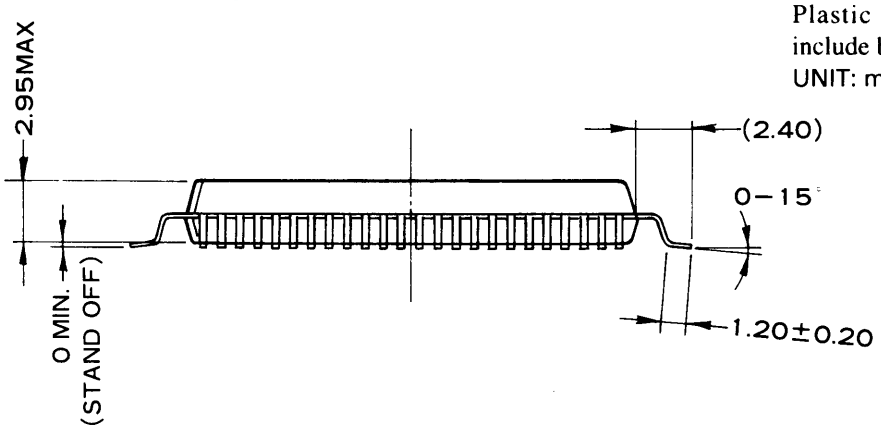
Figure 7.7: Input/Output Timing for Multiframing

Chapter 8

PACKAGE OUTLINE



The figure in the parenthesis ( ) should be used as a reference.
Plastic body dimensions do not include burr of resin.
UNIT: mm



Note : The LSIs for surface mount need especial consideration on storage and soldering conditions. For detailed information, please contact your nearest agent of Yamaha.

The specifications of this product are subject to improvement changes without prior notice.

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