# 2ilas

PRELIMINARY CUSTOMER PROCUREMENT SPECIFICATION

## **Z86E03/E06** CMOS Z8® OTP MICROCONTROLLERS

## FEATURES

Part	ROM (Kbytes)	RAM* (Kbytes)	SPI	Speed (MHz)	
Z86E03	512	61	No	8	
Z86E06	1	125	Yes	12	

\*General-Purpose

- 18-Pin DIP, WIN, and SOIC Packages
- 4.5- to 5.5-Volt Operating Range
- 0°C to +70°C Temperature Range

## **GENERAL DESCRIPTION**

The Z86E03/E06 are One-Time Programmable (OTP) members of the Z8<sup>®</sup> microcontroller family allowing easy software development, debug, and prototyping for small production runs that are not economically desirable with a masked ROM version.

Three address spaces, the Program Memory, Register File, and Expanded Register File (ERF), support a wide range of memory configurations. Through the ERF, the designer has access to four additional control registers that provide extra peripheral devices, I/O ports, register addresses, an SPI receive buffer and SPI compare register. Low-Power Consumption

- Expanded Register File (ERF)
- 14 Input/Output Lines
- Serial Peripheral Interface (SPI) (Z86E06 Only)
- Software Watch-Dog Timer (WDT)
- Power-On Reset (POR)

For applications demanding powerful I/O capabilities, the Z86E03/E06's dedicated input and output lines are grouped into two ports, and are configurable under software control to provide timing, status signals, or parallel I/O.

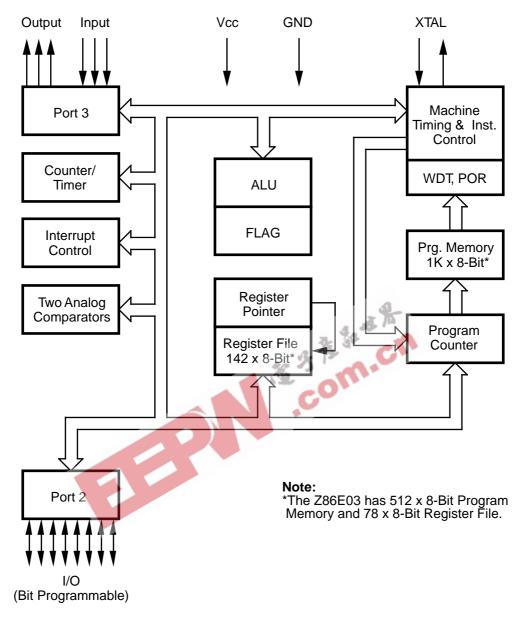
### Notes:

All Signals with a preceding front slash, "/", are active Low, e.g.: B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V <sub>cc</sub>	V <sub>DD</sub>
Ground	GND	V <sub>SS</sub>

## **GENERAL DESCRIPTION** (Continued)



**Functional Block Diagram** 

#### Z86E03/E06 2ilas PRELIMINARY CP95DZ81301 **GENERAL DESCRIPTION** (Continued) P24 P23 D4 D3 1 18 1 18 P25 2 17 P22 D5 2 17 D2 P26 3 P21 3 D6 D1 16 16 P27 D7 4 Z86E03/ 15 P20 4 15 D0 E06 Z86E03/E06 Vcc 5 5 GND Vcc GND 14 14 EPROM PDIP XTAL2 P36 N/C /PGM 6 13 6 13 XTAL1 /CE 7 P35 7 CLOCK 12 12 P31 P34 /OE CLEAR 8 11 8 11 P32 EPM 9 P33 9 10 10 VPP 18-Pin EPROM Mode Pin Configuration **18-Pin DIP/WIN Pin Configuration 18-Pin Identification Direction** Pin # Symbol Function 1-4 P24-P27 Port 2, Pins 4,5,6,7 Input/Output $V_{\underline{c}\underline{c}}$ 5 Power Supply Crystal Oscillator Clock Output XTAL2 6 Crystal Oscillator Clock Input 7 XTAL1 P31-P33 Port 3, Pins 1,2,3 8-10 **Fixed Input** P34-P36 Port 3, Pins 4,5,6 Fixed Output 11-13

Input/Output

14

15-18

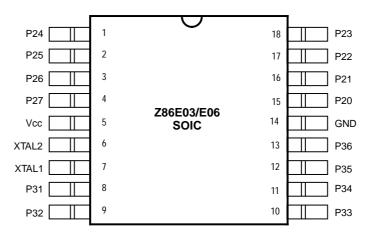
GND

P20-23

Ground

Port 2, Pins 0,1,2,3

## **GENERAL DESCRIPTION** (Continued)



18-Pin SOIC Pin Configuration

ABSOLUTE	MAXIMUM	RATINGS	

Symbol	Description	Min	Max	Units
V <sub>cc</sub>	Supply Voltage*	-0.3 -0.3	+7.0 V <sub>cc</sub> + 0.3	V
V <sub>IN</sub> T <sub>STG</sub>	Storage Temp	-65	+150	C
T <sub>A</sub>	Oper Ambient Temp	1		С

#### Notes:

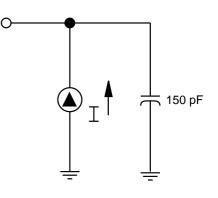
\* Voltage on Vcc with respect to Vss.

† See Ordering Information

\*\* Voltages on all pins with respect to Vss without current limitations.

## STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to ground. Positive current flows into the referenced pin (Test Load Configuration).



Stress greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended period

may affect device reliability.

**Test Load Configuration** 

## DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V <sub>cc</sub> Note [3]		to 70°C o 5.5V) Max	Typical @ 25°C	Units	Conditions	Notes
	Max Input Voltage	5.0V		12		V	I <sub>IN</sub> ≤ 250 µA	[8]
V <sub>CH</sub>	Clock Input High Voltage	5.0V	0.9 V <sub>cc</sub>	V <sub>CC</sub> +0.3	2.7	V	Driven by External Clock Generator	
V <sub>cl</sub>	Clock Input Low Voltage	5.0V	V <sub>ss</sub> -0.3	0.2 V <sub>cc</sub>	1.7	V	Driven by External Clock Generator	
V <sub>IH</sub>	Input High Voltage	5.0V	0.7 V <sub>cc</sub>	V <sub>cc</sub> +0.3	2.5	V		
V <sub>IL</sub>	Input Low Voltage	5.0V	V <sub>ss</sub> -0.3	0.2 V <sub>cc</sub>	1.6	V		
V <sub>OH</sub>	Output High Voltage (Low EMI Mode)	5.0V 5.0V	V <sub>cc</sub> -0.4 V <sub>cc</sub> -0.4		4.9 4.9	V V	I <sub>oH</sub> = -2.0 mA I <sub>OH</sub> = -0.5 mA	[10]
V <sub>OL1</sub>	Output Low Voltage (Low EMI Mode)	5.0V 5.0V		0.4 0.4	0.1 0.1	V V	I <sub>oL</sub> =+4.0 mA I <sub>oL</sub> =+1.0 mA	[10]
V <sub>OL2</sub>	Output Low Voltage	5.0V		1.0	0.3	V	$I_{0L} = +12 \text{ mA},$	[10]
V <sub>OFFSET</sub>	Comparator Input	5.0V		±10	±5	3 mV		
V <sub>ICR</sub>	Input Common Mode Voltage Range	5.0V	OV	V <sub>cc</sub> -1.5v		V S W		[7]
I	Input Leakage	5.0V	-1.0	1.0		μΑ	$V_{IN} = OV, V_{CC}$	
I <sub>ol</sub>	Output Leakage	5.0V	-1.0	1.0		μΑ	$V_{IN} = OV, V_{CC}$	
I <sub>cc</sub>	Supply Current	5.0V 5.0V		11.0 15	8.0 11	mA mA	@ 8 MHz @ 12 MHz	[4, 5, 12] [4, 5, 13]
I <sub>OB</sub>	Input Bias Current	5.0V		300		nA		[7]
I <sub>10</sub>	Input Offset Current	5.0V		±150		nA		[7]

## DC ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	V <sub>cc</sub> Note [3]		C to 70°C to 5.5V) Max	Typical @ 25°C	Units	Conditions	Notes
C1	Standby Current	5.0V		5	3.0	mA	HALT Mode V <sub>IN</sub> = OV, V <sub>CC</sub> @ 8 MHz	[4, 5, 12]
		5.0V		7.0	4.0	mA	HALT Mode $V_{IN} = OV$ , $V_{cc} @ 12 MHz$	[4, 5,13]
		5.0V		3.5	2.0	mA	Clock Divide by 16 @ 8 MHz	[4, 5,13]
		5.0V		4.5	2.5	mA	Clock Divide by 16 @ 12 MHz	[4, 5,13]
		5.0V		1.0		mA	HALT Mode@12 MHz	[4, 5,11,13]
C2	Standby Current	5.0V		10	1.6	μA	STOP Mode $V_{IN} = OV, V_{CC}$ WDT is not Running	[6, 9]
		5.0V			50	μA	STOP Mode $V_{IN} = OV, V_{CC}$ WDT is Running	[6, 9]
LL	Auto Latch Low Current	5.0V		30	19	μA	OV < V <sub>IN</sub> < V <sub>CC</sub>	
H	Auto Latch High Current	5.0V		-20	-11 ×	μΑ	$OV < V_{IN} < V_{CC}$	
POR	Power On Reset	5.0V	3	13	5 🕑	ms		
POR	$V_{\rm cc}$ Low Voltage		2.2	2.8	2.5	V		[3]
lotes: 1] I <sub>cc1</sub> Clock I	Driven	Тур 3.0			<b>req</b> MHz			
Crystal 2] $V_{ss} = 0V$ 3] The $V_{POI}$ 4] All outpon 5] $C_{L1} = C_{L}$ 6] Same as	or Ceramic Resonato V = GND a increases as the ten uts unloaded, I/O pins $_2 = 100 \text{ pF}$ s note [4] except inputs log comparator inputs	or 0.3 nperature decrea floating, inputs ts at V <sub>cc</sub> .	5.0 ases. at rail.	mA 8	MHz			

[8] Excludes clock pins and Port 3 inputs.

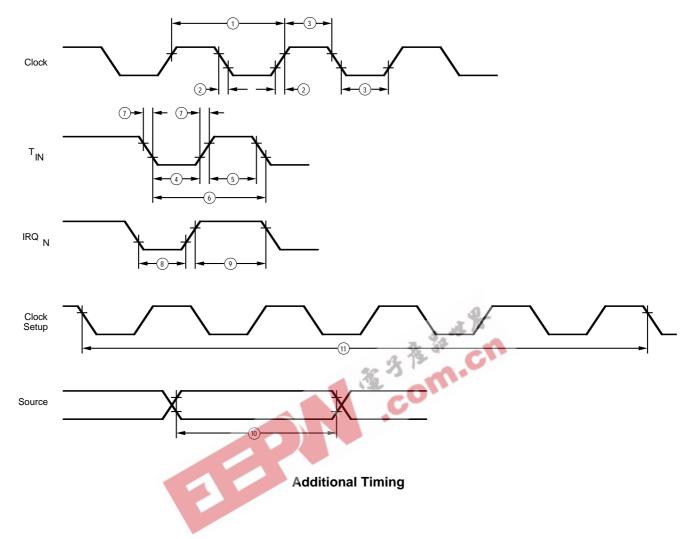
[9] Clock must be forced low when XTAL1 is clock driven and XTAL2 is floating.

[10] Standard mode (not low EMI mode).[11] Low EMI oscillator enabled.

[12] Z86E03.

[13] Z86E06.

## AC ELECTRICAL CHARACTERISTICS



## AC ELECTRICAL CHARACTERISTICS

			V <sub>cc</sub>	T <sub>A</sub> = 8 MI (E03			ИНz			
No	Symbol	Parameter	Note[3]	Min	Max	Min	Max	Units	Notes	
1	ТрС	Input Clock Period	5.0V	125	DC	83	DC	ns	[1,7,8]	
2	TrC,TfC	Clock Input Rise	5.0V		25		15	ns	[1,7,8]	
3 4	TwC TwTinL	Input Clock Width Timer Input Low Width	5.0V 5.0V	62 70		41 70		ns ns	[1,7,8] [1,7,8]	
5	TwTinH	Timer Input High Width	5.0V	5TpC		5TpC			[1,7,8]	

## AC ELECTRICAL CHARACTERISTICS (Continued)

					C To +70°C		
No	Symbol	Parameter	V <sub>cc</sub> Note[3]	8 MHz (E03) Min Max	12 MHz (E06) c Min Max	Units	Notes
6	TpTin	Timer Input Period	5.0V	8TpC	8ТрС		[1,7,8]
7	TrTin, TtTin	Timer Input Rise and Fall Timer	5.0V	100	100	ns	[1,7]
8	TwIL	Int. Request Input Low Time	5.0V	70	70	ns	[1,2,7]
9	TwiH	Int. Request Input High Time	5.0V	5TpC	5TpC		[1,8,10]
10	Twsm	STOP Mode Recovery Width Spec	5.0V	20	20	ns	[1]
11	Tost	Oscillator Startup Time	5.0V	5TpC	5TpC	ms	[1,4,9]
12	Twdt	Watch-Dog Timer Refresh Time	5.0V 5.0V 5.0V 5.0V	6 12 25 100	6 12 25 100	ms ms ms ms	D1 = 0 [5,6] D1 = 0 [5,6] D1 = 1 [5,6] D1 = 1 [5,6]
Note	s.						

#### Notes:

[1] Timing Reference uses 0.7  $\rm V_{cc}$  for a logic 1 and 0.2  $\rm V_{cc}$  for a logic 0.

[2] Interrupt request through Port 3 (P33-P31).

[3] V<sub>cc</sub> = 4.5V to 5.5V.
[4] SMR-D5 = 0, POR delay is off.

[4] SWR-D5 = 0, POR [5] Reg. WDTMR.

[6] Internal RC oscillator only.

[7] SMR D1 = 0.

 [8] Maximum frequency for internal system clock is 4 MHz when using SCLK = external clock.

[9] For RC and LC oscillator and for clock driven oscillator.

[10] SMR-D5 = 1, STOP mode recovery delay is on.



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