Z89300/01
DIGITAL TELEVISION CONTROLLER

GENERAL DESCRIPTION

The Z89300/01 Digital Television Controller is an application- specific controller designed to provide complete audio and video control of television receivers, video recorders, and advanced on-screen display facilities. The Z89301 is the one-time-programmable (OTP) version of the Z89300.The powerful 12 MHz Z89C00 RISC processor core allows the user to control the on-board peripheral functions and registers using the standard processor instruction set.

The extensive character attributes can be controlled in two modes: by the on-screen display controller character control mode for maximum display control flexibility, and closed caption mode for optimum display of closed caption text.

Closed caption text can be decoded directly from the composite video signal with the assistance of the processor's digital signal processing capabilities and displayed on the screen. The character representation in this mode allows for a simple attribute control through the insertion of control characters, and each word of RAM specifies two displayed characters.

The character control mode provides access to the full set of attribute controls. Each word of RAM specifies a single displayed character and basic character attributes, allowing the modification of attributes on a character-by-character basis. The insertion of control characters permits direction of other character attributes.

The fully customized 512 character set, formatted in two 256 character banks, can be displayed with a host of display attributes that incude underlining, italics, blinking, eight foreground/background colors, character position offset delay, and background transparency. The 16-bit display character representation allows the modification of some key attributes on a character-by-character basis. A character's pixel array is stored as a 16- or 18-word representation in Character Graphics ROM (CGROM). The ROM contents are referenced by a 16-bit word stored in video RAM (VRAM) defining the character type and its key attributes.

Serial interfacing with the television tuner is provided through the tuner serial port. Other serial devices, such as digital channel tunning adjustments, may be accessed through the industry standard I^2C port.

Additional hardware provides the capability to display two to three times normal size characters. The smoothing logic contained in the on-screen display circuit improves the appearance of larger fonts. Fringing circuitry can be activated to improve the visibiity of text by surrounding the character lines with a one-pixel border.

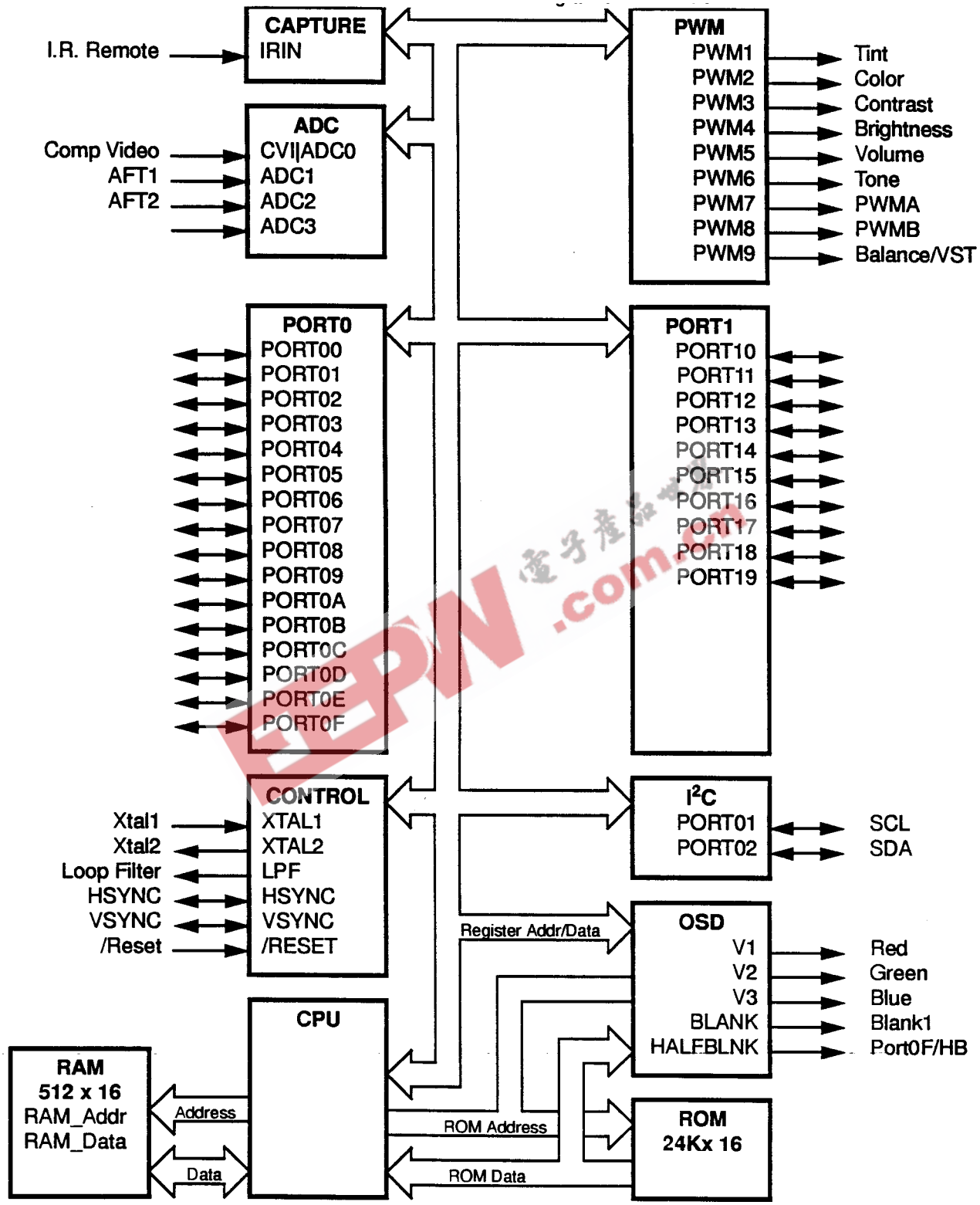
RGB outputs provide the direct video signals, and a blanking output is provided to control the video multiplexor. Dot clock and verticle line synchronization are normally obtained from H_FLYBACK and V_FLYBACK, but can be generated by the Z89300/01 and driven to the external deflection unit through the bidirectional SYNC ports when external video synchronization signals are not present.

User control can be monitored through the keypad scanning port, or the 16-bit remote control capture register. Receiver functions such as color and volume can be directly controlled by eight 8-bit pulse width modulated ports.

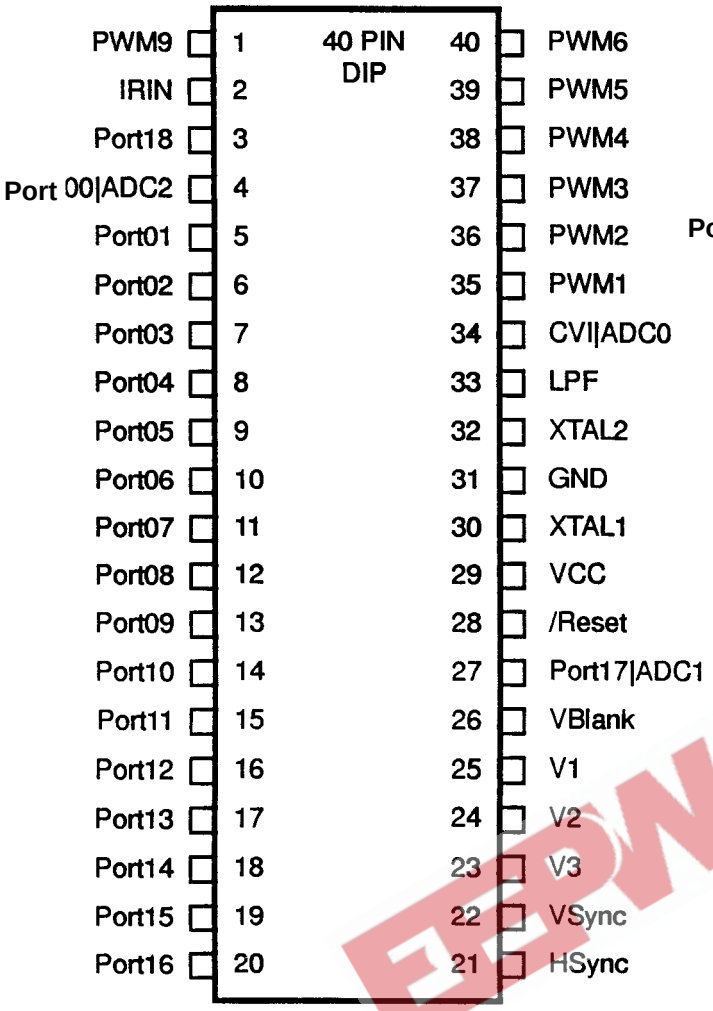
All nine PWM ports are only available in the 52-pin package. Only six 8-bit and one 14-bit PWM output pins are available in the 40-pin package.

The Z89300/01 has two internal 12 MHz VCOs that are referenced to a 32 KHz internal oscillator to provide the system clock. In Sleep mode, the controller uses the 32 KHz clock for the system clock to reduce power consumption. The processor can be suspended by placing it into STOP mode when main power is not available for minimal power consumption.

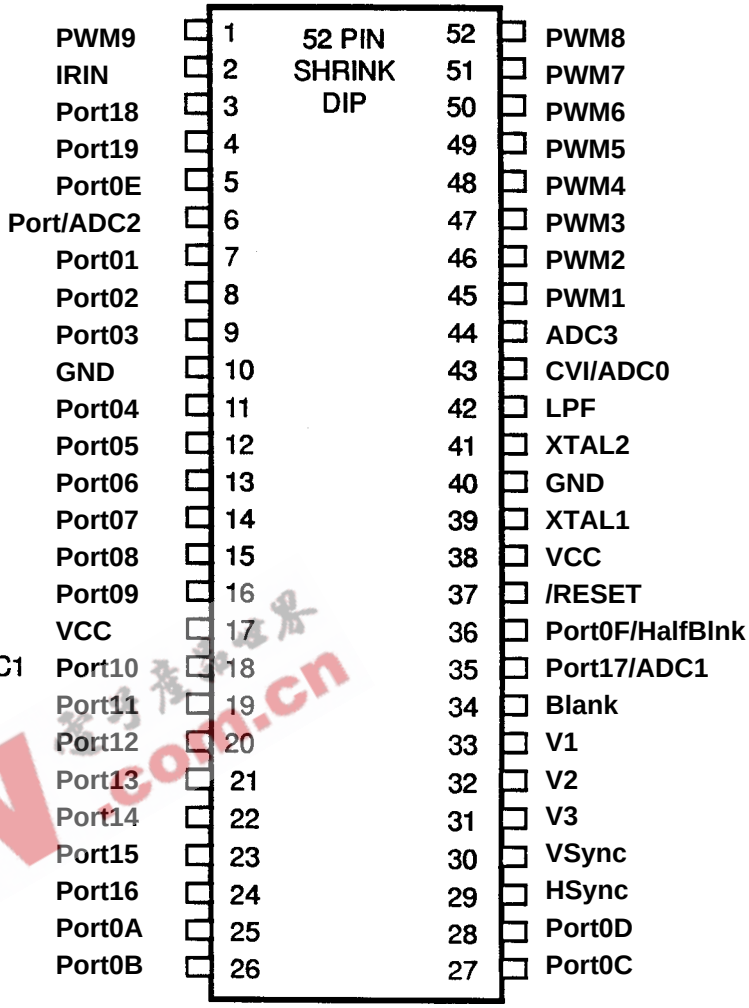
GENERAL DESCRIPTION (Continued)



Functional Block Diagram



40-Pin DIP Configuration



52-Pin Shrink DIP Configuration

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PIN DESCRIPTIONS
Z89300

Pin Name	Standard Application	52-Pin	40-Pin	I/O/B/ PWR	Reset Condition	Pad Type	Description
CVI/ADC0	COMP_VID	43	34	I		1	Analog Input
/RESET	RESET	37	28	I		8	Reset Signal
ADC3	A/D	44	-	I		1	Analog Input to A/D
Port1 [7] /ADC1		35	27	B/I		4/1	
PWM9	BALANCE/ VST	1	1	O		7	14-Bit PWM
PWM8	PWMB	52	-	O		7	General-Purpose PWM B
PWM7	PWMA	51	-	O		7	General-Purpose PWM A
PWM6	TONE	50	40	O		7	Tone Control
PWM5	VOLUME	49	39	O		7	Volume Control
PWM4	BRIGHT	48	38	O		7	Brightness Control
PWM3	CONTRAST	47	37	O		7	Contrast Control
PWM2	COLOR	46	36	O		7	Color Control
PWM1	TINT	45	35	O		7	Tint Control
							Data I/O
PORT0 [8]	SER_DATA	15	12	B	O	4	Serial Data
PORT0 [9]	SER_CLK	16	13	B	O	4	Serial Clock
PORT0 [3]	SER_EN	9	7	B	O	4	Serial Enable
PORT0 [2]	IIC_DATA	8	6	B		4	I^2C Data
PORT0 [1]	IIC_CLK	7	5	B		4	I^2C Clock
							Keyscanning Ports
PORT0 [4]	SCAN_IN0	11	8	B	I	4	Key Scan Input 0
PORT0 [5]	SCAN_IN1	12	9	B	I	4	Key Scan Input 1
PORT0 [6]	SCAN_IN2	13	10	B	I	4	Key Scan Input 2
PORT0 [7]	SCAN_IN3	14	11	B	I	4	Key Scan Input 3
PORT1 [6]	SCAN_OUT0	24	20	B	O	4	Key Scan Output 0
PORT1 [7]	SCAN_OUT1	35	27	B	O	4	Key Scan Output 1
PORT1 [8]	SCAN_OUT2	3	3	B	O	4	Key Scan Output 2
PORT1 [9]	SCAN_OUT3	4	-	B	O	4	Key Scan Output 3
						4	General-Purpose Control
PORT0 [0] /ADC2		6	4	B/I	O	4	
PORT0 [A]		25	-	B	O	4	
PORT0 [B]		26	-	B	O	4	
PORT0 [C]		27	-	B	O	4	

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PIN DESCRIPTIONS
Z89300 (continued)

Pin Name	Standard Application	52-Pin	40-Pin	I/O/B/ PWR	Reset Condition	Pad Type	Description
PORT0 [D]		28	-	B	O	4	
PORT0 [E]		5	-	B	O	4	
PORT0 [F] /HalfBlnk		36	-	B	O	4	
PORT1 [0]	LED1_PWR	18	14	B	O	4	Power LED Control
PORT1 [1]	LED2_AUD	19	15	B	O	4	Mono/Stereo LED Control
PORT1 [2]	LED3_TMR	20	16	B	O	4	Timer On/OFF LED Control
PORT1 [3]	TV_VCR	21	17	B	O	4	TV/Video Switch Control
							Power & Power Mgmt
PORT1 [4]	PWR_CTL	22	18	B	O	4	Power On/Off Control
PORT1 [5]	PWR_DET	23	19	B		4	Low Power Detect Input
VCC	+ 5 Volts	17 38	29	PWR			Supply Power
GND	0 Volts	10 40	31	PWR			Digital/Analog Ground
XTAL2		41	32	Analog		3	Oscillator Oscillator Crystal Terminal 2
XTAL1		39	30	Analog		1	Oscillator Crystal Terminal 1
LPF	LOOP FILTER	42	33	I			PLL Loop Filter
V1	RED	33	25	O		6+Analog	RGB Display Red Display Signal
V2	GREEN	32	24	O		6+Analog	Green Dislay Signal
V3	BLUE	31	23	O		6+Analog	Blue Display Signal
BLANK	BLANK	34	26	O		3	RGB Video Multipleor Control Signal
							Display Synchronization
HSYNC	H_SYNC	29	21	B	I	4	Horizontal Synchronization Detect/Source
VSYNC	V_SYNC	30	22	B	I	4	Vertical Synchronization Source
IRIN	REMOTE	2	2	I		1	Remote Control Capture

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V1, V2, V3 ANALOG OUTPUT
Specifications V_{CC} = 5.25V

V_{CC} = 5.25V	Condition	Limit
Output Voltage	Bit = 11 Bit = 10	4.30V +/– 0.25V 3.20V +/– 0.2V
	Bit = 01 Bit = 00	2.10V +/– 0.15V 0.1V +/– 0.1V
Settling Time	70% of DC Level, 10pf Load	< 50 nsec

V1, V2, V3 ANALOG OUTPUT
Specifications V_{CC} = 4.75V

V_{CC} = 4.75V	Condition	Limit
Output Voltage	Bit = 11 Bit = 10	3.90V +/– 0.25V 2.90V +/– 0.2V
	Bit = 01 Bit = 00	1.90V +/– 0.15V 0.1V +/– 0.1V
Settling Time	70% of DC Level, 10pf Load	< 50 nsec

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DC CHARACTERISTICS

T_A = 0°C to + 70°C; V_{CC} = + 4.75 V to + 5.25V

Symbol	Parameter	TA = 0° to + 70°C Min	Max	Typical @ 25°C	Units	Conditions
V_{IL}	Input Voltage Low	0	0.2 V_{CC}	1.48	V	
V_{IH}	Input Voltage High	0.7 V_{CC}	V_{CC}	3.0	V	
V_{HY}	Schmitt Hysteresis	0.1 V_{CC}		0.8	V	
V_{PU}	Maximum Pull-Up Voltage		13.2		V	[2]
V_{OL}	Output Voltage Low		0.4	0.16	V	I_{OL} = 1.00 mA
			0.4	0.19	V	I_{OL} = mA, [1]
			0.4	0.19	V	I_{OL} =0.75 mA, [2]
V_{OH}	Output Voltage High	V_{CC} –0.4		4.75	V	I_{OH} = –0.75 mA
I_{IR}	Reset Input Current		–80	–46	µA	V_{RL} = 0 V
I_{IL}	Input Leakage	–3.0	3.0	0.01	µA	0 V, V_{CC}
I_{OL}	Tri-State Leakage	–3.0	3.0	0.02	µA	0 V, V_{CC}

[1] Port 0, 1
[2] PWM Open-Drain

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