



Z89303/05/07 DIGITAL TELEVISION CONTROLLER

GENERAL DESCRIPTION

The Z89303/05/07 Digital Television Controllers are application-specific controllers designed to provide complete audio and video control of television receivers, video recorders, with advanced on-screen display facilities. The Z89303/05/07 are 24K, 16K and 12K ROM versions in 52-pin SDIP packages. The powerful 12 MHz Z89C00 RISC processor core allows the user to control the on-board peripheral functions and registers using the standard processor instruction set.

The extensive character attributes can be controlled in two modes: by the on-screen display controller character control mode for maximum display control flexibility, and closed caption mode for optimum display of closed caption text.

Closed caption text can be decoded directly from the composite video signal with the assistance of the processor's digital signal processing capabilities and displayed on the screen. The character representation in this mode allows for a simple attribute control through the insertion of control characters, and each word of RAM specifies two displayed characters.

The character control mode provides access to the full set of attribute controls. Each word of RAM specifies a single displayed character and basic character attributes, allowing the modification of attributes on a character-by-character basis. The insertion of control characters permits direction of other character attributes.

The fully customized 512 character set, formatted in two 256 character banks, can be displayed with a host of display attributes that include underlining, italics, blinking, eight foreground/background colors, character position offset delay, and background transparency. The 16-bit display character representation allows the modification of some key attributes on a character-by-character basis. A character's pixel array is stored as a 16- or 18-word representation in Character Graphics ROM (CGROM). The ROM contents are referenced by a 16-bit word stored in video RAM (VRAM) defining the character type and its key attributes.

Serial interfacing with the television tuner is provided through the tuner serial port. Other serial devices, such as digital channel tuning adjustments, may be accessed through the industry standard I²C port.

Additional hardware provides the capability to display two times normal size characters. The smoothing logic contained in the on-screen display circuit improves the appearance of larger fonts. Fringing circuitry can be activated to improve the visibility of text by surrounding the character lines with a one-pixel border.

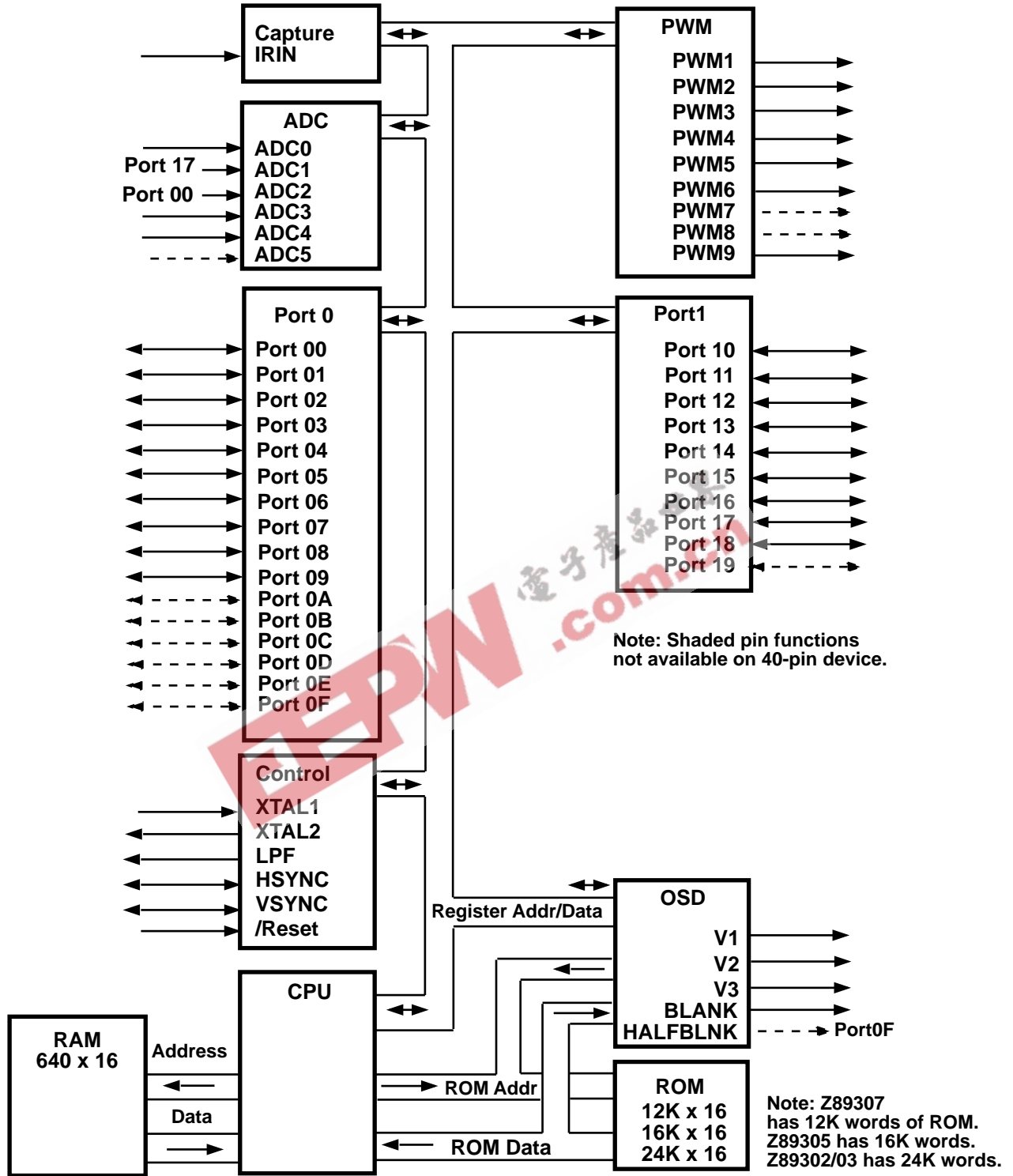
RGB outputs provide the direct video signals, and a blanking output is provided to control the video multiplexor. Dot clock and verticle line synchronization are normally obtained from H_FLYBACK and V_FLYBACK, but can be generated by the Z89303/05/047, and driven to the external deflection unit through the bidirectional SYNC ports when external video synchronization signals are not present.

User control can be monitored through the keypad scanning port, or the 16-bit remote control capture register. Receiver functions such as color and volume can be directly controlled by eight 8-bit pulse width modulated ports.

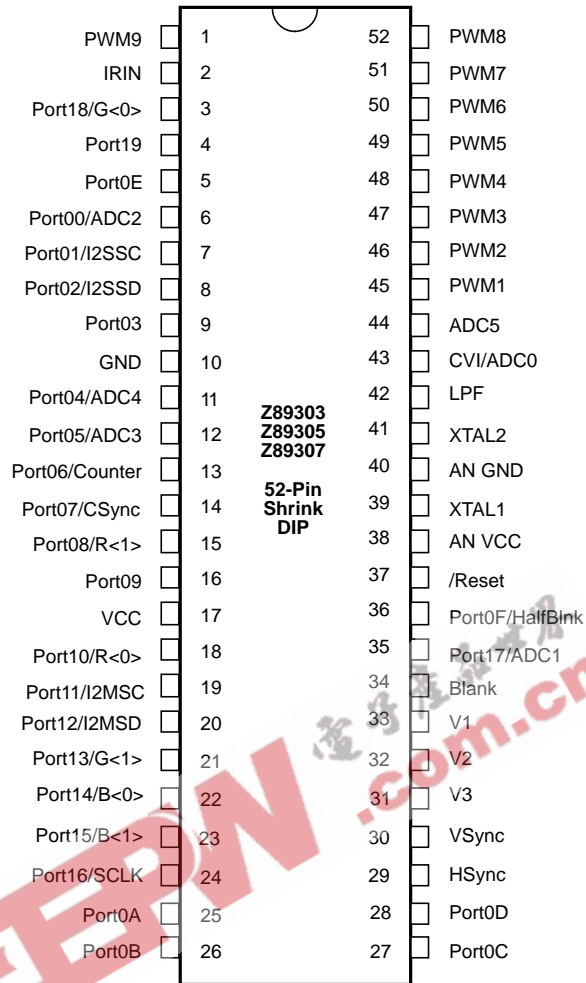
All nine PWM ports are available in the 52-pin package.

The Z89303/05/07 has two internal 12 MHz VCOs that are referenced to a 32 KHz internal oscillator to provide the system clock. In Sleep mode, the controller uses the 32 KHz clock for the system clock to reduce power consumption. The processor can be suspended by placing it into STOP mode when main power is not available for minimal power consumption.

GENERAL DESCRIPTION (Continued)



Functional Block Diagram



52-Pin Shrink DIP Configuration

PIN DESCRIPTIONS
 Z89303/05/07

Pin Name	Function	Z89303/05/07 52-Pin	Configuration	
			Direction	Reset
V _{CC}	+5 V	17,38		PWR
GND	0 V	10,40		PWR
IRIN	Infrared Remote Capture Input	2	I	I
ADC[5:0] ^a	4-Bit Analog to Digital Converter Input ^b	44,11,12,6,35,43	nAI	I
PWM10, PWM9	14-Bit Pulse Width Modulator Output	-,1	OD	O
PWM[8:1] ^c	8-Bit Pulse Width Modulator Output	52,51,50,49, 48,47,46,45	OD	O
Port0[F:0] ^d	Bit Programmable Input/Output Ports	36,5,28,27,26,25, 16,15,14,13,12, 11,9,8,7,6	B	I
Port1[9:0] ^c	Bit Programmable Input/Output Ports	4,3,35,24,23,22, 21,20,19,18	B	I
SCLf	12C Clock I/O	7 or 19	BOD	
SCD ^g	12C Data I/O	8 or 20	BOD	
XTAL1	Crystal Oscillator Input	39	AI	I
XTAL2	Crystal Oscillator Output	41	AO	O
LPF	Loop Filter	42	AB	O
HSYNC	H_Sync	29	B	I
VSYNC	V_Sync	30	B	I
/RESET	Device Reset	37	I	I
V[3:1] (Typically Drive B, G, and R Outputs)	OSD Video Output	31,32,33	O	O
Blank	OSD Blank Output	34	O	O
Half Blank ^h	OSD Half Blank Output	36	O	
RGB Digital Outputs ⁱ	R[1:0],G[1:0], and B[1:0] Outputs of the RGB Matrix	23,22,21, 18,15,3	O	
SCLK ^k	Internal Processor SCLK	24	O	

V1, V2, V3 ANALOG OUTPUT

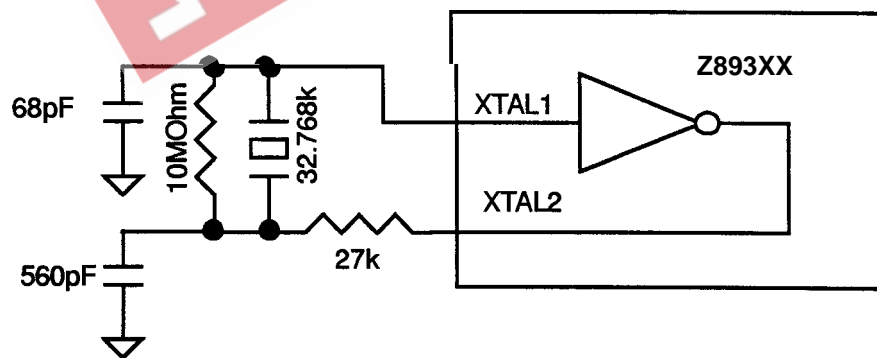
Specifications $V_{CC} = 5.25\text{ V}$

$V_{CC} = 5.25\text{ V}$	Condition	Limit
Output Voltage	Bit = 11	4.55 V +/- 0.25 V
	Bit = 10	3.205V +/- 0.2 V
	Bit = 01	1.95 V +/- 0.15 V
	Bit = 00	0.65 V +/- 0.1 V
Settling Time	70% of DC Level, 10pf Load	< 50 nsec

V1, V2, V3 ANALOG OUTPUT

Specifications $V_{CC} = 4.75\text{V}$

$V_{CC} = 4.75\text{V}$	Condition	Limit
Output Voltage	Bit = 11	3.90 V +/- 0.25 V
	Bit = 10	2.90 V +/- 0.2 V
	Bit = 01	1.90 V +/- 0.15 V
	Bit = 00	0.1 V +/- 0.1 V
Settling Time	70% of DC Level, 10pf Load	< 50 nsec



32K Oscillator Recommended Circuit

Notes:

- c) PWM[8,7] is not available on the 40-pin DIP version.
- d) Port0[F:A] is not available on the 40-pin DIP version.
- e) Port19 is not available on the 40-pin DIP version.
- f) SCL I/O pin is shared with Port0 or Port11.
- g) SCD I/O pin is shared with Port02 or Port12.
- h) Half Blank output is a function shared with Port0F.
Half Blank output is not available on the 40-pin DIP version.
- i) Digital RGB outputs and the internal SCLK are shared with Port1[5:0].
- k) Internal processor SCLK is shared with Port16.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min	Max	Units	Conditions
V_{CC}	Power Supply Voltage	0	7	V	
V_{ID}	Input Voltage	-0.3	$V_{CC} + 0.3$	V	Digital Inputs
V_{IA}	Input Voltage	-0.3	$V_{CC} + 0.3$	V	Analog Inputs (A/D0...A/D4)
V_O	Output Voltage	-0.3	$V_{CC} + 0.3$	V	All Push-Pull Digital Output
V_O	Output Voltage	-0.3	$V_{CC} + 8.0$	V	Open-Drain PWM Outputs (PWM1...PWM8)
I_{OH}	Output Current High		-10	mA	One Pin
I_{OH}	Output Current High		-100	mA	All Pins
I_{OL}	Output Current Low		20	mA	One Pin
I_{OL}	Output Current Low		200	mA	All Pins
T_A	Operating Temperature	0	70	°C	
T_A	Storage Temperature	-65	150	°C	

DC CHARACTERISTICS

$T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$; $V_{CC} = 4.5\text{ V}$ to $+5.5\text{ V}$; $F_{osc} = 32.768\text{ KHz}$

Symbol	Parameter	Min	Max	Typical	Units	Conditions
V_{IL}	Input Voltage Low	0	$0.2 V_{CC}$	0.4	V	
V_{IH}	Input Voltage High	$0.6 V_{CC}$	V_{CC}	3.6	V	
V_{PU}	Max. Pull-Up Voltage		12		V	PWM0...PWM8 Only
V_{OL}	Output Voltage Low		0.4	0.16	V	@ $I_{OL} = 1\text{ mA}$
V_{OL}	Output Voltage High	$V_{CC} - 0.9$		4.75	V	@ $I_{OL} = 0.75\text{ mA}$
V_{XL}	Input Voltage XTAL1 Low		$0.3 V_{CC}$	1.0	V	External Clock
V_{XH}	Input Voltage XTAL1 High	$V_{CC} - 2.0$		3.5	V	Generator Driven
V_{HY}	Schmitt Hysteresis	3.0	0.75	0.5	V	On XTAL1 Input Pin
I_{IR}	Reset Input Current		150	90	μA	$V_{RL} = 0\text{ V}$
I_{IL}	Input Leakage	-3.0	3.0	0.01	μA	@ 0 V and V_{CC}
I_{CC}	Supply Current		100	60	mA	
I_{CC1E}	Supply Current of the OTP		700	300	μA	Sleep Mode @ 32 KHz
I_{CC1}	Supply Current		300	100	μA	Sleep Mode @ 32 KHz
I_{CC2}	Supply Current		10	5	μA	Sleep Mode

AC CHARACTERISTICS
 $T_A = 0^{\circ}\text{C to } +70^{\circ}\text{C}; V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}; F_{OSC} = 32.768 \text{ KHz}$

Symbol	Parameter	Min	Max	Typical	Units
T_{pC}	Input Clock Period	16	100	32	μS
T_{rC}, T_{fC}	Clock Input Rise and Fall			12	μS
$T_{D,POR}$	Power On Reset Delay	0.8		1.2	s

AC CHARACTERISTICS
 $T_A = 0^{\circ}\text{C to } +70^{\circ}\text{C}; V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}; F_{OSC} = 32.768 \text{ KHz}$

Symbol	Parameter	Min	Max	Typical	Units
$T_{w,RES}$	Power-On Reset Min. Width		5TPC		μS
T_{D,H_S}	H_Sync Incoming Signal Width	5.5	12.5	11	μS
T_{D,V_S}	V_Sync Incoming Signal Width	0.15	1.5	1.0	mS
T_{D,E_S}	Time Delay Between Leading Edge of V_Sync and H_Sync in Even Field	-12	+12	0	μS
T_{D,O_S}	Time Delay Between Leading Edge of H_Sync in Odd Field	20	44	32	μS
T_{w,HV_S}	H_Sync/V_Sync Edge Width		2.0	0.5	μS

Notes:

All timing of the I²C bus interface are defined by related specifications of the I²C bus interface.

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