



# Z90110/120/130

## 40-PIN LOW-COST DIGITAL TELEVISION CONTROLLER

### FEATURES

Part	ROM (KB)	RAM* (Kbyte)	Speed (MHz)
Z90110	4	236	4
Z90120	6	236	4
Z90130	8	236	4

\*General-Purpose

- n 40-Pin DIP Package
- n 4.5V to 5.5V Operating Range
- n 0°C to +70°C Temperature Range
- n Low-Power Consumption

- n On-Screen Display (OSD) Logic Circuits
- n One 14-Bit and Three 6-Bit Pulse Width Modulator (PWM) Circuits
- n 24 Input/Output Lines
- n Program Memory, Video RAM, and Register File Address Spaces
- n Two On-Chip Counter/Timers

### GENERAL DESCRIPTION

The Z901XX 40-pin Digital Television Controller is a cost-effective member of the Z8® single-chip microcontroller family. The device provides an ideal performance and reliability solution for consumer and industrial television applications.

The Z901XX offers mask-programmed ROM, which enables the Z8 microcontroller to be used in a high-volume production application device embedded with a custom program (customer-supplied program) and combines to provide support for mid-range and low-end TV applications.

The device features an 8-bit internal data path controlled by a Z8 microcontroller, On-Screen Display (OSD) logic circuits, and Pulse Width Modulators (PWM). On-chip peripherals include two register mapped I/O ports (Ports 2 and Port 3), interrupt control logic (one software, two external and three internal interrupts) and a standby mode recovery input port (Port 3, pin P30).

The OSD control circuits support six rows by 20 columns of characters. The character color is specified by row. One of the eight rows is assigned to show two kinds of colors for bar type displays such as volume control. The OSD is capable of displaying either low resolution (5x7 dot pattern) or high resolution (11x15 dot pattern) characters.

A 14-bit PWM port provides enough voltage resolution for a voltage synthesizer tuning system. Three 6-bit PWM ports are used for controlling audio signal levels, and Three 8-bit PWM ports used to vary picture levels.

Three basic address spaces, The Program Memory, Video RAM, and Register File, support a wide range of memory configurations.

For applications demanding powerful I/O capabilities, the Z901XX's dedicated input and output lines are grouped into three ports, and are configurable under software control to provide timing, status signals, parallel I/O and an address/data bus for interfacing to external memory.

To unburden the program from coping with the real-time problems such as counting/timing and data communication, the Z901XX offers two on-chip counter/timers with a large number of user selectable modes.

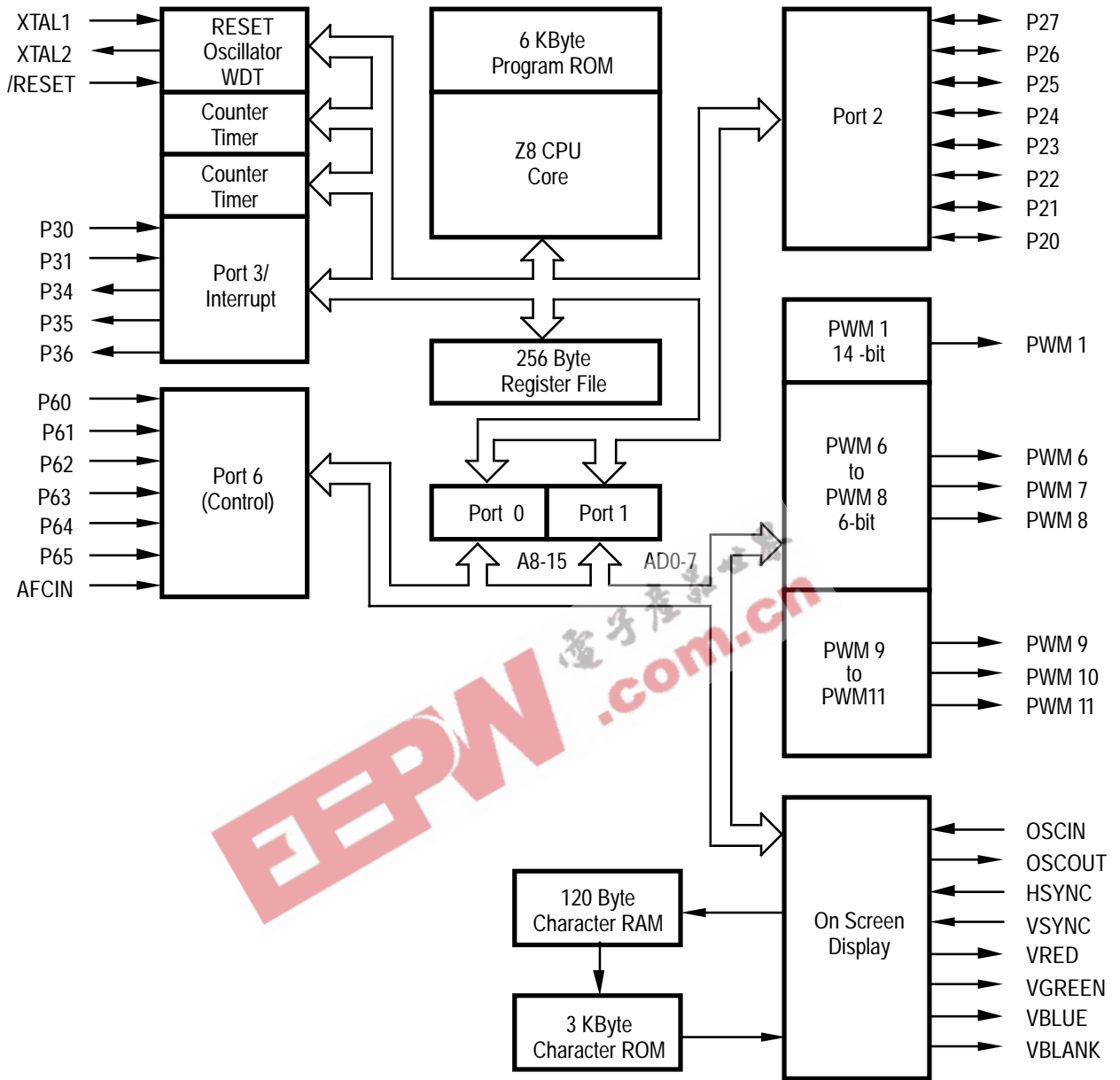
#### Notes:

All Signals with a preceding front slash, "/", are active Low, e.g.: B/W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

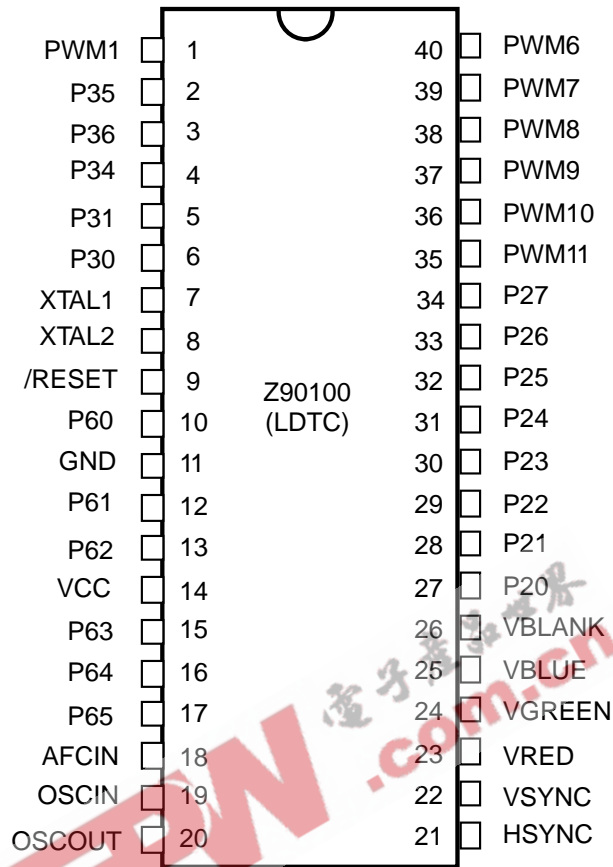
Connection	Circuit	Device
Power	V <sub>CC</sub>	V <sub>DD</sub>
Ground	GND	V <sub>SS</sub>

GENERAL DESCRIPTION (Continued)



Functional Block Diagram

PIN CONFIGURATION



40-Pin Mask-ROM Plastic DIP

## ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational

sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Symbol	Parameters	Min	Max	Units	Notes
$V_{CC}$	Power Supply Voltage*	-0.3	+7	V	
$V_I$	Input Voltage	-0.3	$V_{CC}+0.3$	V	
$V_I$	Input Voltage	-0.3	$V_{CC}+0.3$	V	[1]
$V_O$	Output Voltage	-0.3	$V_{CC}+8.0$	V	[2,3]
$I_{OH}$	Output Current High		-10	mA	1 pin
$I_{OH}$	Output Current High		-100	mA	All total
$I_{OL}$	Output Current Low		20	mA	1 pin
$I_{OL}$	Output Current Low		200	mA	All total
$T_A$	Operating Temperature	†			
$T_{STG}$	Storage Temperature	-65	+150	C	

### Notes:

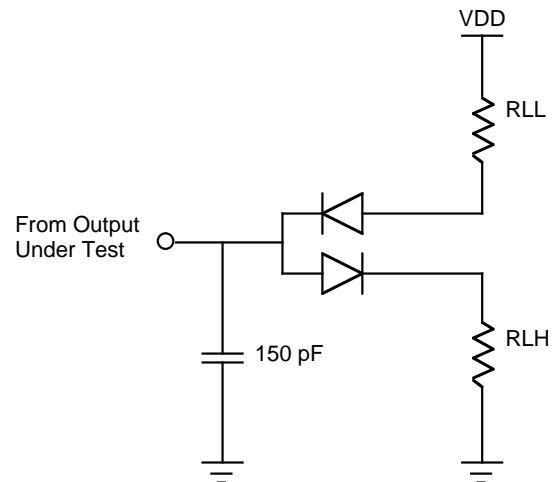
- [1] Port 2 open-drain
- [2] PWM open-drain outputs
- [3] PWM breakdown is 13.2V (normal operation). Will withstand 16V max. (non-momentary operating).

\* Voltage on all pins with respect to GND.

† See Ordering Information

## STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (Test Load Diagram).



Test Load Diagram

### CAPACITANCE

$T_A=25^\circ\text{C}$ ;  $V_{CC}=\text{GND}=0\text{V}$ ; Freq=1.0 MHz; unmeasured pins to GND.

Parameter	Max	Units
Input capacitance	10	pF
Output capacitance	20	pF
I/O capacitance	25	pF
AFC <sub>IN</sub> input capacitance	10	pF

### DC CHARACTERISTICS

$T_A=0^\circ\text{C}$  to  $+70^\circ\text{C}$ ;  $V_{CC}=+4.5\text{V}$  to  $+5.5\text{V}$ ;  $F_{\text{OSC}}=4$  MHz

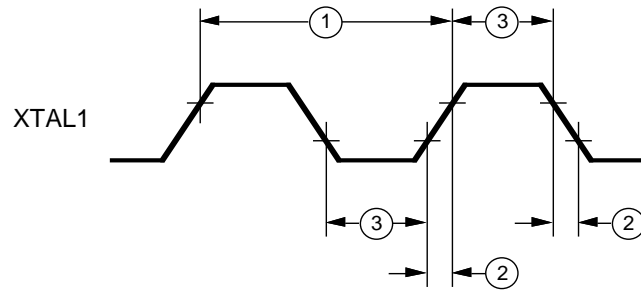
Sym	Parameter	$T_A=0^\circ\text{C}$ to $+70^\circ\text{C}$		Typical @ 25°C	Units	Conditions
		Min	Max			
$V_{\text{IL}}$	Input Voltage Low	0	$0.2 V_{\text{CC}}$	1.48	V	
$V_{\text{ILC}}$	Input XTAL/Osc In Low		$0.07 V_{\text{CC}}$	0.98	V	External Clock Generator Driven
$V_{\text{IH}}$	Input Voltage XTAL/Osc In High	$0.7 V_{\text{CC}}$	$V_{\text{CC}}$	3.2	V	External Clock Generator Driven
$V_{\text{IHC}}$	Input XTAL/Osc In High	$0.8 V_{\text{CC}}$	$V_{\text{CC}}$	3.0	V	External Clock Generator Driven
$V_{\text{HY}}$	Schmitt Hysteresis	$0.1 V_{\text{CC}}$		0.8	V	
$V_{\text{PU}}$	Maximum Pull-Up Voltage		12		V	[1]
$V_{\text{OL}}$	Output Voltage Low		0.4	0.16	V	$I_{\text{OL}}=1.00$ mA
			0.4	0.19	V	$I_{\text{OL}}=0.75$ mA [1]
$V_{00-01}$	AFC Level 01 In		$0.45 V_{\text{CC}}$	1.9	V	
$V_{01-11}$	AFC Level 11 In	$0.5 V_{\text{CC}}$	$0.75 V_{\text{CC}}$	3.12	V	
$V_{\text{OH}}$	Output Voltage High	$V_{\text{CC}}-0.4$		4.75	V	$I_{\text{OH}}=-0.75$ mA
$I_{\text{IR}}$	Reset Input Current		-80	-46	$\mu\text{A}$	$V_{\text{RL}}=0\text{V}$
$I_{\text{IL}}$	Input Leakage	-3.0	3.0	0.01	$\mu\text{A}$	$0\text{V}, V_{\text{CC}}$
$I_{\text{OL}}$	Tri-State Leakage	-3.0	3.0	0.02	$\mu\text{A}$	$0\text{V}, V_{\text{CC}}$
$I_{\text{CC}}$	Supply Current		20	13.2	mA	All inputs at rail
$I_{\text{CC1}}$			6	3.2	mA	All inputs at rail
$I_{\text{CC2}}$			10	2.0	$\mu\text{A}$	All inputs at rail

**Note:**

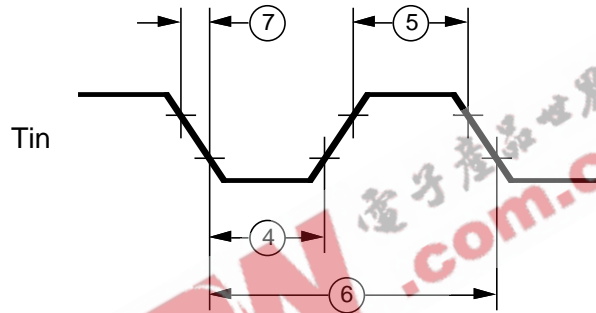
[1] PWM open-drain

### AC CHARACTERISTICS

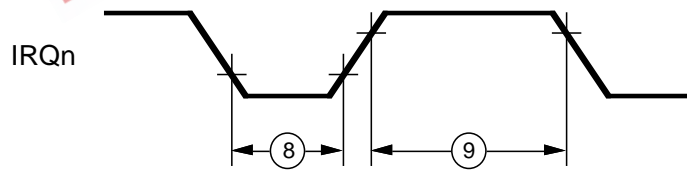
Timing Diagrams



External Clock

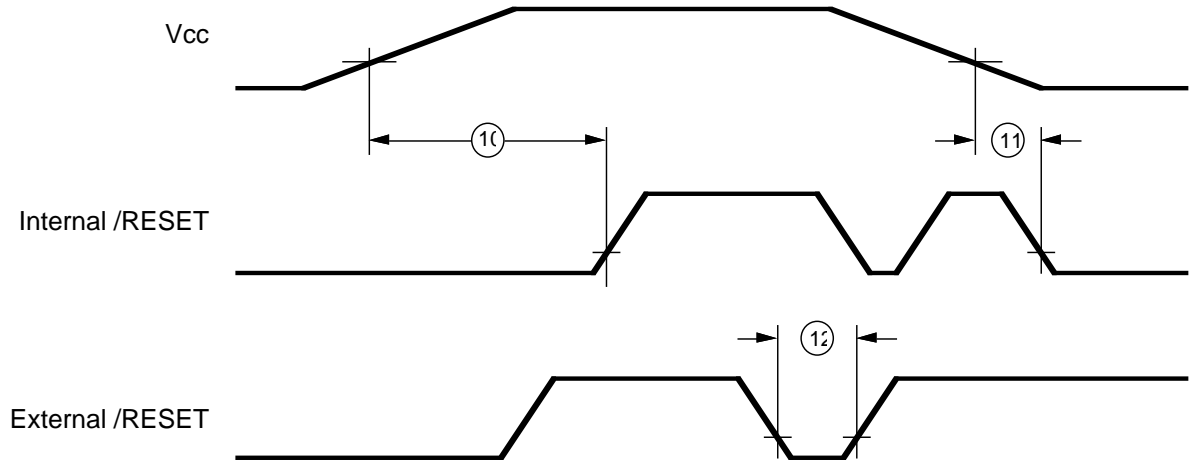


Counter Timer

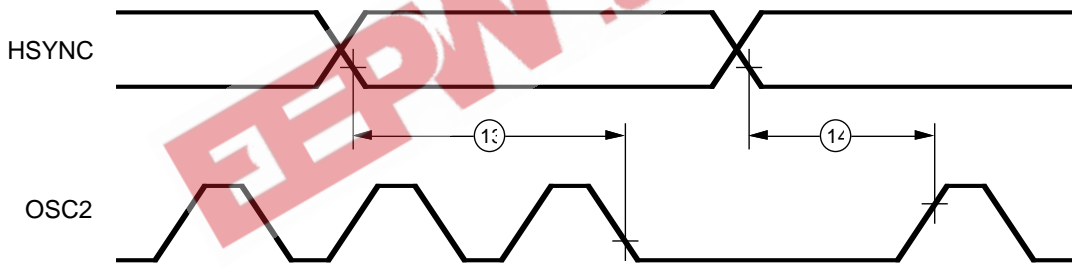


Interrupt Request

**AC CHARACTERISTICS**  
Timing Diagrams (Continued)



Power-On Reset



On-Screen Display

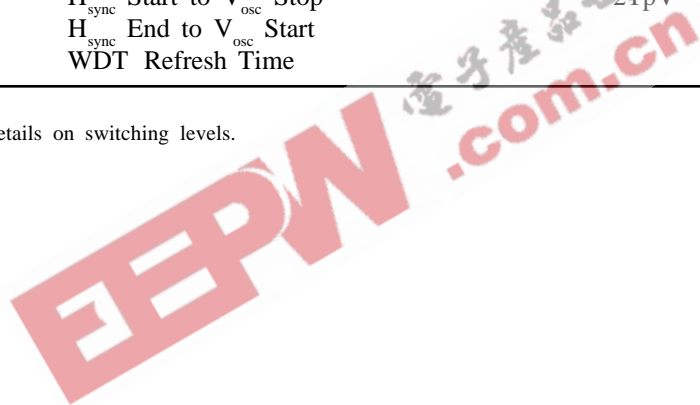
**AC CHARACTERISTICS**

$T_A = 0^\circ \text{C}$  to  $+70^\circ \text{C}$ ;  $V_{CC} = +4.5\text{V}$  to  $+5.5\text{V}$ ;  $F_{OSC} = 4 \text{ MHz}$

No	Symbol	Parameter	Min	Max	Unit
1	TpC	Input Clock Period	250	1000	ns
2	TrC,TfC	Clock Input Rise and Fall		15	ns
3	TwC	Input Clock Width	70		ns
4	TwTinL	Timer Input Low Width	70		ns
5	TwTinH	Timer Input High Width	3TpC		
6	TpTin	Timer Input Period	8TpC		
7	TrTin,TfTin	Timer Input Rise and Fall		100	ns
8 a	TwIL	Int Req Input Low	70		ns
8 b	TwIL		3TpC		
9	TwIH	Int Request Input High	3TpC		
10	TdPOR	Power On Reset Delay	25	100	ms
11	TdLVIRES	Low Voltage Detect to Internal RESET Condition	200		ns
12	TwRES	Reset Minimum Width	5TpC		
13	TdHsOI	$H_{sync}$ Start to $V_{osc}$ Stop	2TpV	3TpV	
14	TdHsOh	$H_{sync}$ End to $V_{osc}$ Start		1TpV	
15	TdWDT	WDT Refresh Time		12	ms

**Note:**

Refer to DC Characteristics for details on switching levels.



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