Z8E001

CMOS OTP MICROCONTROLLER

FEATURES

Part Number	ROM (KB)	RAM* (Bytes)	Speed (MHz)
Z8E001	1	64	10

* General-Purpose

Microcontroller Core Features

- All Instructions Execute in one 1 µs Instruction Cycle with 10 MHz Crystal
- 1K x 8 On-Chip OTP EPROM Memory
- 64 x 8 General-Purpose Registers (SRAM)
- Six Vectored Interrupts with Fixed Priority
- Operating Speed: DC - 10 MHz
- Six Addressing Modes: R, IR, X, D, RA, & IM

Peripheral Features

- 13 Total Input/Output Pins
- One 8-Bit I/O Port (Port A)
  - I/O Bit Programmable
  - Each Bit Programmable as Push-Pull or Open-Drain
- One 5-Bit I/O Port (Port B)
  - I/O Bit Programmable
  - Includes Special Functionality:
    Stop-Mode Recovery Input
    Comparator Inputs
    Selectable Edge Interrupts
    Timer Output
- One Analog Comparator
- 16-Bit Programmable Watch-Dog Timer (WDT)
- Software Programmable Timers Configurable as:
  - Two 8-Bit Standard Timers and One 16-Bit Standard Timer or
  - One 16-Bit Standard Timer and One 16-Bit Pulse Width Modulator (PWM) Timer

Additional Features

- On-Chip Oscillator that Accepts XTAL, Ceramic Resonator, LC, or External Clock
- Programmable Options:
  - EPROM Protect
- Power Reduction Modes:
  - HALT Mode with Peripheral Units Active
  - STOP Mode with all Functionality Shut Down

CMOS/Technology Features

- Low-Power Consumption
- 3.0V to 5.5V Operating Range @ 0°C to +70°C
  4.5V to 5.5V Operating Range @ -40°C to +105°C
- 18-Pin DIP,SOIC, and 20-Pin SSOP Packages.

GENERAL DESCRIPTION

Zilog's Z8E001 Microcontroller (MCU) is a One-Time Programmable (OTP) member of Zilog's single-chip Z8^{Plus} MCU family that allows easy software development, debug, prototyping, and small production runs not economically desirable with masked ROM versions.

For applications demanding powerful I/O capabilities, the Z8E001's dedicated input and output lines are grouped into two ports, and are configurable under software control.

Both 8-bit and 16-bit on-chip timers, with a large number of user selectable modes, offload the system of administering real-time tasks such as counting/timing and I/O data communications.

Note: All signals with a preceding front slash, "/", are active Low. For example, B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

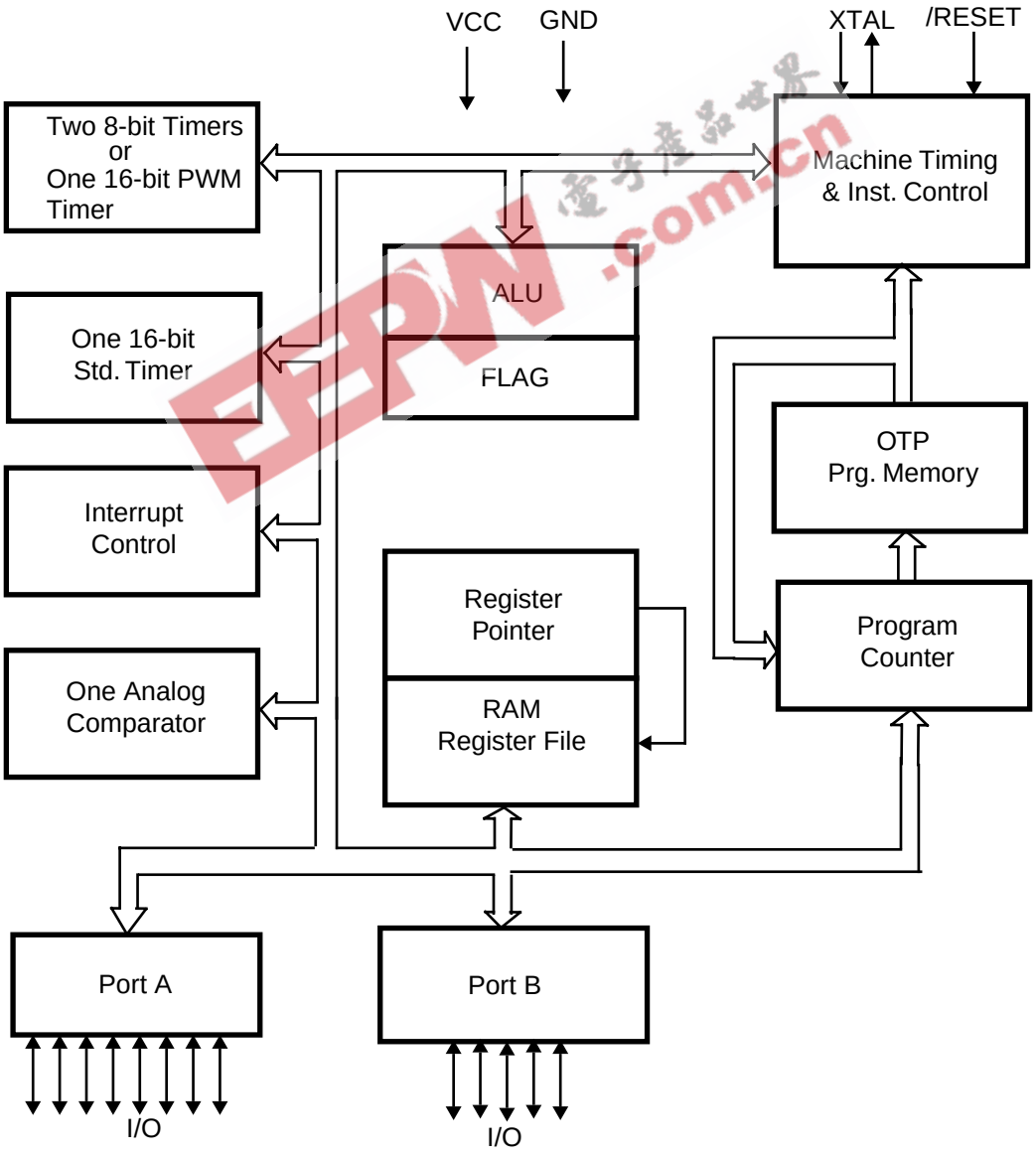


Figure 1. Functional Block Diagram

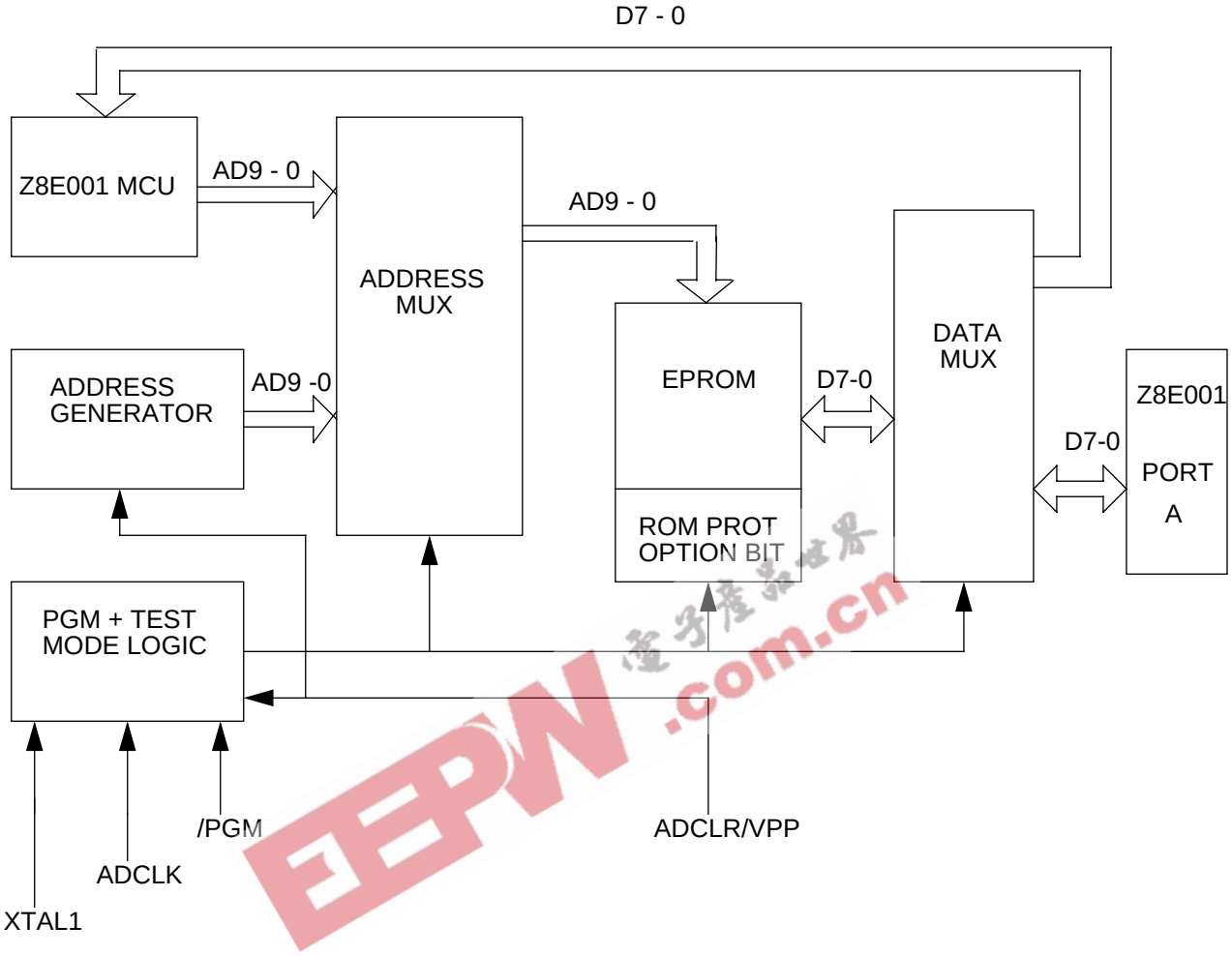


Figure 2. EPROM Programming Mode Block Diagram

PIN DESCRIPTION

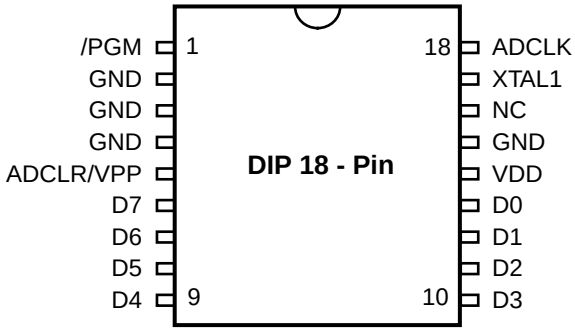


Figure 3. 18-Pin DIP/SOIC Pin Identification/EPROM Programming Mode

Table 1. 18-Pin DIP/SOIC Pin Assignments/EPROM Programming Mode

EPROM Programming Mode			
Pin #	**Symbol**	**Function**	**Direction**
1	/PGM	Prog Mode	Input
2-4	GND	Ground	
5	ADCLR/V_{PP}	Clear Clk./Prog Volt.	Input
6-9	D7-D4	Data 7,6,5,4	In/Output
10-13	D3-D0	Data 3,2,1,0	In/Output
14	V_{DD}	Power Supply	
15	GND	Ground	
16	NC	No Connection	
17	XTAL1	1MHz Clock	Input
18	ADCLK	Address Clock	Input

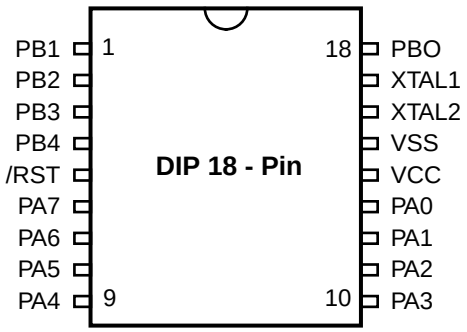


Figure 4. 18-Pin DIP/SOIC Pin Identification

Table 2. 18-Pin DIP/SOIC Pin Assignments

Standard Mode

Pin #	Symbol	Function	Direction
1–4	PB1–PB4	Port B, Pins 1,2,3,4	In/Output
5	/RESET	Reset	Input
6-9	PA7-PA4	Port A, Pins 7,6,5,4	In/Output
10-13	PA3-PA0	Port A, Pins 3,2,1,0	In/Output
14	V_{CC}	Power Supply	
15	V_{SS}	Ground	
16	XTAL2	Crystal Osc. Clock	Output
17	XTAL1	Crystal Osc. Clock	Input
18	PB0	Port B, Pin 0	In/Output

PIN DESCRIPTION (Continued)

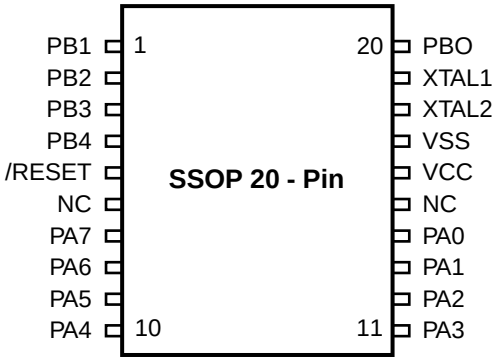


Figure 5. 20-Pin SSOP Pin Identification

Table 3. 20-Pin SSOP Pin Assignments

Standard Mode

Pin #	Symbol	Function	Direction
1–4	PB1–PB4	Port B, Pins 1,2,3,4	In/Output
5	/RESET	Reset	Input
6	NC	No Connection	
7-10	PA7-PA4	Port A, Pins 7,6,5,4	In/Output
11-14	PA3-PA0	Port A, Pins 3,2,1,0	In/Output
15	NC	No Connection	
16	V_{CC}	Power Supply	
17	V_{SS}	Ground	
18	XTAL2	Crystal Osc. Clock	Output
19	XTAL1	Crystal Osc. Clock	Input
20	PB0	Port B, Pin 0	In/Output

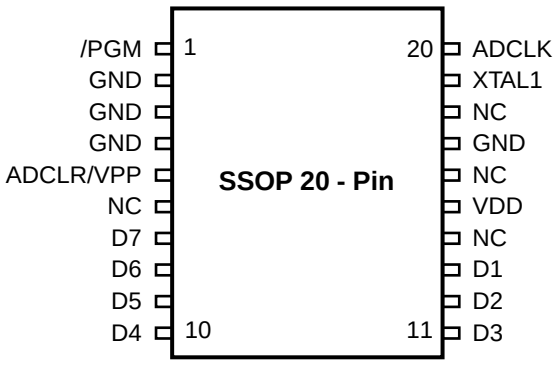


Figure 6. 20-Pin SSOP Pin Identification/EPROM Programming Mode

Table 4. 20-Pin SSOP Pin Assignments/EPROM Programming Mode

EPROM Programming Mode			
Pin #	**Symbol**	**Function**	**Direction**
1	/PGM	Prog Mode	Input
2-4	GND	Ground	
5	ADCLR/V_{PP}	Clear Clk./Prog Volt.	Input
6	NC	No Connection	
7-10	D7-D4	Data 7,6,5,4	In/Output
11-14	D3-D0	Data 3,2,1,0	In/Output
15	NC	No Connection	
16	V_{DD}	Power Supply	
17	GND	Ground	
18	NC	No Connection	
19	XTAL1	1MHz Clock	Input
20	ADCLK	Address Clock	Input

ABSOLUTE MAXIMUM RATINGS

Parameter	Min	Max	Units	Note
Ambient Temperature under Bias	–40	+105	C	
Storage Temperature	–65	+150	C	
Voltage on any Pin with Respect to V_{SS}	–0.6	+7	V	1
Voltage on V_{DD} Pin with Respect to V_{SS}	–0.3	+7	V	
Voltage on /RESET Pin with Respect to V_{SS}	–0.6	V_{DD}+1	V	2
Total Power Dissipation		880	mW	
Maximum Allowable Current out of V_{SS}		80	mA	
Maximum Allowable Current into V_{DD}		80	mA	
Maximum Allowable Current into an Input Pin	–600	+600	µA	3
Maximum Allowable Current into an Open-Drain Pin	–600	+600	µA	4
Maximum Allowable Output Current Sunk by Any I/O Pin		25	mA	
Maximum Allowable Output Current Sourced by Any I/O Pin		25	mA	
Maximum Allowable Output Current Sunk by Port A		40	mA	
Maximum Allowable Output Current Sourced by Port A		40	mA	
Maximum Allowable Output Current Sunk by Port B		40	mA	
Maximum Allowable Output Current Sourced by Port B		40	mA	

Notes:
1. This applies to all pins except the /RESET pin and where otherwise noted.
2. There is no input protection diode from pin to V_{DD}.
3. This excludes XTAL pins.
4. Device pin is not at an output Low state.

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability. Total power dissipation should not exceed 880 mW for the package. Power dissipation is calculated as follows:

Total Power Dissipation = V_{DD} x [I_{DD} - (sum of I_{OH})]
+ sum of [(V_{DD} - V_{OH}) x I_{OH}]
+ sum of (V_{0L} x I_{0L})

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to Ground. Positive current flows into the referenced pin (Figure 7).

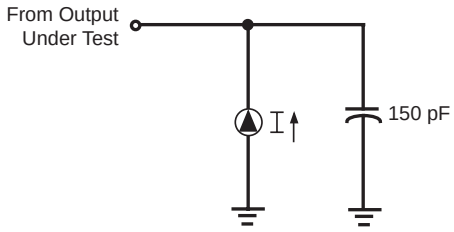


Figure 7. Test Load Diagram

CAPACITANCE

T_A = 25°C, V_{CC} = GND = 0V, f = 1.0 MHz, unmeasured pins returned to GND.

Parameter	Min	Max
Input capacitance	0	12 pF
Output capacitance	0	12 pF
I/O capacitance	0	12 pF

DC ELECTRICAL CHARACTERISTICS

			T_A = 0°C to +70 °C		Typical [1]			
Sym	**Parameter**	**V_{CC} [3]**	**Min**	**Max**	**@ 25°C**	**Units**	**Conditions**	**Notes**
V_{CH}	Clock Input High Voltage	3.0V	$0.7V_{CC}$	V_{CC}+0.3	1.3	V	Driven by External Clock Generator	
		5.5V	$0.7V_{CC}$	V_{CC}+0.3	2.5	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	3.0V	V_{SS}–0.3	$0.2V_{CC}$	0.7	V	Driven by External Clock Generator	
		5.5V	V_{SS}–0.3	$0.2V_{CC}$	1.5	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	3.0V	$0.7V_{CC}$	V_{CC}+0.3	1.3	V		
		5.5V	$0.7V_{CC}$	V_{CC}+0.3	2.5	V		
V_{IL}	Input Low Voltage	3.0V	V_{SS}–0.3	$0.2V_{CC}$	0.7	V		
		5.5V	V_{SS}–0.3	$0.2V_{CC}$	1.5	V		
V_{OH}	Output High Voltage	3.0V	V_{CC}–0.4		3.1	V	I_{OH} = –2.0 mA	
		5.5V	V_{CC}–0.4		4.8	V	I_{OH} = –2.0 mA	
V_{OL1}	Output Low Voltage	3.0V		0.6	0.2	V	I_{OL} = +4.0 mA	
		5.5V		0.4	0.1	V	I_{OL} = +4.0 mA	
V_{OL2}	Output Low Voltage	3.0V		1.2	0.5	V	I_{OL} = +6 mA,	
		5.5V		1.2	0.5	V	I_{OL} = +12 mA,	
V_{RH}	Reset Input High Voltage	3.0V	$0.5V_{CC}$	V_{CC}	1.1	V		
		5.5V	$0.5V_{CC}$	V_{CC}	2.2	V		
V_{RL}	Reset Input Low Voltage	3.0V	V_{SS}–0.3	$0.2V_{CC}$	0.9	V		
		5.5V	V_{SS}–0.3	$0.2V_{CC}$	1.4	V		
V_{OFFSET}	Comparator Input Offset Voltage	3.0V		25.0	10.0	mV		
		5.5V		25.0	10.0	mV		
I_{IL}	Input Leakage	3.0V	–1.0	2.0	0.064	µA	V_{IN} = 0V, V_{CC}	
		5.5V	–1.0	2.0	0.064	µA	V_{IN} = 0V, V_{CC}	
I_{OL}	Output Leakage	3.0V	–1.0	2.0	0.114	µA	V_{IN} = 0V, V_{CC}	
		5.5V	–1.0	2.0	0.114	µA	V_{IN} = 0V, V_{CC}	
V_{ICR}	Comparator Input Common Mode Voltage Range	3.0V	V_{SS}–0.3	V_{CC} –1.0		V		7
		5.5V	V_{SS}–0.3	V_{CC} –1.0		V		7
I_{IR}	Reset Input Current	3.0V	-10	-60	-30	µA		
		5.5V	-20	-180	-100	µA		
I_{CC}	Supply Current	3.0V		2.5	2.0	mA	@ 10 MHz	4,5
		5.5V		6.0	4.0	mA	@ 10 MHz	4,5
I_{CC1}	Standby Current	3.0V		2.0	1.0	mA	HALT Mode V_{IN} = 0V,V_{CC} @ 10 MHz	4,5
		5.5V		2.0	1.0	mA	HALT Mode V_{IN} = 0V,V_{CC} @ 10 MHz	4,5

Sym	Parameter	V_{CC} [3]	T_A = 0 °C to +70 °C Min	Max	Typical [1] @ 25°C	Units	Conditions	Notes
I_{CC2}	Standby Current	3.0V		500	150	nA	STOP Mode V_{IN} = 0V, V_{CC}	6
		5.5V		500	250	nA	STOP Mode V_{IN} = 0V,V_{CC}	6

Notes:
1. Typical values are measured at V_{CC} = 3.3V and V_{CC} = 5.0V.
2. V_{SS} = 0V = GND
3. The V_{CC} voltage specification of 3.0 V guarantees 3.3 V +/- 0.3 V and the V_{CC} voltage specification of 5.5 V guarantees 5.0 V +/- 0.5 V.
4. All outputs unloaded, I/O pins floating, and all inputs are at V_{CC} or V_{SS} level.
5. CL1 = CL2 = 22 pF.
6. Same as note [4] except inputs at V_{CC}.
7. For analog comparator input when analog comparator is enabled.

DC ELECTRICAL CHARACTERISTICS (Continued)

Sym	Parameter	V_{CC} [3]	T_A = -40°C to +105°C Min	Max	Typical [1] @ 25°C	Units	Conditions	Notes
V_{CH}	Clock Input High Voltage	4.5V	0.7 V_{CC}	V_{CC}+0.3	2.5	V	Driven by External Clock Generator	
		5.5V	0.7 V_{CC}	V_{CC}+0.3	2.5	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	4.5V	V_{SS}–0.3	0.2 V_{CC}	1.5	V	Driven by External Clock Generator	
		5.5V	V_{SS}–0.3	0.2 V_{CC}	1.5	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	4.5V	0.7 V_{CC}	V_{CC}+0.3	2.5	V		
		5.5V	0.7 V_{CC}	V_{CC}+0.3	2.5	V		
V_{IL}	Input Low Voltage	4.5V	V_{SS}–0.3	0.2 V_{CC}	1.5	V		
		5.5V	V_{SS}–0.3	0.2 V_{CC}	1.5	V		
V_{OH}	Output High Voltage	4.5V	V_{CC}–0.4		4.8	V	I_{OH} = –2.0 mA	
		5.5V	V_{CC}–0.4		4.8	V	I_{OH} = –2.0 mA	
V_{OL1}	Output Low Voltage	4.5V		0.4	0.1	V	I_{OL} = +4.0 mA	
		5.5V		0.4	0.1	V	I_{OL} = +4.0 mA	
V_{OL2}	Output Low Voltage	4.5V		1.2	0.5	V	I_{OL} = +12 mA,	
		5.5V		1.2	0.5	V	I_{OL} = +12 mA,	
V_{RH}	Reset Input High Voltage	4.5V	0.5V_{CC}	V_{CC}	1.1	V		
		5.5V	0.5V_{CC}	V_{CC}	2.2	V		
V_{OFFSET}	Comparator Input Offset Voltage	4.5V		25.0	10.0	mV		
		5.5V		25.0	10.0	mV		
I_{IL}	Input Leakage	4.5V	-1.0	2.0	<1.0	µA	V_{IN} = 0V, V_{CC}	
		5.5V	-1.0	2.0	<1.0	µA	V_{IN} = 0V, V_{CC}	
I_{OL}	Output Leakage	4.5V	-1.0	2.0	<1.0	µA	V_{IN} = 0V, V_{CC}	
		5.5V	-1.0	2.0	<1.0	µA	V_{IN} = 0V, V_{CC}	
V_{ICR}	Comparator Input Common Mode Voltage Range	4.5V	0	V_{CC} –1.5V		V		7
		5.5V	0	V_{CC} –1.5V		V		7
I_{IR}	Reset Input Current	4.5V	-18	-180	-112	µA		
		5.5V	-18	-180	-112	µA		
I_{CC}	Supply Current	4.5V		7.0	4.0	mA	@ 10 MHz	4,5
		5.5V		7.0	4.0	mA	@ 10 MHz	4,5
I_{CC1}	Standby Current	4.5V		2.0	1.0	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 10 MHz	4,5
		5.5V		2.0	1.0	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 10 MHz	4,5

Sym	Parameter	V_{CC}[3]	T_A = -40 °C to +105 °C Min	Max	Typical [1] @ 25°C	Units	Conditions	Notes
I_{CC2}	Standby Current	4.5V		700	250	nA	STOP Mode V_{IN} = 0V, V_{CC}	6
		5.5V		700	250	nA	STOP Mode V_{IN} = 0V, V_{CC}	6

Notes:

1. Typical values are measured at V_{CC} = 3.3V and V_{CC} = 5.0V.
2. V_{SS} = 0V = GND
3. The V_{CC} voltage specification of 3.0 V guarantees 3.3 V +/- 0.3 V and the V_{CC} voltage specification of 5.5 V guarantees 5.0 V +/- 0.5 V.
4. All outputs unloaded, I/O pins floating, and all inputs are at V_{CC} or V_{SS} level.
5. CL1 = CL2 = 22 pF.
6. Same as note [4] except inputs at V_{CC}.
7. For analog comparator input when analog comparator is enabled.

AC ELECTRICAL CHARACTERISTICS

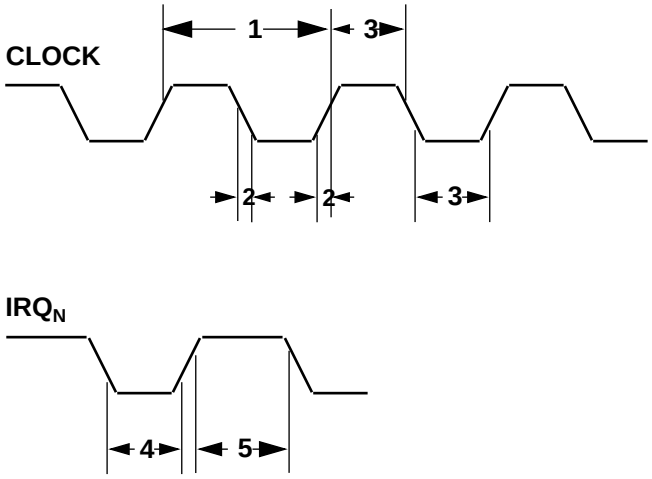


Figure 8. AC Electrical Timing Diagram

Additional Table

			T_A= 0 °C to +70 °C 10 MHz				
No	Symbol	Parameter	V_{CC} [2]	Min	Max	Units	Notes
1	TpC	Input Clock Period	3.0V	100	DC	ns	1
			5.5V	100	DC	ns	1
2	TrC,TfC	Clock Input Rise and Fall Times	3.0V		15	ns	1
			5.5V		15	ns	1
3	TwC	Input Clock Width	3.0V	50		ns	1
			5.5V	50		ns	1
4	TwIL	Int. Request Input Low Time	3.0V	70		ns	1
			5.5V	70		ns	1
5	TwIH	Int. Request Input High Time	3.0V	5TpC			1
			5.5V	5TpC			1
6	Twsm	STOP Mode Recovery Width Spec.	3.0V	12		ns	
			5.5V	12		ns	
7	Tost	Oscillator Start-Up Time	3.0V		5TpC		
			5.5V		5TpC		

Notes:
1. Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. The V_{DD} voltage specification of 3.0V guarantees 3.3V +/- 0.3V. The V_{DD} voltage specification of 5.5V guarantees 5.0V +/- 0.5V.

			T_A= –40 °C to +105 °C 10 MHz				
No	Symbol	Parameter	V_{CC} [2]	Min	Max	Units	Notes
1	TpC	Input Clock Period	4.5V	100	DC	ns	1
			5.5V	100	DC	ns	1
2	TrC,TfC	Clock Input Rise and Fall Times	4.5V		15	ns	1
			5.5V		15	ns	1
3	TwC	Input Clock Width	4.5V	50		ns	1
			5.5V	50		ns	1
4	TwIL	Int. Request Input Low Time	4.5V	70		ns	1
			5.5V	70		ns	1
5	TwIH	Int. Request Input High Time	4.5V	5TpC			1
			5.5V	5TpC			1
6	Twsm	STOP Mode Recovery Width Spec.	4.5V	12		ns	
			5.5V	12		ns	
7	Tost	Oscillator Start-Up Time	4.5V		5TpC		
			5.5V		5TpC		

Notes:
1. Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. The V_{DD} voltage specification of 3.0V guarantees 3.3V +/- 0.3V. The V_{DD} voltage specification of 5.5V guarantees 5.0V +/- 0.5V.

Z8PLUS CORE

The Z8E001 is based on the Zilog Z8Plus Core Architecture. This core is capable of addressing up to 64KBytes of program memory and 4KBytes of RAM. Register RAM is accessed as either 8 or 16 bit registers using a combination of 4, 8, and 12 bit addressing modes. The architecture supports up to 15 vectored interrupts from external and internal sources. The processor decodes 44 CISC instructions using six addressing modes. See the Z8Plus User's Manual (UM97Z8X0300) for more information.

RESET

This section describes the Z8E001 reset conditions, reset timing, and register initialization procedures. Reset is generated by the Reset Pin, Watch-Dog Timer (WDT), and Stop-Mode Recovery (SMR).

A system reset overrides all other operating conditions and puts the Z8E001 into a known state. To initialize the chip's internal logic, the /RESET input must be held Low for at least 30 XTAL clock cycles. The control registers and ports are reset to their default conditions after a reset from the /RESET pin. The control registers and ports are not reset to their default conditions after wakeup from Stop Mode or WDT timeout.

During RESET, the program counter is loaded with 0020H. I/O ports and control registers are configured to their default reset state. Resetting the Z8E001 does not effect the contents of the general-purpose registers.

RESET PIN OPERATION

The Z8E001 hardware /RESET pin initializes the control and peripheral registers, as shown in Table 4. Specific reset values are shown by 1 or 0, while bits whose states are unchanged are indicated by the letter U.

/RESET must be held low until the oscillator stabilizes, then for an additional 30 XTAL clock cycles to be sure that the internal reset is complete. The /RESET pin has a Schmitt-Trigger input with a trip point. There is no high side protection diode. The user should place an external diode from /RESET to V_{CC}. A pull-up resistor on the /RESET pin is approximately 500 K-ohms, typical.

Program execution starts 10 XTAL clock cycles after /RESET has returned High. The initial instruction fetch is from location 0020H. Figure 7 shows reset timing.

After a reset, the first routine executed must be one that initializes the TCTLHI control register to the required system configuration, followed by initialization of the remaining control registers.

Table 5. Control and Peripheral Register Reset Values

Register (HEX)	Register Name	Bits 7	6	5	4	3	2	1	0	Comments
FF	Stack Pointer	0	0	U	U	U	U	U	U	Stack pointer is not affected by RESET
FE	Reserved									
FD	Register Pointer	U	U	U	U	0	0	0	0	Register pointer is not affected by RESET
FC	Flags	U	U	U	U	U	U	*	*	Only WDT & SMR flags are affected by RESET
FB	Interrupt Mask	0	0	0	0	0	0	0	0	All interrupts masked by RESET
FA	Interrupt Request	0	0	0	0	0	0	0	0	All interrupt requests cleared by RESET
F9-F0	Reserved									
EF-E0	Virtual Copy									Virtual Copy of the Current Working Register Set
DF-D8	Reserved									
D7	PortB Spec. Func.	0	0	0	0	0	0	0	0	Deactivates all port special functions after RESET
D6	PortB Control	0	0	0	0	0	0	0	0	Defines all bits as inputs in PortB after RESET
D5	PortB Output	U	U	U	U	U	U	U	U	Output register not affected by RESET
D4	PortB Input	U	U	U	U	U	U	U	U	Current sample of the input pin following RESET
D3	PortA Spec. Func.	0	0	0	0	0	0	0	0	Deactivates all port special functions after RESET
D2	PortA Control	0	0	0	0	0	0	0	0	Defines all bits as inputs in PortA after RESET
D1	PortA Output	U	U	U	U	U	U	U	U	Output register not affected by RESET
D0	PortA Input	U	U	U	U	U	U	U	U	Current sample of the input pin following RESET
CF	Reserved									
CE	Reserved									
CD	T1VAL	U	U	U	U	U	U	U	U	
CC	T0VAL	U	U	U	U	U	U	U	U	
CB	T3VAL	U	U	U	U	U	U	U	U	
CA	T2VAL	U	U	U	U	U	U	U	U	
C9	T3AR	U	U	U	U	U	U	U	U	
C8	T2AR	U	U	U	U	U	U	U	U	
C7	T1ARHI	U	U	U	U	U	U	U	U	
C6	T0ARHI	U	U	U	U	U	U	U	U	
C5	T1ARLO	U	U	U	U	U	U	U	U	
C4	T0ARLO	U	U	U	U	U	U	U	U	
C3	WDTHI	1	1	1	1	1	1	1	1	
C2	WDTLO	1	1	1	1	1	1	1	1	
C1	TCTLHI	1	1	1	1	1	0	0	0	WDT Enabled in HALT Mode, WDT timeout at maximum value, STOP Mode disabled
C0	TCTLLO	0	0	0	0	0	0	0	0	All standard timers are disabled

* The SMR and WDT flags are set indicating the source of the RESET.

D1	D0	Reset Source
0	0	/RESET Pin
0	1	SMR Recovery
1	0	WDT Reset
1	1	Reserved

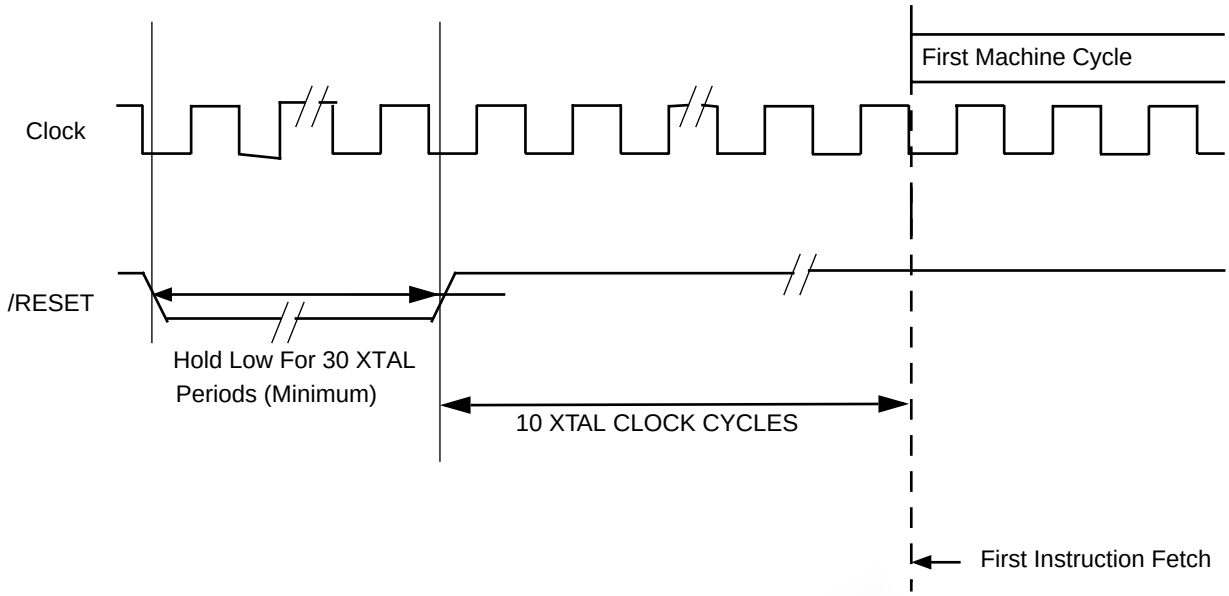


Figure 9. Reset Timing

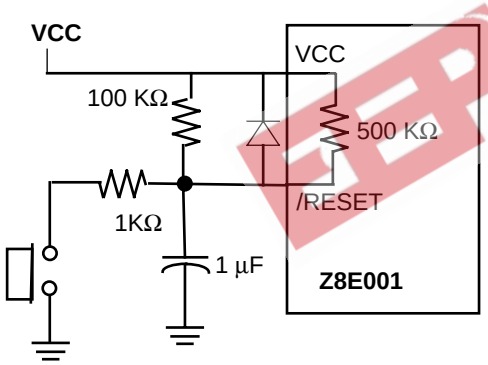


Figure 10. Example of External Power-On Reset Circuit

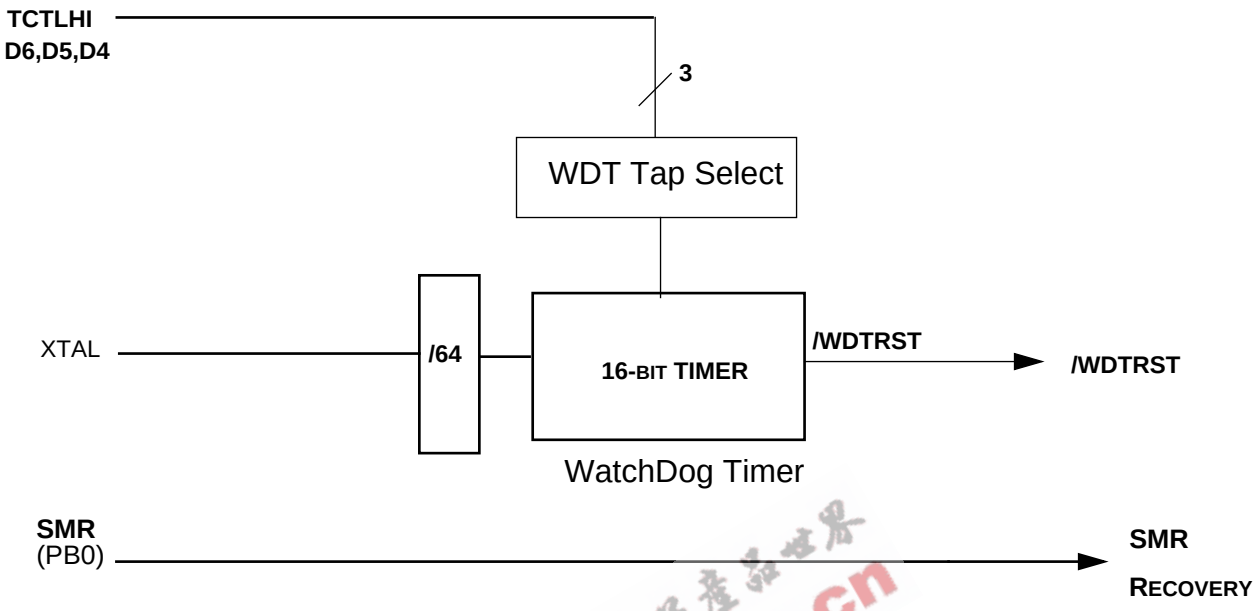


Figure 11. Z8E001 Reset Circuitry with WDT and SMR

Z8E001 WATCH-DOG TIMER (WDT)

The WDT is a retriggerable one-shot 16-bit timer that resets the Z8E001 if it reaches its terminal count. The WDT is driven by the XTAL2 clock pin. In order to provide the longer timeout periods desired in applications, the watchdog timer is only updated every 64th clock cycle. When operating in the RUN or HALT Modes, a WDT timeout reset is functionally equivalent to an interrupt vectoring the PC to 0020H and setting the WDT flag to a one state. Coming out of RESET, the WDT will be fully enabled with its timeout value set at the maximum value, unless otherwise programmed during the first instruction. Subsequent executions of the WDT instruction reinitialize the watchdog timer registers, C2H and C3H, to their initial values as defined by bits D6, D5, and D4 of the TCTLHI register. The WDT cannot be disabled except on the first cycle after RESET, and if the device enters Stop mode.

The WDT instruction should be executed often enough to provide some margin before allowing the WDT registers to get near 0. Because the WDT timeout periods are relatively long, a WDT reset **will** occur in the unlikely event that the WDT times out on exactly the same cycle that the WDT instruction is executed.

The WDT and SMR flags are the only flags that are affected by the external RESET pin. /RESET clears both the WDT and SMR flags. A WDT timeout sets the WDT flag. The STOP instruction sets the SMR flag. This behavior enables software to determine whether a pin RESET occurred, or whether a WDT timeout occurred, or whether a return from STOP Mode occurred. Reading the WDT flag does not reset it to zero, the user must clear it via software. Failure to clear the flag may result in undefined behavior.

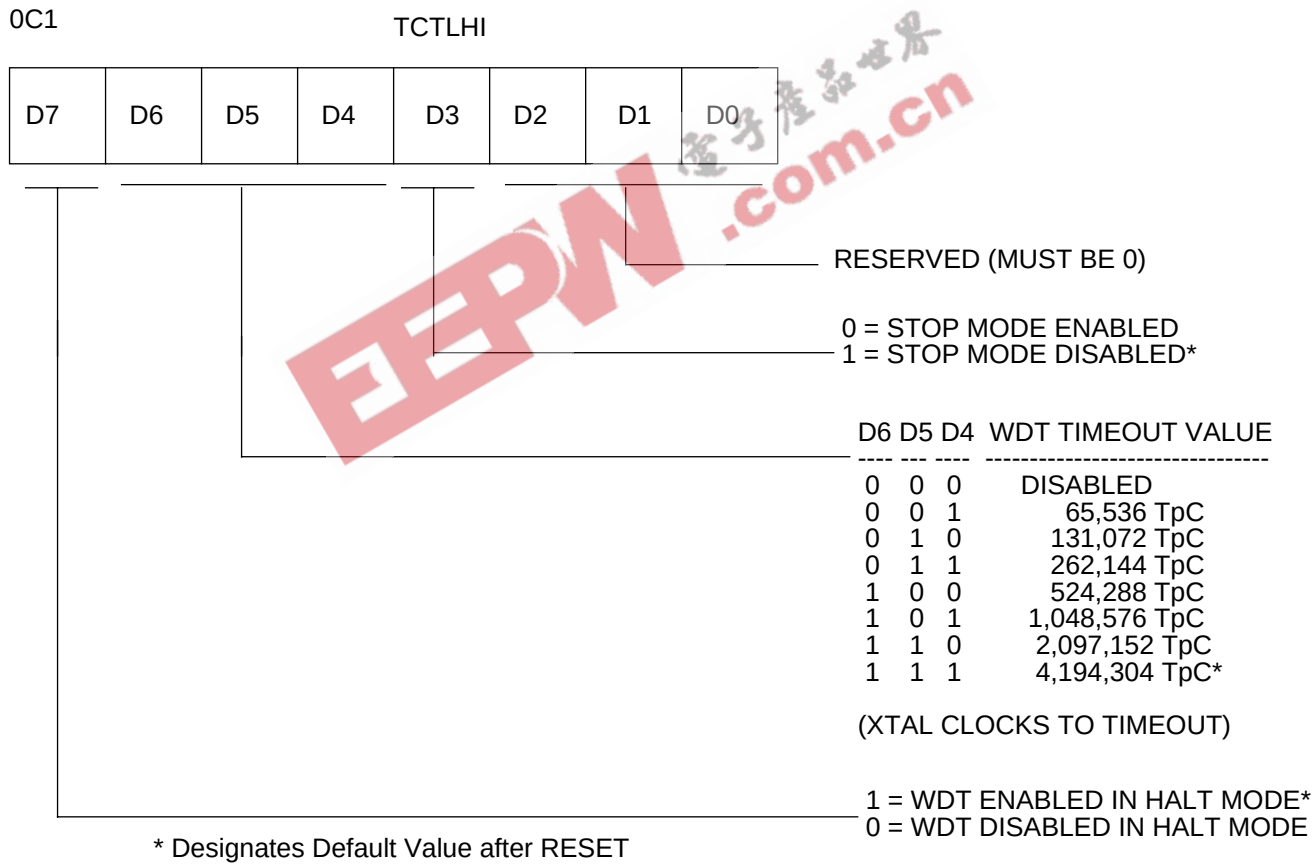


Figure 12. Z8E001 TCTLHI Register for Control of WDT

Note: The WDT can only be disabled via software if the first instruction out of RESET performs this function. Logic within the Z8E001 will detect that it is in the process of executing the first instruction after the part leaves RESET. During the execution of this instruction, the upper five bits of the TCTLHI register can be written. After this first instruction, hardware will not allow the upper five bits of this register to be written.

The TCTLHI bits for control of the WDT are described below:

WDT Time Select (D6, D5, D4). Bits 6, 5, and 4 determine the time-out period. Figure 11 shows the range of timeout values that can be obtained. The default values of D6, D5, and D4 are all 1, thus setting the WDT to its maximum timeout period when coming out of RESET.

Figure 13. Time-Out Period of the WDT

D6	D5	D4	Crystal Clocks to Timeout	Time-Out Using a 10 MHZ Crystal
0	0	0	Disabled	Disabled
0	0	1	65,536 TpC	6.55 ms
0	1	0	131,072 TpC	13.11 ms
0	1	1	262,144 TpC	26.21 ms
1	0	0	524,288 TpC	52.43 ms
1	0	1	1,048,576 TpC	104.86 ms
1	1	0	2,097,152 TpC	209.72 ms
1	1	1	4,194,304 TpC	419.43 ms

Notes:
TpC = XTAL clock cycle
The default on reset is D6 = D5 = D4 = 1.

WDT During HALT (D7). This bit determines whether or not the WDT is active during HALT Mode. A 1 indicates active during HALT. A 0 prevents the WDT from resetting the part while halted.Coming out of reset, the WDT will be enabled during HALT Mode.

STOP MODE (D3). Coming out of RESET, the Z8E001 will have STOP Mode disabled. If an application desires to use STOP Mode, bit D3 must be cleared immediately upon leaving RESET. If bit D3 is set, the STOP instruction will execute as a NOP. If bit D3 is cleared, the STOP instruction will enter Stop Mode. Whenever the Z8E001 wakes up after having been in STOP Mode, the STOP Mode will, once again, be disabled.

Bits 2, 1 and 0. These bits are reserved and must be 0.

POWER-DOWN MODES

In addition to the standard RUN mode, the Z8E001 MCU supports two Power-Down modes to minimize device current consumption. The two modes supported are HALT and STOP.

HALT MODE OPERATION

The HALT Mode suspends instruction execution and turns off the internal CPU clock. The on-chip oscillator circuit remains active so the internal clock continues to run and is applied to the timers and interrupt logic.

To enter the HALT Mode, the Z8E001 only needs to execute a HALT instruction. It is NOT necessary to execute a NOP instruction immediately before the HALT instruction.

```
7F      HALT      ;enter HALT Mode
```

The HALT Mode may be exited by servicing an interrupt, either externally or internally generated. Upon completion of the interrupt service routine, the user program continues from the instruction after the HALT instruction.

The HALT Mode may also be exited via a /RESET activation or a Watch-Dog Timer (WDT) timeout. In these cases, program execution will restart at the reset restart address 0020H.

STOP MODE OPERATION

The STOP Mode provides the lowest possible device standby current. This instruction turns off the on-chip oscillator and internal system clock.

To enter the STOP Mode, the Z8E001 only needs to execute a STOP instruction. It is NOT necessary to execute a NOP instruction immediately before the STOP instruction.,

```
6F      STOP      ;enter STOP Mode
```

The STOP Mode is exited by any one of the following resets: /RESET pin or a STOP-Mode Recovery source. Upon reset generation, the processor will always restart the application program at address 0020H and the STOP Mode Flag will be set. Reading this flag does not clear it, the user must clear this flag with software. Failure to clear this flag may result in undefined behavior.

The Z8E001 provides a dedicated STOP-Mode Recovery (SMR) circuit. In this case, a low level applied to input pin PB0 will trigger a SMR. To use this mode, pin PB0 (I/O Port B, bit 0) must be configured as an input before the STOP Mode is entered. The low level on PB0 must be held for a minimum pulse width T_{WSM}.

Note: Use of the PB0 input for the stop mode recovery does not initialize the control registers.

Note: The STOP Mode current (I_{CC2}) will be minimized when:

- V_{CC} is at the low end of the devices operating range.
- Output current sourcing is minimized.
- All inputs (digital and analog) are at the low or high rail voltages.

CLOCK

The Z8E001 MCU derives its timing from on-board clock circuitry connected to pins XTAL1 and XTAL2. The clock circuitry consists of an oscillator, a glitch filter, a divide-by-two shaping circuit, a divide-by-four shaping circuit, and a divide-by-eight shaping circuit. Figure 12 illustrates the clock circuitry. The oscillator's input is XTAL1 and its output is XTAL2. The clock can be driven by a crystal, a ceramic resonator, LC clock, or an external clock source.

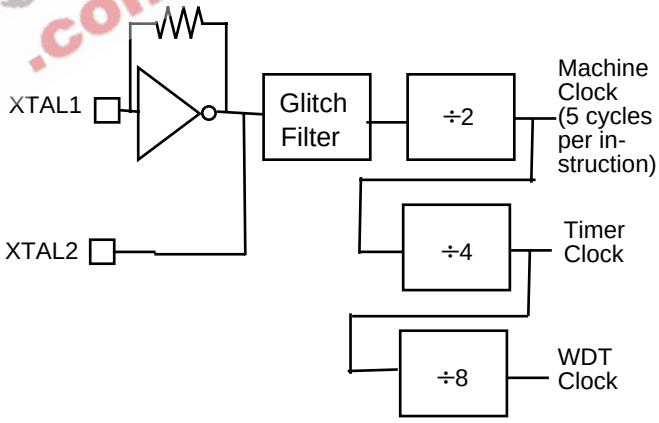


Figure 14. Z8E001 Clock Circuit

OSCILLATOR OPERATION

The Z8E001 MCU uses a Pierce oscillator with an internal feedback (Figure 13). The advantages of this circuit are low cost, large output signal, low-power level in the crystal, stability with respect to V_{CC} and temperature, and low impedances (not disturbed by stray effects).

One draw back is the need for high gain in the amplifier to compensate for feedback path losses. The oscillator amplifies its own noise at start-up until it settles at the frequency that satisfies the gain/phase requirements A x B = 1, where $A = V_0/V_i$ is the gain of the amplifier and $B = V_i/V_0$ is the gain of the feedback element. The total phase shift around the loop is forced to zero (360 degrees). Since VIN must be in phase with itself, the amplifier/inverter provides 180 degree phase shift and the feedback element is forced to provide the other 180 degrees of phase shift.

R1 is a resistive component placed from output to input of the amplifier. The purpose of this feedback is to bias the amplifier in its linear region and to provide the start-up transition.

Capacitor C_2 combined with the amplifier output resistance provides a small phase shift. It will also provide some attenuation of overtones.

Capacitor C_1 combined with the crystal resistance provides additional phase shift.

C_1 and C_2 can affect the start-up time if they increase dramatically in size. As C_1 and C_2 increase, the start-up time increases until the oscillator reaches a point where it does not start up any more.

It is recommended for fast and reliable oscillator start-up (over the manufacturing process range) that the load capacitors be sized as low as possible without resulting in overtone operation.

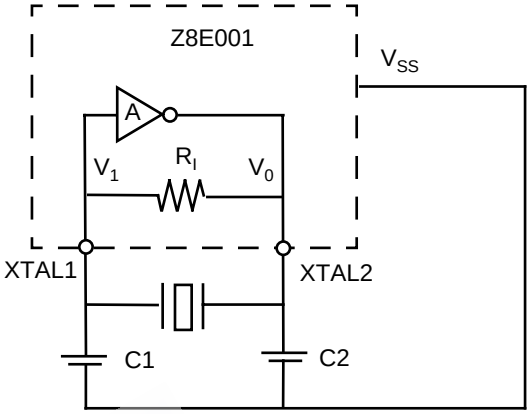


Figure 15. Pierce Oscillator with Internal Feedback Circuit

Layout

Traces connecting crystal, caps, and the Z8E001 oscillator pins should be as short and wide as possible. This reduces parasitic inductance and resistance. The components (caps, crystal, resistors) should be placed as close as possible to the oscillator pins of the Z8E001.

The traces from the oscillator pins of the IC and the ground side of the lead caps should be guarded from all other traces (clock, V_{CC}, address/data lines, system ground) to reduce cross talk and noise injection. This is usually accomplished by keeping other traces and system ground trace planes away from the oscillator circuit and by placing a Z8E001 device V_{SS} ground ring around the traces/components. The ground side of the oscillator lead caps should be connected to a single trace to the Z8E001 V_{SS} (GND) pin. It should not be shared with any other system ground trace or components except at the Z8E001 device V_{SS} pin. This is to prevent differential system ground noise injection into the oscillator (Figure 14).

Indications of an Unreliable Design

There are two major indicators that are used in working designs to determine their reliability over full lot and temperature variations. They are:

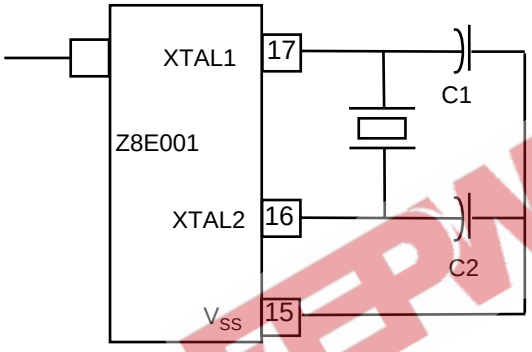
Start-up Time. If start -up time is excessive, or varies widely from unit to unit, there is probably a gain problem. C1/C2 needs to be reduced; the amplifier gain is not adequate at frequency, or crystal Rs is too large.

Output Level. The signal at the amplifier output should swing from ground to V_{CC}. This indicates there is adequate gain in the amplifier. As the oscillator starts up, the signal amplitude grows until clipping occurs, at which point the loop gain is effectively reduced to unity and constant oscillation is achieved. A signal of less than 2.5 volts peak-to-peak is an indication that low gain may be a problem. Either C_1 or C_2 should be made smaller or a low-resistance crystal should be used.

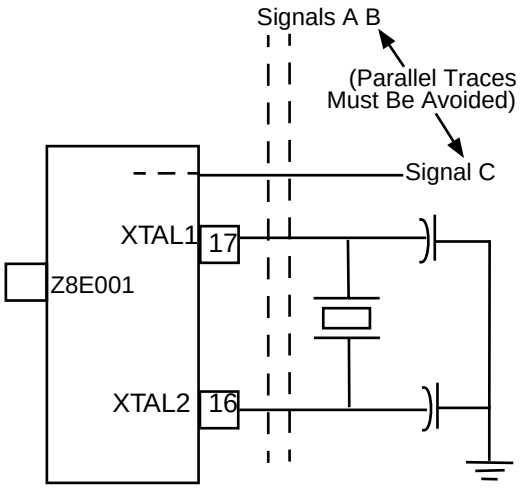
Circuit Board Design Rules

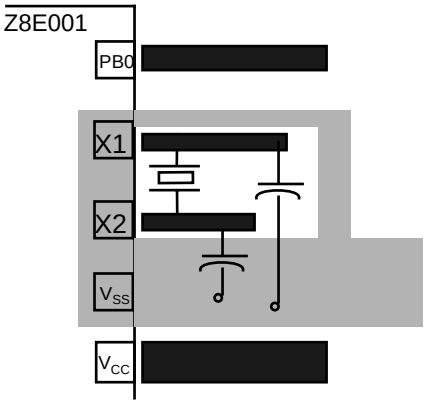
The following circuit board design rules are suggested:

- To prevent induced noise the crystal and load capacitors should be physically located as close to the Z8E001 as possible.
- Signal lines should not run parallel to the clock oscillator inputs. In particular, the crystal input circuitry and the internal system clock output should be separated as much as possible.
- V_{CC} power lines should be separated from the clock oscillator input circuitry.
- Resistivity between XTAL1 or XTAL2 and the other pins should be greater than 10 Mohms.



Clock Generator Circuit





Board Design Example
(Top View)

Figure 16. Circuit Board Design Rules

Crystals and Resonators

Crystals and ceramic resonators (Figure 15) should have the following characteristics to ensure proper oscillator operation:

Crystal Cut	AT (crystal only)
Mode	Parallel, Fundamental Mode
Crystal Capacitance	<7pF
Load Capacitance	10pF < CL < 220 pF, 15 typical
Resistance	100 ohms max

Depending on operation frequency, the oscillator may require the addition of capacitors C1 and C2 (shown in Figures 15 and16). The capacitance values are dependent on the manufacturer's crystal specifications.

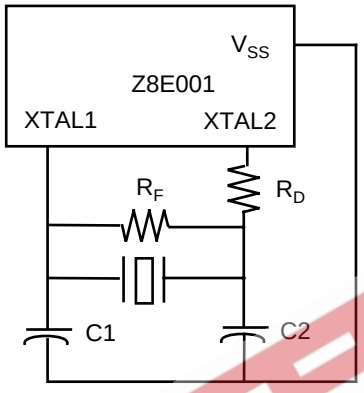


Figure 17. Crystal/Ceramic Resonator Oscillator

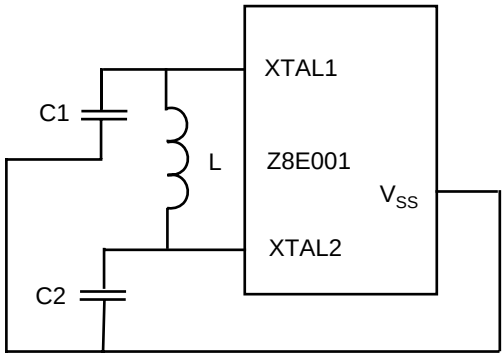


Figure 18. LC Clock

In most cases, the R_D is 0 Ohms and R_F is infinite. It is determined and specified by the crystal/ceramic resonator manufacturer. The R_D can be increased to decrease the amount of drive from the oscillator output to the crystal. It can also be used as an adjustment to avoid clipping of the oscillator signal to reduce noise. The R_F can be used to improve the start-up of the crystal/ceramic resonator. The Z8E001 oscillator already has an internal shunt resistor in parallel to the crystal/ceramic resonator.

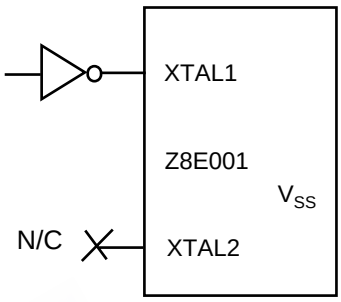


Figure 19. External Clock

It is recommended in Figures 14, 15, and 16 to connect the load capacitor ground trace directly to the V_{SS} (GND) pin of the Z8E001. This ensures that no system noise is injected into the Z8E001 clock. This trace should not be shared with any other components except at the V_{SS} pin of the Z8E001.

Please note that a parallel resonant crystal or resonator data sheet will specify a load capacitor value that is the series combination of C_1 and C_2, including all parasitics (PCB and holder).

LC OSCILLATOR

The Z8E001 oscillator can use a LC network to generate a XTAL clock (Figure 16).

The frequency stays stable over V_{CC} and temperature. The oscillation frequency is determined by the equation:

$$\text{Frequency} = \frac{1}{2\pi (LC_T)^{1/2}}$$

where L is the total inductance including parasitics and C_T is the total series capacitance including the parasitics.

Simple series capacitance is calculated using the following equation:

$$1/C_T = 1/C_1 + 1/C_2$$

$$\text{If } C_1 = C_2$$

$$1/C_T = 2\,C_1$$

$$C_1 = 2C_T$$

Sample calculation of capacitance C_1 and C_2 for 5.83 MHz frequency and inductance value of 27 uH:

$$5.83\ (10\text{^}6) = \frac{1}{2\pi\,[2.7\ (10^{-6})\ C_T]\ 1/2}$$

$$C_T = 27.6 \text{ pf}$$

Thus C_1 = 55.2 pf and C_2 = 55.2 pf.

TIMERS

For the Z8E001, 8-bit timers T0 and T1 are available to function as a pair of independent 8-bit standard timers, or they can be cascaded to function as a 16-bit PWM timer. In addition, 8-bit timers T2 and T3 are provided but they can only operate in cascade to function as a 16-bit standard timer.

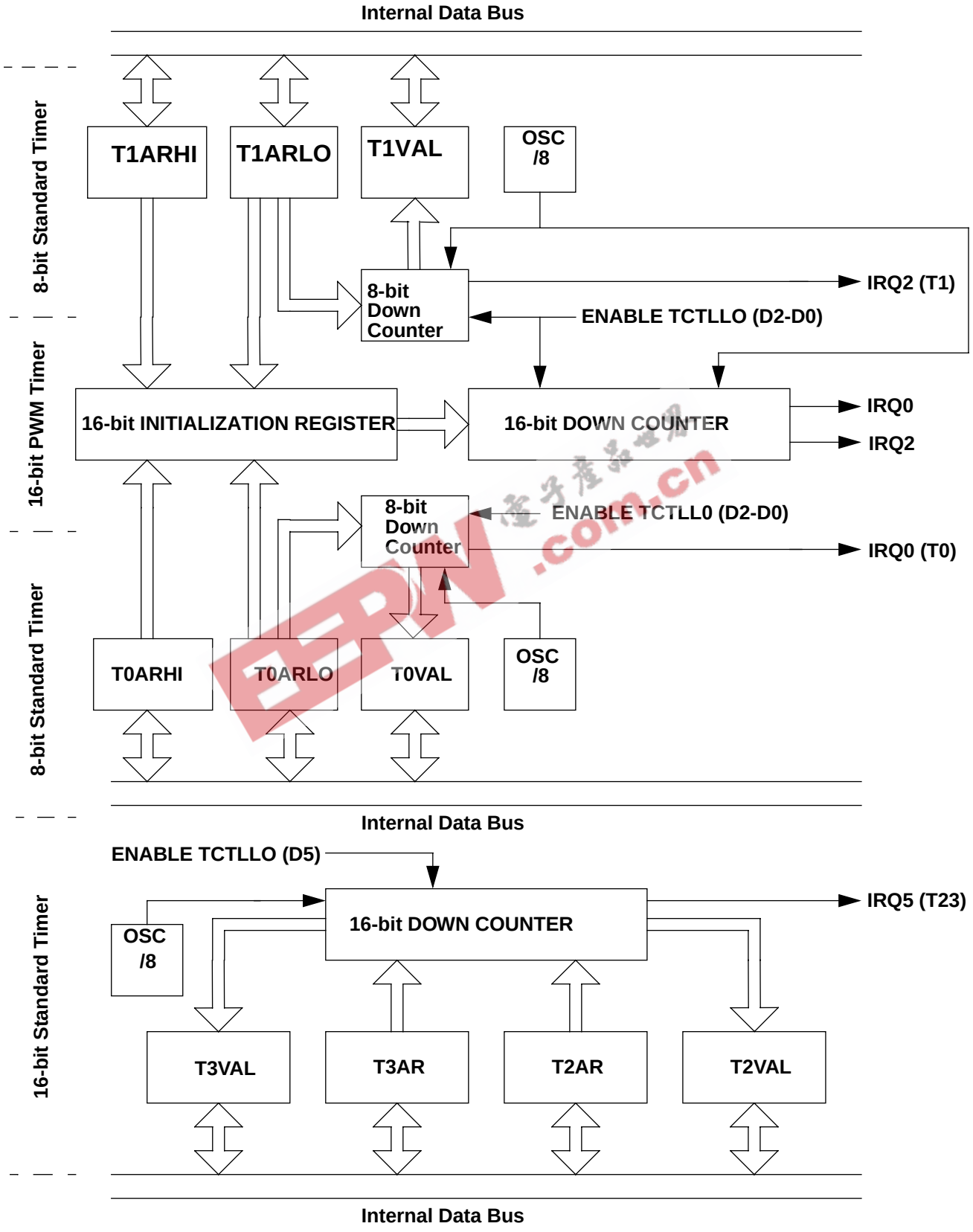
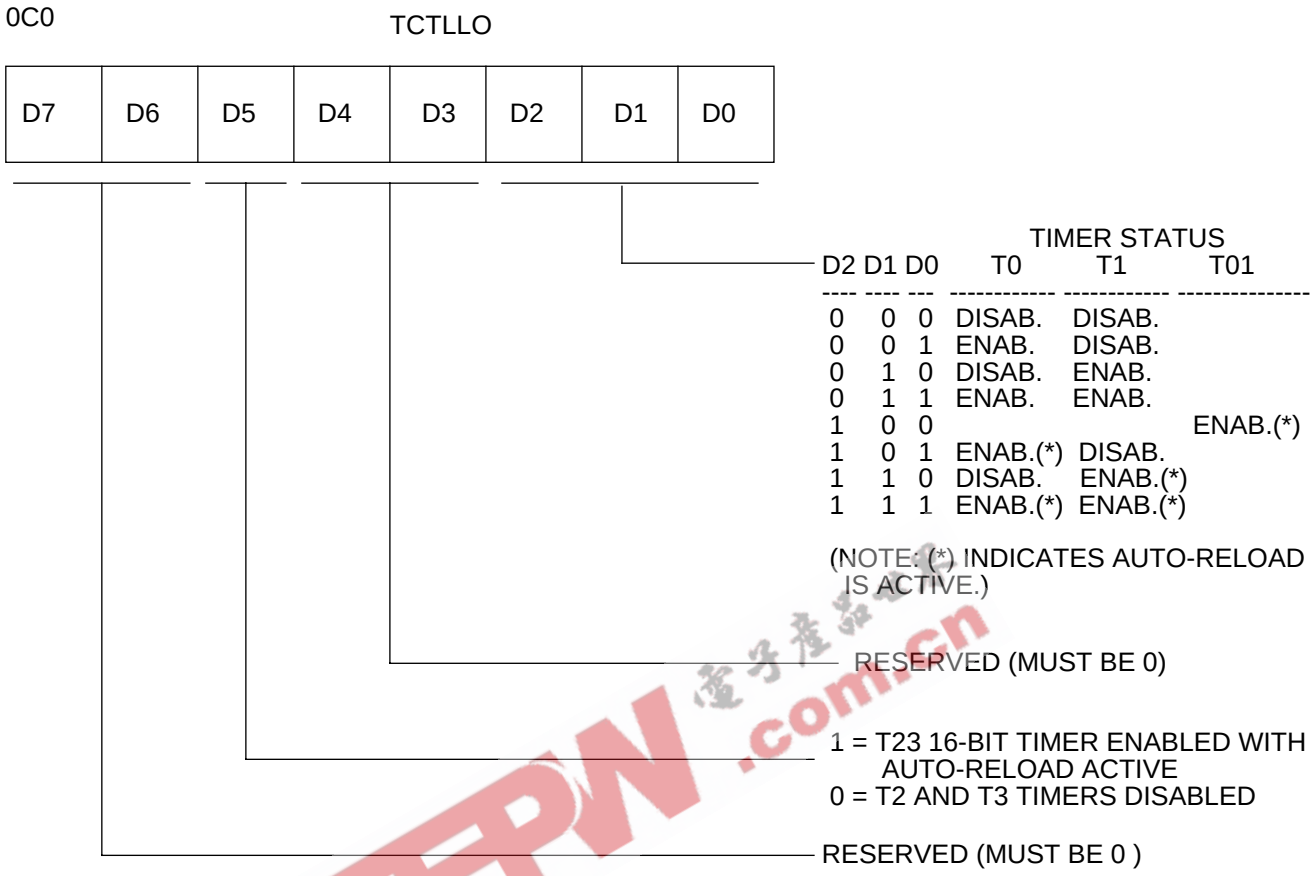


Figure 20. Timers Block Diagram



NOTE: TIMER T01 IS A 16-BIT PWM TIMER FORMED BY CASCADING 8-BIT TIMERS T1 (MSB) AND T0 (LSB). TIMER T23 IS A STANDARD 16-BIT TIMER FORMED BY CASCADING 8-BIT TIMERS T3(MSB) AND T2(LSB).

Figure 21. TCTLLO Register

Each 8-bit timer is given a pair of registers, which are both readable and writable. One of the registers is defined to contain the auto-initialization value for the timer, while the second register contains the current value for the timer. When a timer is enabled, the timer will decrement whatever value is currently held in its count register, and will then continue decrementing until it reaches 0, at which time an interrupt will be generated and the contents of the auto-initialization register are optionally copied into the count value register. If auto-initialization is not enabled, the timer will stop counting upon reaching 0 and control logic will clear the appropriate control register bit to disable the timer.This is referred to as "single-shot" operation. If auto-initialization is enabled, the timer will continue counting from the initialization value. Software should not attempt to use registers that are defined as having timer functionality.

Software is allowed to write to any register at any time, but care should be taken if timer registers be updated while the timer is enabled. If software updates the count value while the timer is in operation, the timer will continue counting based upon the software-updated value. This can produce strange behavior if the software update occurred at exactly the point that the timer was reaching 0 to trigger an interrupt and/or reload.

Similarly, if software updates the initialization value register while the timer is active, the next time that the timer reaches 0, it will be initialized using the updated value. Again, strange behavior could result if the initialization value register is being written while the timer is in the process of being initialized. Whether initialization is done with the new or old value is a function of the exact timing of the write operation. In all cases, the Z8E001 will prioritize the software write above that of a decrementer writeback. However, when hardware clears a control register bit for a timer that is configured for single-shot operation; the clearing of the control bit will override a software write. Reading either register can be done at any time, and will have no effect on the functionality of the timer.

If a timer pair is defined to operate as a single 16-bit entity, the entire 16-bit value must reach 0 before an interrupt is generated. In this case, a single interrupt will be generated, and the interrupt will correspond to the even 8-bit timer. For example, timers T2 and T3 are cascaded to form a single 16-bit timer, so the interrupt for the combined timer will be defined to be that of timer T2 rather than T3. When a timer pair is specified to act as a single 16-bit timer, the even timer registers in the pair (timer T0 or T2) will be defined to hold the timer's least significant byte; while the odd timer in the pair will hold the timer's most significant byte.

In parallel with the posting of the interrupt request, the interrupting timer's count value will be initialized by copying the contents of the auto-initialization value register to the count value register. It should be noted that any time that a timer pair is defined to act as a single 16-bit timer, that the auto-reload function will be performed automatically. All 16-bit timers will continue counting while their interrupt requests are active, and will operate in a free-running manner.

If interrupts are disabled for a long period of time, it is possible for the timer to decrement to 0 again before its initial interrupt has been responded to. This is a degenerate case, and hardware is not required to detect this condition.

When the timer control register is written, all timers that are enabled by the write will begin counting using the value that is held in their count register. An auto-initialization is not performed. All timers can receive an internal clock source only. Each timer that is enabled will be updated every 8th XTAL clock cycle.

If T0 and T1 are defined to work independently, then each will work as an 8-bit timer with a single auto-initialization register; T0ARLO for T0, and T1ARLO for T1. Each timer will assert its predefined interrupt when it times out, and will optionally perform the auto-initialization function. If T0 and T1 are cascaded to form a single 16-bit timer, then the single 16-bit timer will be capable of performing as a Pulse-Width Modulator (PWM). This timer is referred to as T01 to distinguish it as having special functionality that is not available when T0 and T1 act independently.

When T01 is enabled, it can use a pair of 16-bit auto-initialization registers. In this mode, one 16-bit auto-initialization value is composed of the concatenation of T1ARLO and T0ARLO, and the second auto-initialization value is composed of the concatenation of T1ARHI and T0ARHI. When T01 times out, it will alternately initialize its count value using the LO auto-init pair followed by the HI auto-init pair. This functionality corresponds to a PWM where the T1 interrupt will define the end of the HI section of the waveform, and the T0 interrupt will mark the end of the LO portion of the PWM waveform.

To use the cascaded timers as a PWM, one must initialize the T0 and T1 count registers to work in conjunction with the port pin. The user should initialize the T0 and T1 count registers to the PWM_HI auto-init value to obtain the desired PWM behavior. The PWM is arbitrarily defined to use the LO autoreload registers first. This implies that it had just timed out after beginning in the HI portion of the PWM waveform. As such, the PWM is defined to assert the T1 interrupt after the first timeout interval.

After the auto-initialization has been completed, decrementing occurs for the number of counts defined by the PWM_LO registers. When decrementing again reaches 0, the T0 interrupt is asserted; and auto-init using the PWM_HI registers occurs. Decrementing occurs for the number of counts defined by the PWM_HI registers until reaching 0, at which time the the T1 interrupt is asserted, and the cycle begins again.

The internal timers can be used to trigger external events by toggling the PB1 output when generating an interrupt. This functionality can only be achieved in conjunction with the port unit defining the appropriate pin as an output signal with the timer output special function enabled. In this mode, the appropriate port output will be toggled when the timer count reaches 0, and will continue toggling each time that the timer times out.

T_{OUT} Mode

The PortB special function register PTBSFR (0D7H) (Figure 20), is used in conjunction with the Port B directional control register PTBDIR (0D6) (Figure 21) to configure PB1 for T_{OUT} operation for timer0. In order for T_{OUT} to function, PB1 must be defined as an output line by setting PTBCTL bit 1 to 1. Configured in this way, PB1 has the capability of being a clock output for timer0, toggling the PB1 output pin on each timer0 timeout.

At end-of-count, the interrupt request line IRQ0 , clocks a toggle flip-flop. The output of this flip-flop drives the T_{OUT} line, PB1. In all cases, when timer0 reaches its end-of-count, T_{OUT} toggles to its opposite state (Figure 22). If, for example, timer0 is in Continuous Counting Mode, Tout will have a 50 percent duty cycle output. This duty cycle can easily be controlled by varying the initial values after each end-of-count.

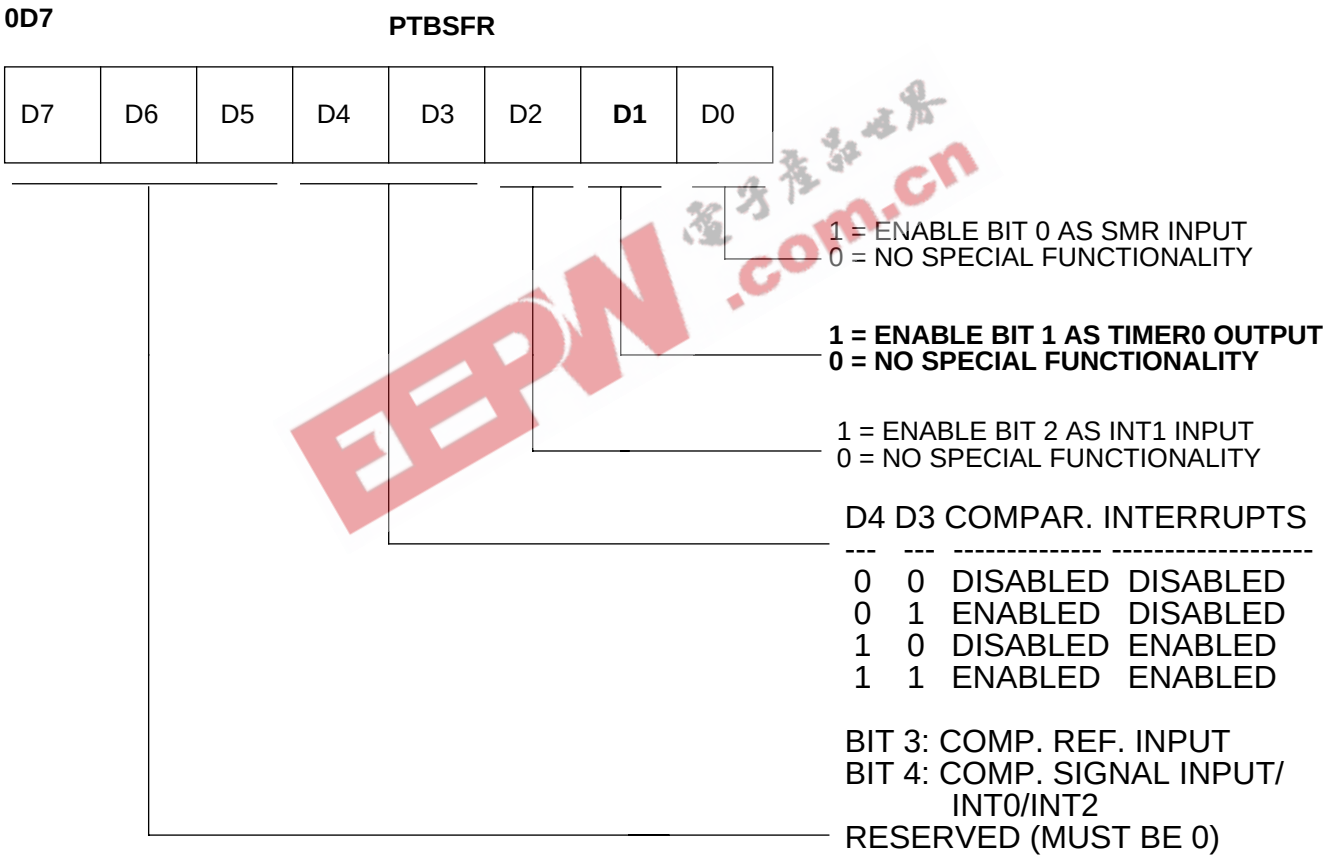


Figure 22. PortB Special Function Register (T_{out} Operation)

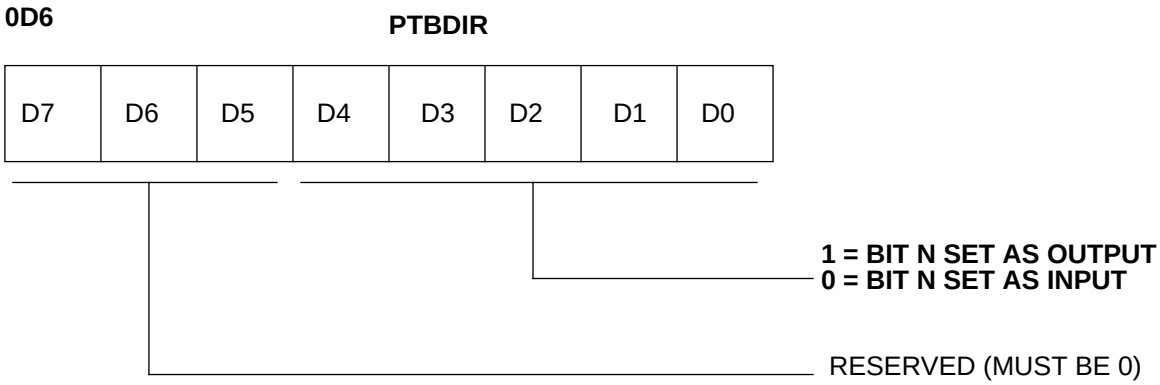


Figure 23. PortB Directional Control Register

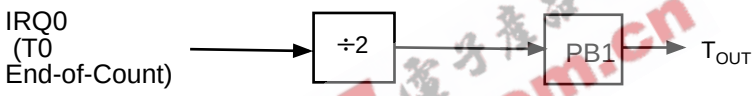


Figure 24. Timer T0 Output Through T_{OUT}

RESET CONDITIONS

After a hardware RESET, the timers are disabled. See Table 4 for timer control, value, and auto-initialization register status after RESET.

I/O PORTS

The Z8E001 has 13 lines dedicated to input and output. These lines are grouped into two ports known as Port A and Port B. Port A is an 8-bit port, bit programmable as either inputs or outputs. Port B can be programmed to provide standard input/output or the following special functions: timer0 output, comparator input, SMR input, and external interrupt inputs.

All ports have push-pull CMOS outputs. In addition, the outputs of Port A on a bit-wise basis may be configured for open-drain operation.The ports operate on a bit-wise basis. As such, the register values for/at a given bit position only affect the bit in question.

Each port is defined by a set of four control registers. See Figure 25, below.

Directional Control and Special Function Registers

Each port on the Z8E001 has an associated, dedicated Directional Control Register that determines on a bit-wise basis whether a given port bit will operate as an input or as an output.

Each port on the Z8E001 has a Special Function Register that in conjunction with the directional control register implements, on a bit-wise basis, any special functionality that may be defined for each particular port bit.

Input and Output Value Registers

Each port has an Output Value Register and an Input Value Register. For port bits configured as an input by means of the Directional Control Register, the Input Value Register for that bit position will contain the current synchronized input value.

For port bits configured as an output by means of the Directional Control Register, the value held in the corresponding bit of the Output Value Register is driven directly onto the output pin. The opposite register bit for a given pin (the output register bit for an input pin and the input register bit for an output pin) will hold their previous value. They will not be changed by hardware nor will they have any effect on the hardware.

REGISTER	ADDRESS	IDENTIFIER
Port B SPECIAL FUNCTION	0D7H	PTBSFR
Port B DIRECTION CONTROL	0D6H	PTBDIR
Port B OUTPUT VALUE	0D5H	PTBOUT
Port B INPUT VALUE	0D4H	PTBIN
Port A SPECIAL FUNCTION	0D3H	PTASFR
Port A DIRECTION CONTROL	0D2H	PTADIR
Port A OUTPUT VALUE	0D1H	PTAOUT
Port A INPUT VALUE	0D0H	PTAIN

Figure 25. Z8E001 I/O Ports Registers

READ/WRITE OPERATIONS

The control for each port is done on a bit-wise basis. All bits are capable of operating as inputs or outputs, depending upon the setting of the port's directional control register. If configured as an input, each bit is given a Schmitt-trigger. The output of the Schmitt-trigger is latched twice to perform a synchronization function, and the output of the synchronizer is fed to the port input register, which can be read by software.

A write to a port input register has the effect of updating the contents of the input register, but subsequent reads will not necessarily return the same value that was written. If the bit in question is defined as an input, the input register for that bit position will contain the current synchronized input value. Thus, writes to that bit position will be overwritten on the next clock cycle with the newly sampled input data. However, if the particular port bit is programmed as an output, the input register for that bit will retain the software-updated value since the port bits that are programmed as outputs do not sample the value being driven out.

Any bit in either port can be defined as an output by setting the appropriate bit in the directional control register. If this is the case, the value held in the appropriate bit of the port output register is driven directly onto the output pin. Note, however, that this does not necessarily reflect the actual output value. If an external error is holding an output pin either high or low against the output driver, the software read will return the DESIRED value, not the actual state caused by the contention. When a bit is defined as an output , the Schmitt-trigger on the input will be disabled to save power.

Updates to the output register will take effect based upon the timing of the internal instruction pipeline, but will be referenced to the rising edge of the clock. The output register can be read at any time, and will return the current output value that is held. No restrictions are placed on the timing of reads and/or writes to any of the port registers with respect to the others, but care should be taken when updating the directional control and special function registers.

When updating a directional control register, the special function register should first be disabled. If this precaution is not taken, spurious events could take place as a result of the change in port I/O status. This is especially important when defining changes in Port B, since the spurious event referred to above could be one or more interrupts. Clearing of the SFR register should be the first step in configuring the port, and setting the SFR register should be the last step in the port configuration process. To ensure deterministic behavior, the SFR register should not be written until the pins are being driven appropriately and all initialization has been completed.

PORT A

Port A is a general-purpose port. Figure 25 shows a block diagram of Port A. Each of its lines can be independently programmed as input or output via the Port A Directional Control Register (PTADIR at 0D2H) as seen in Figure 24. A bit set to a 1 in PTADIR configures the corresponding bit in Port A as an output, while a bit cleared to 0 configures the corresponding bit in Port A as an input.

The input buffers are Schmitt-triggered. Bits programmed as outputs may be individually programmed as either push-pull or open drain by setting the corresponding bit in the Special Function Register (PTASFR, Figure 29.)

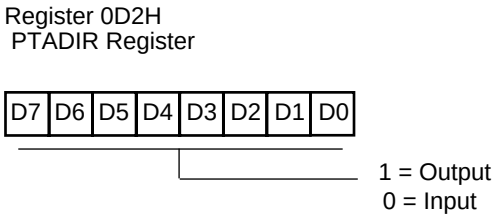


Figure 26. Port A Directional Control Register

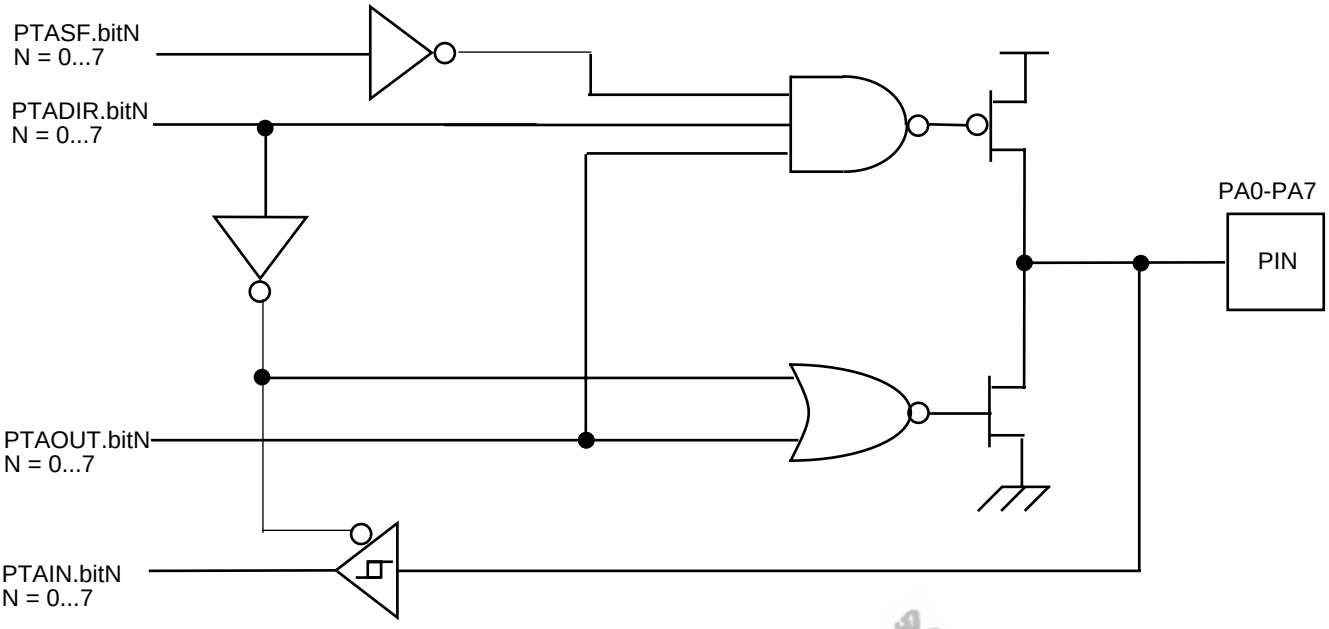


Figure 27. Port A Configuration with Open-Drain Capability and Schmitt-Trigger

Port A Register Diagrams

Port A Input Value Register

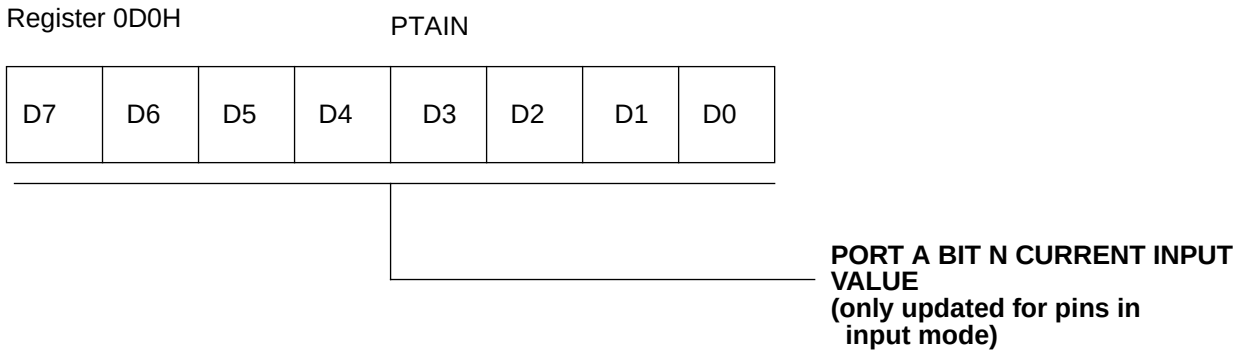


Figure 28. Port A Input Value Register

Port A Output Value Register

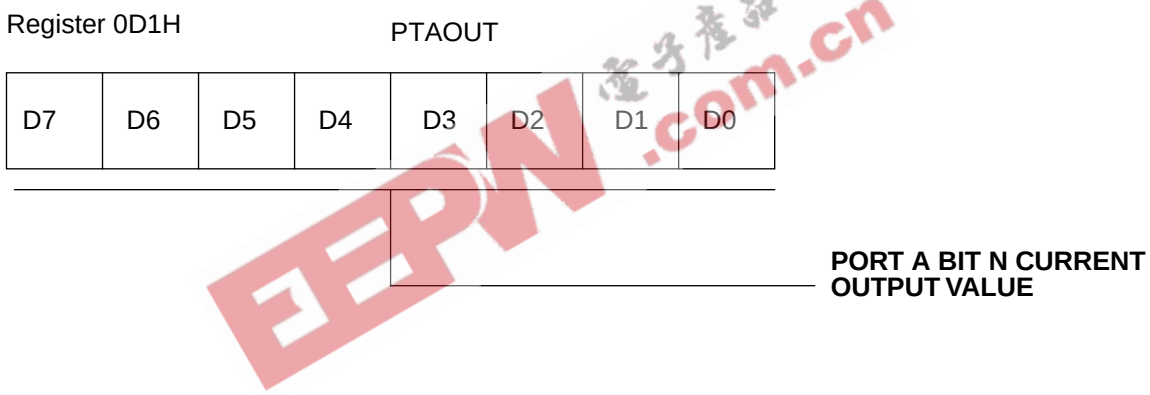


Figure 29. Port A Output Value Register

Port A Directional Control Register

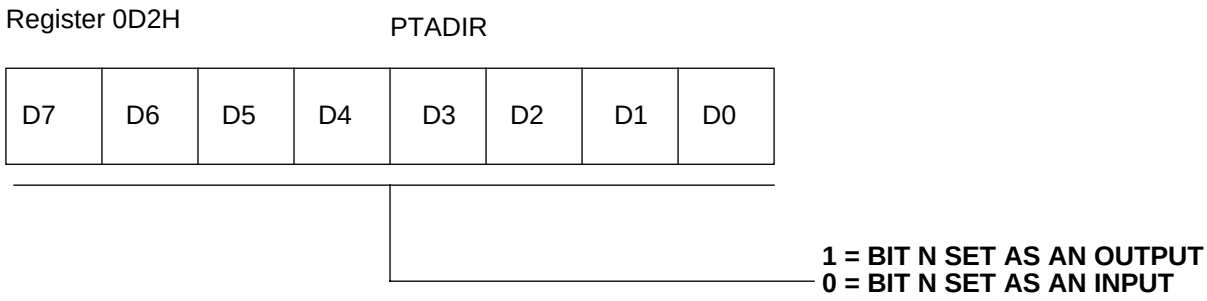


Figure 30. Port A Directional Control Register

Port A Special Function Register

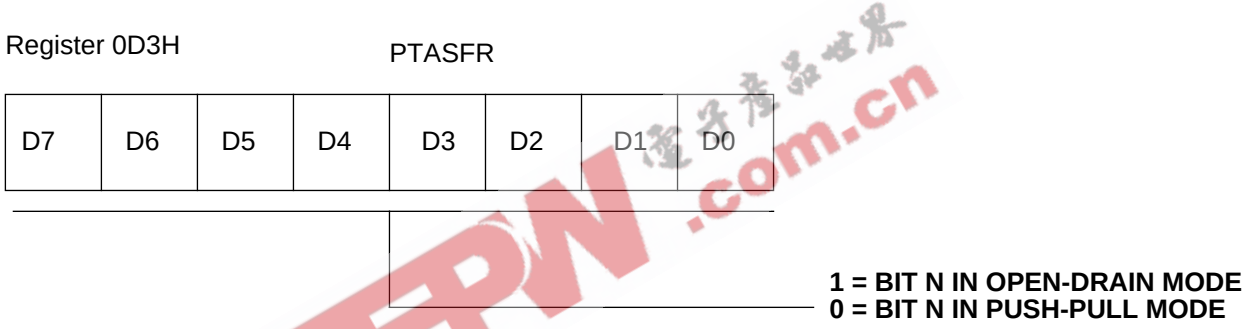


Figure 31. Port A Special Function Register

PORT B

Port B Description

Port B is a 5-bit, bidirectional, CMOS-compatible I/O port. These five I/O lines can be configured under software control to be an input or output, independently. Input buffers are Schmitt-triggered. See Figures 31 through 34 for diagrams of all five Port B pins.

In addition to standard input/output capability on all five pins of Port B, each pin provides special functionality as shown in the following table:

Table 6. Port B Special Functions

Port Pin	Input Special Function	Output Special Function
PB0	Stop Mode Recovery Input	None
PB1	None	Timer0 Output
PB2	Interrupt1	None
PB3	Comparator Reference Input	None
PB4	Comparator Signal Input/Interrupt0/ Interrupt2	None

Special functionality is invoked via the Port B Special Function Register. See Figure 30 for the arrangement and control conventions for this register.

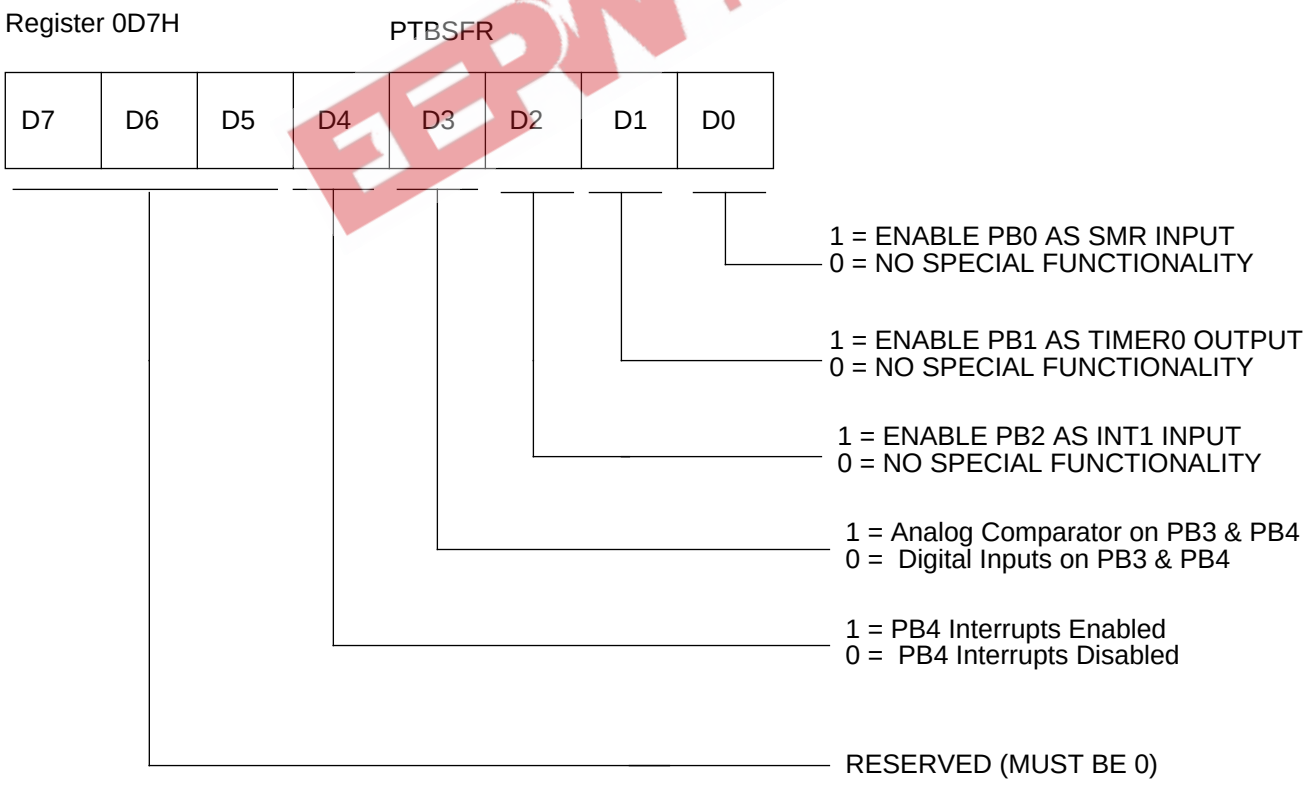


Figure 32. Port B Special Function Register

PORT B - PIN 0 CONFIGURATION

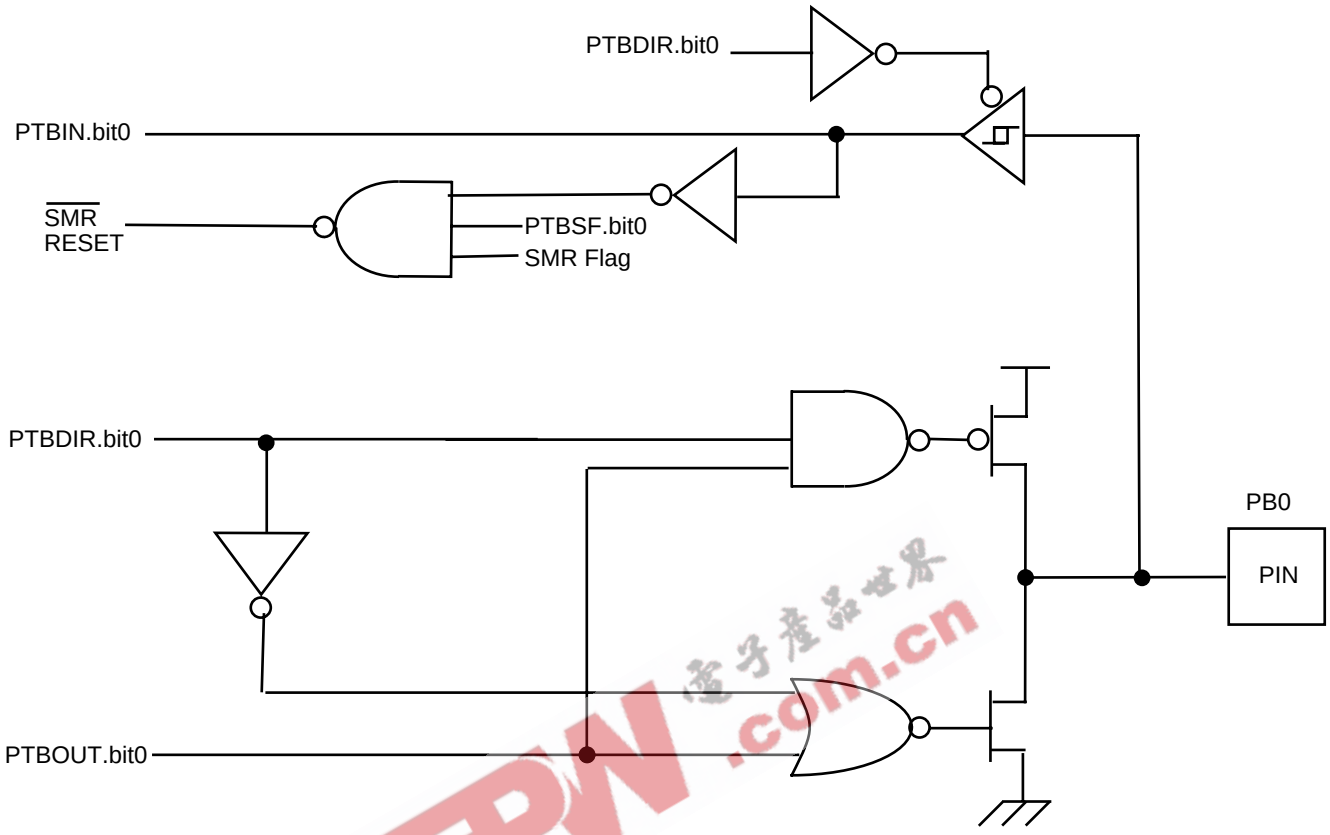


Figure 33. Port B Pin 0 Diagram

PORT B - PIN 1 CONFIGURATION

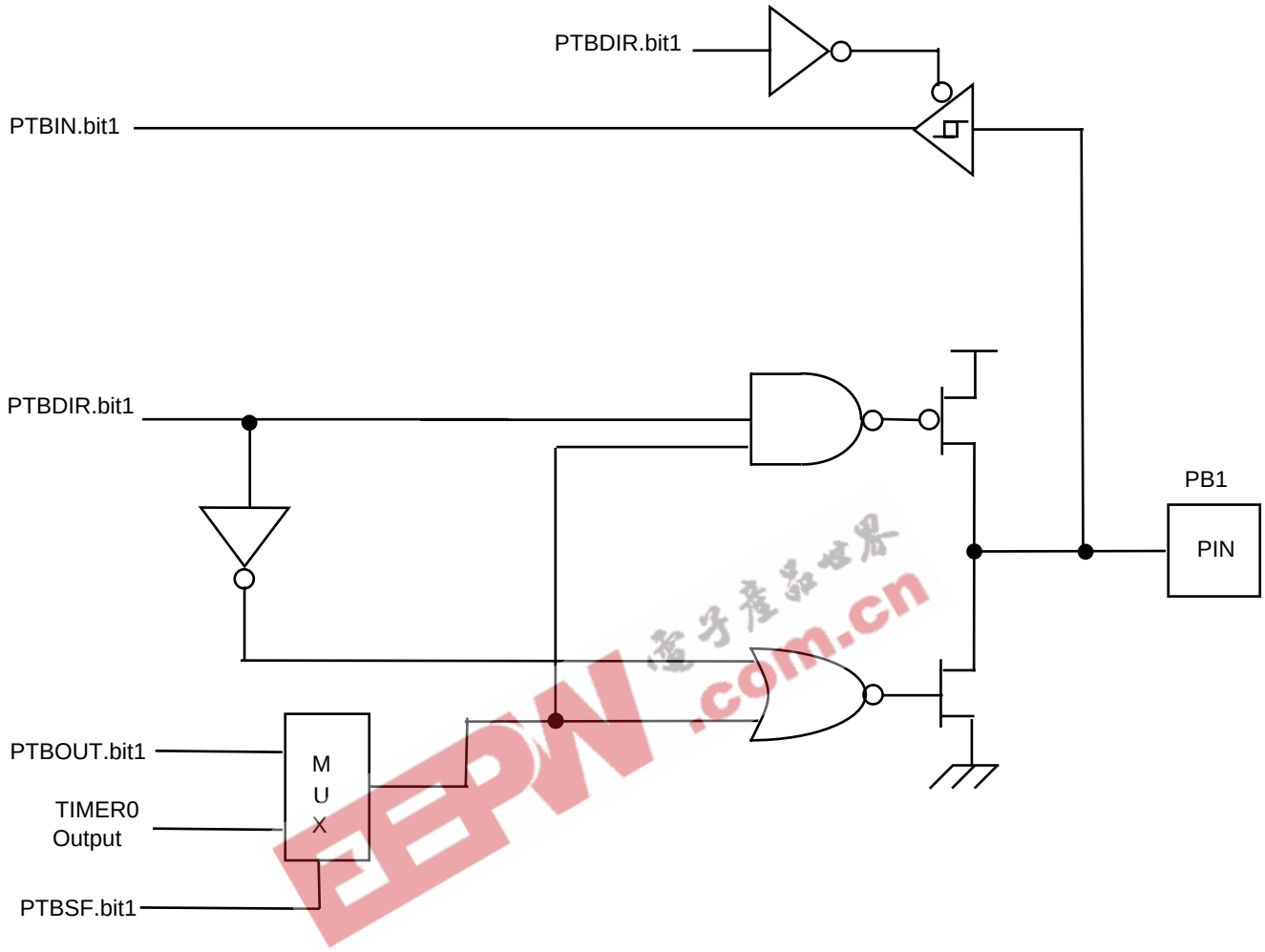


Figure 34. Port B Pin 1 Diagram

PORT B - PIN 2 CONFIGURATION

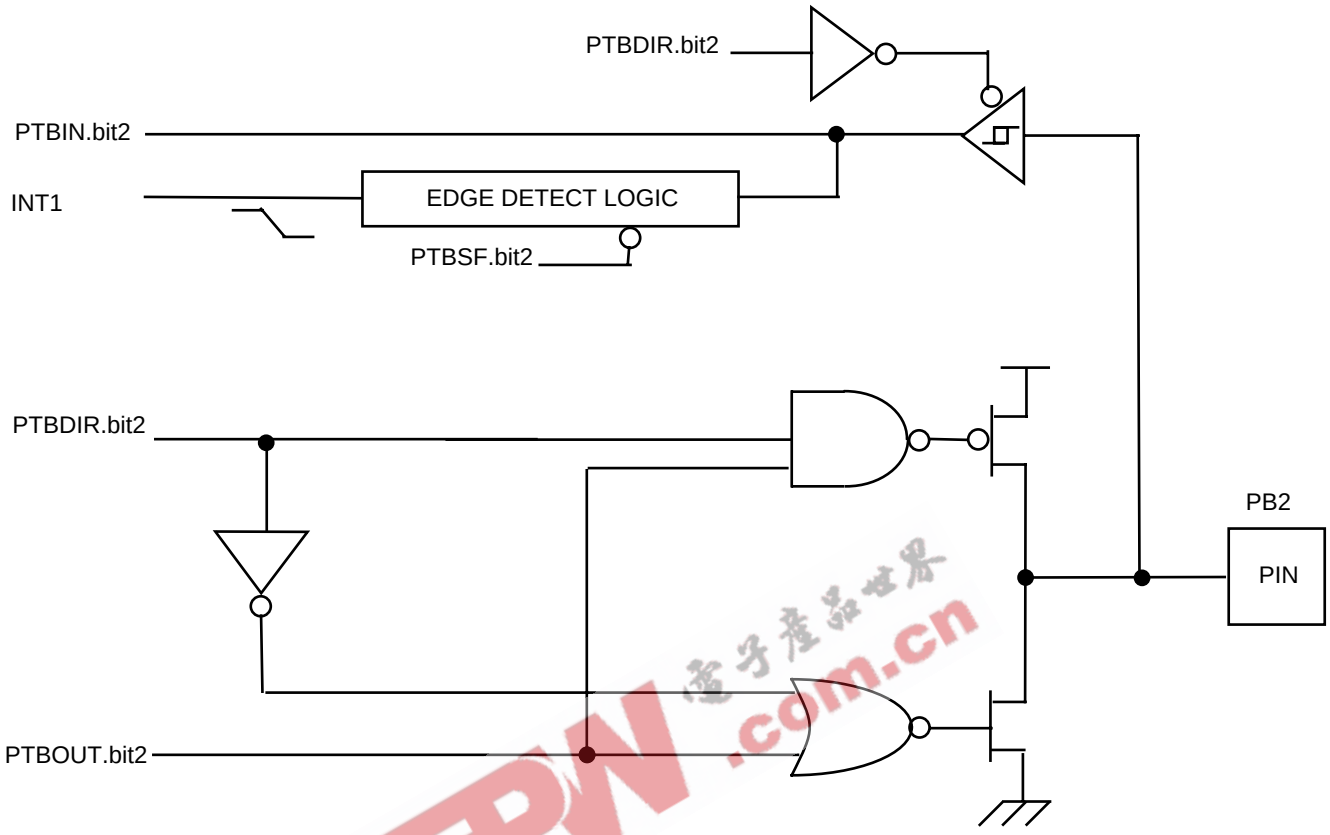


Figure 35. Port B Pin 2 Diagram

PORT B - PINS 3 AND 4 CONFIGURATION

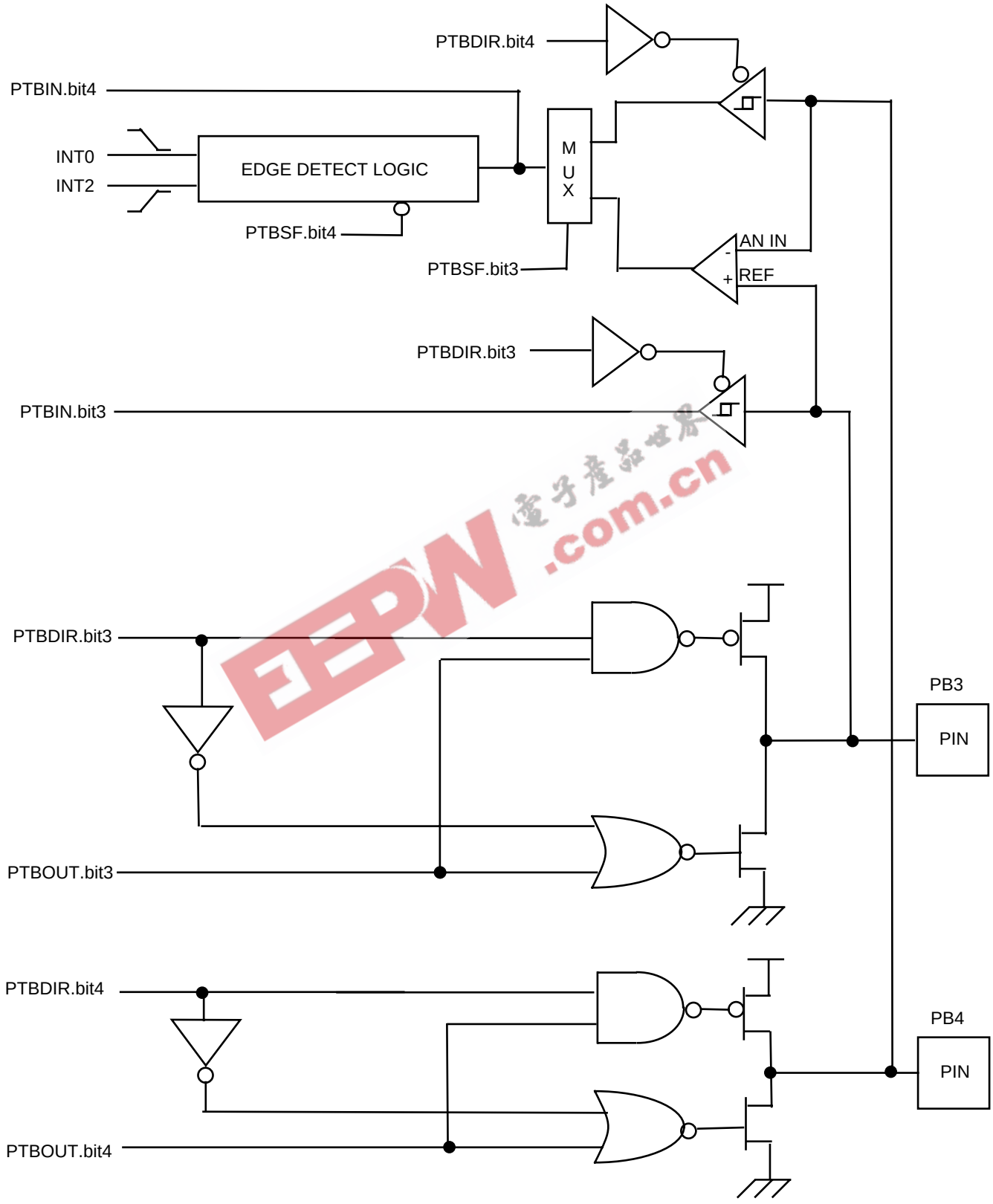


Figure 36. Port B Pins 3 and 4 Diagram

PORT B CONTROL REGISTERS

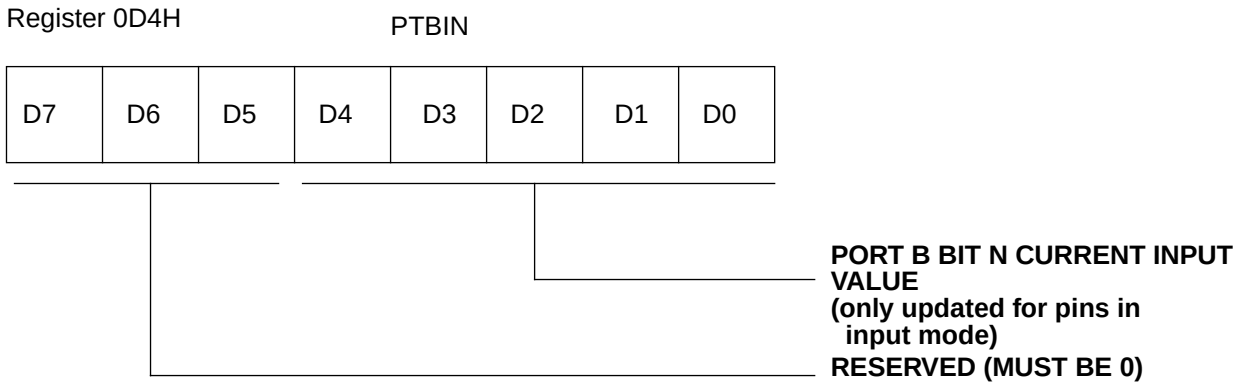


Figure 37. Port B Input Value Register

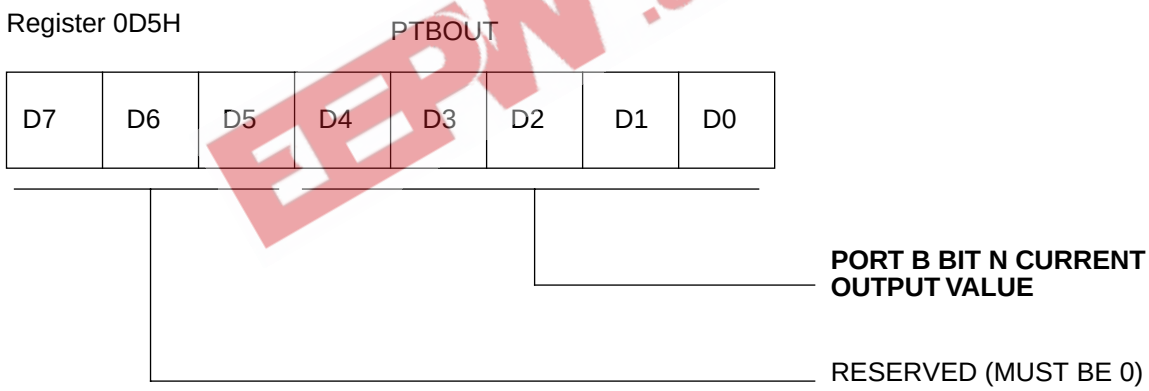


Figure 38. Port B Output Value Register

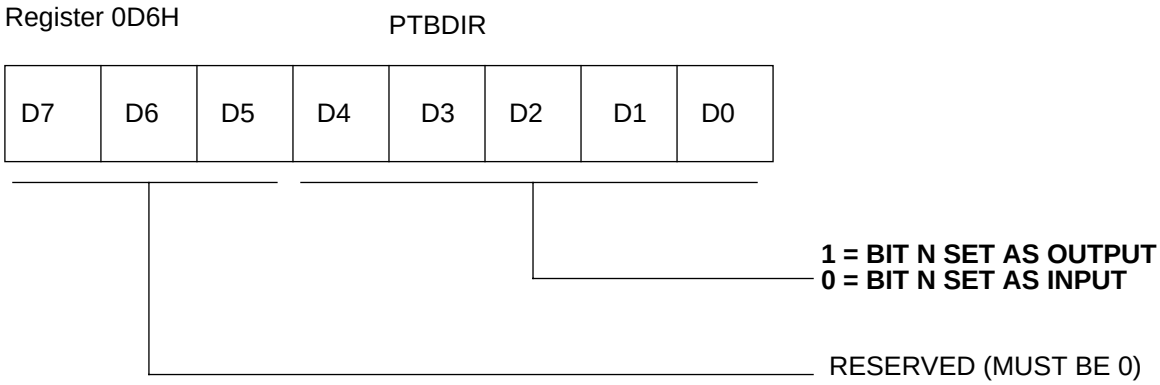


Figure 39. Port B Directional Control Register

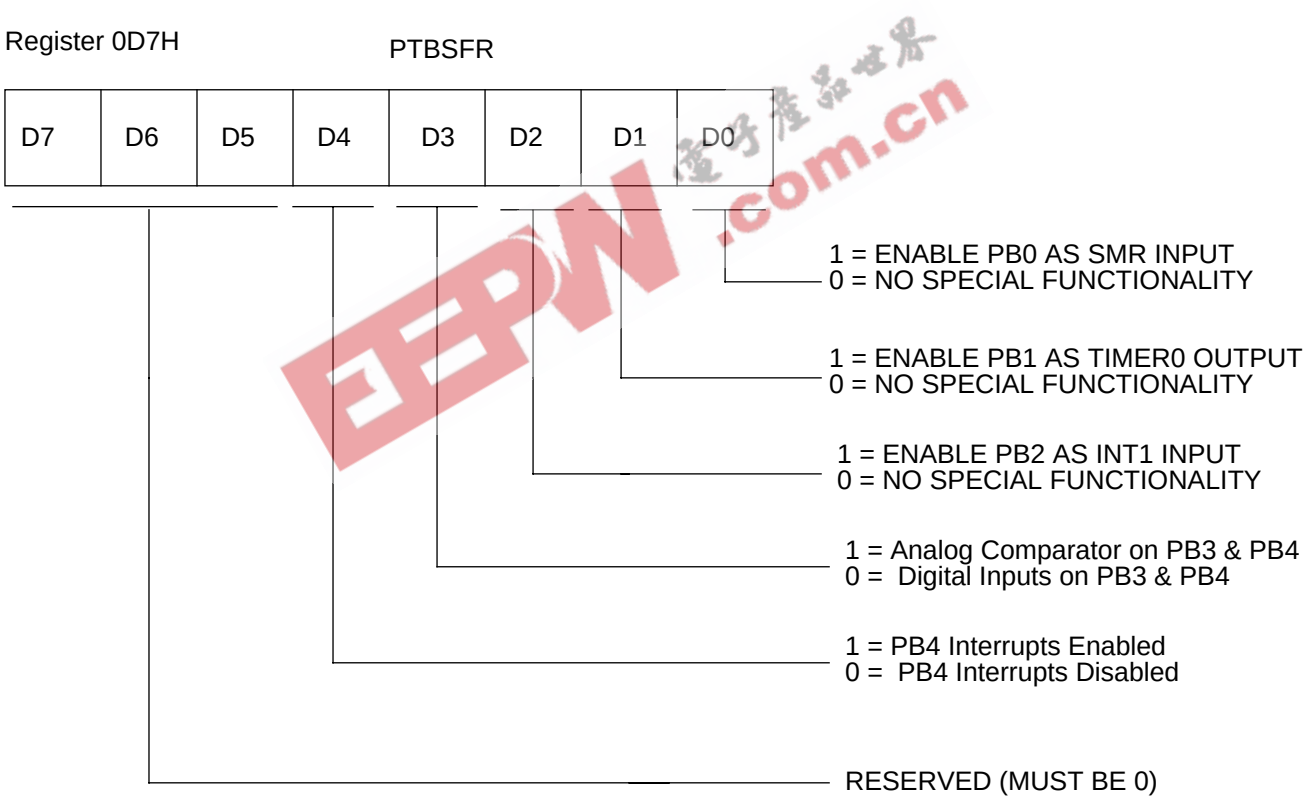


Figure 40. Port B Special Function Register

I/O PORT RESET CONDITIONS

Full Reset

Port A and Port B output value registers are not affected by RESET.

On RESET, the Port A and Port B directional control registers will be cleared to all zeros, which will define all pins in both ports as inputs.

On RESET, since the directional control registers have redefined all pins as inputs, the Port A and Port B input value registers will have the previously held data overwritten with the current sample of the input pins.

On RESET, the Port A and Port B special function registers will be cleared to all zeros, which will deactivate all port special functions.

Note: The SMR and WDT timeout events are NOT full device resets. None of the port control registers is effected by either of these events.

ANALOG COMPARATOR

The Z8E001 includes one on-chip analog comparator. Pin PB4 has a comparator front end. The comparator reference voltage is on pin PB3.

Comparator Description

The on-chip comparator can process an analog signal on PB4 with reference to the voltage on PB3. The analog function is enabled by programming the Port B Special Function Register bits 3 and 4.

When the analog comparator function is enabled, bit 4 of the input register will be defined as holding the synchronized output of the comparator, while bit 3 will retain a synchronized sample of the reference input.

If the interrupts for PB4 are enabled when the comparator special function is selected, the output of the comparator will generate interrupts.

COMPARATOR OPERATION

The comparator output reflects the relationship between the analog input to the reference input. If the voltage on the analog input is higher than the voltage on the reference input, then the comparator output will be at a high state. If the voltage on the analog input is lower than the voltage on the reference input, then the analog output will be at a Low state.

Comparator Definitions

V_{ICR}
The usable voltage range for the positive input and the reference input is called the common mode voltage range (V_{ICR}). The comparator is not guaranteed to work if the input is outside of the V_{ICR} range.

V_{offset}
The absolute value of the voltage between the positive input and the reference input required to make the comparator output voltage switch is the input offset voltage (V_{offset}).

I_{IO}
For the CMOS voltage comparator input, the input offset current (I_{IO}) is the leakage current of the CMOS input gate.

HALT Mode

The analog comparator is functional during HALT Mode. If the interrupts are enabled, an interrupt generated by the comparator will cause a return from HALT Mode.

STOP Mode

The analog comparator is disabled during STOP Mode. The comparator is powered down to prevent it from drawing any current.

INPUT PROTECTION

All I/O pins on the Z8E001 have diode input protection. There is a diode from the I/O pad to V_{CC} and to V_{SS}. See Figure 41.

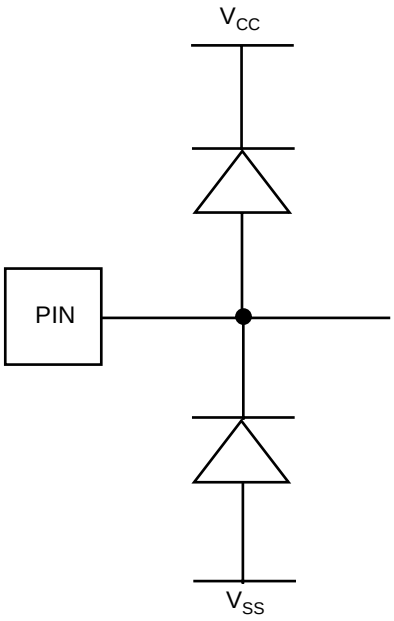


Figure 41. I/O Pin Diode Input Protection

However, on the Z8E001, the /RESET pin has only the input protection diode from pad to V_{SS}. See Figure 42.

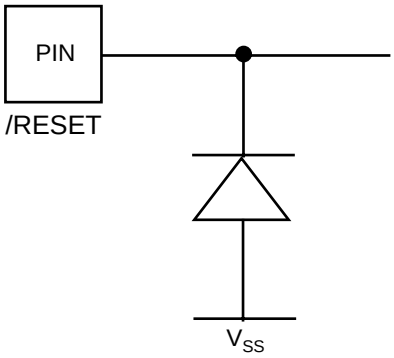
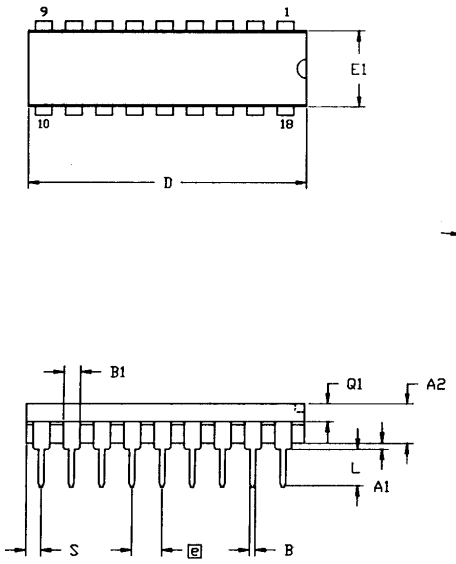


Figure 42. /RESET Pin Input Protection

The high-side input protection diode was removed on this pin to allow the application of high voltage during the OTP programming mode.

For better noise immunity in applications that are exposed to system EMI, a clamping diode to V_{CC} from this pin may be required to prevent entering the OTP programming mode or to prevent high voltage from damaging this pin.

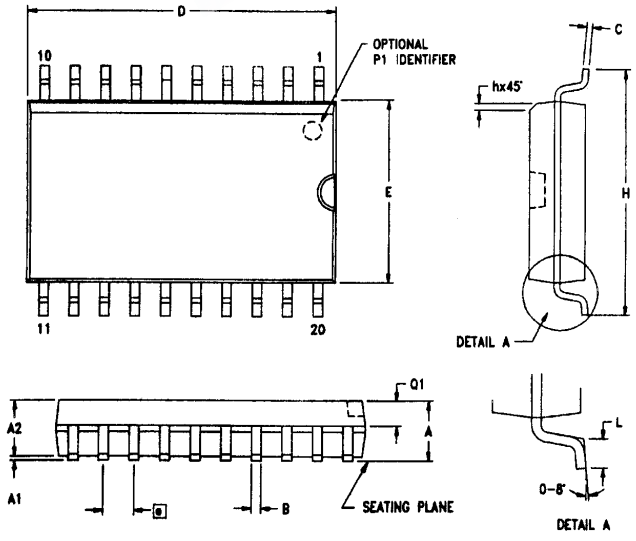
PACKAGE INFORMATION



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	0.81	.020	.032
A2	3.25	3.43	.128	.135
B	0.38	0.53	.015	.021
B1	1.14	1.65	.045	.065
C	0.23	0.38	.009	.015
D	22.35	23.37	.880	.920
E	7.62	8.13	.300	.320
E1	6.22	6.48	.245	.255
e	2.54 TYP		.100 TYP	
eA	7.87	8.89	.310	.350
L	3.18	3.81	.125	.150
Q1	1.52	1.65	.060	.065
S	0.89	1.65	.035	.065

CONTROLLING DIMENSIONS : INCH

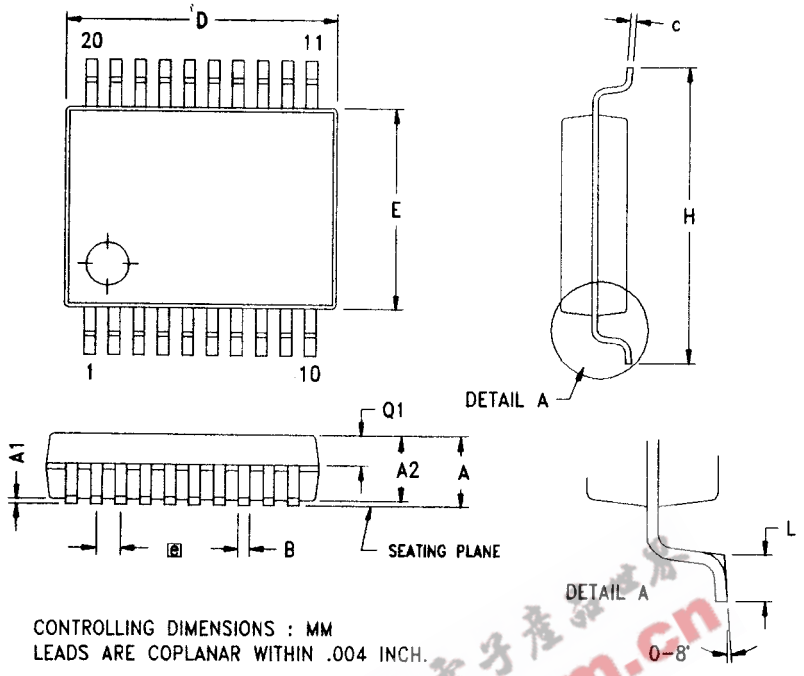
Figure 43. 18-Pin DIP Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.40	2.65	.094	.104
A1	0.10	0.30	.004	.012
A2	2.24	2.44	.088	.096
B	0.36	0.46	.014	.018
C	0.23	0.30	.009	.012
D	12.60	12.95	.496	.510
E	7.40	7.60	.291	.299
e	1.27 TYP		.050 TYP	
H	10.00	10.65	.394	.419
h	0.30	0.40	.012	.016
L	0.60	1.00	.024	.039
Q1	0.97	1.07	.038	.042

CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH.

Figure 44. 18-Pin SOIC Package Diagram



SYMBOL	MILLIMETER			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.73	1.85	1.98	0.068	0.073	0.078
A1	0.05	0.13	0.21	0.002	0.005	0.008
A2	1.68	1.73	1.83	0.066	0.068	0.072
B	0.25	0.30	0.38	0.010	0.012	0.015
C	0.13	0.15	0.22	0.005	0.006	0.009
D	7.07	7.20	7.33	0.278	0.283	0.289
E	5.20	5.30	5.38	0.205	0.209	0.212
e	0.65 TYP			0.0256 TYP		
H	7.65	7.80	7.90	0.301	0.307	0.311
L	0.56	0.75	0.94	0.022	0.030	0.037
Q1	0.74	0.78	0.82	0.029	0.031	0.032

Figure 45. 20-Pin SSOP Package Diagram

ORDERING INFORMATION

Standard Temperature

18-Pin DIP	18-Pin SOIC	20-Pin SSOP
Z8E00110PSC	Z8E00110SSC	Z8E00110HSC

Extended Temperature

18-Pin DIP	18-Pin SOIC	20-Pin SSOP
Z8E00110PEC	Z8E00110SEC	Z8E00110HEC

For fast results, contact your local Zilog sales office for assistance in ordering the part(s) desired.

CODES

Preferred Package

P = Plastic DIP

Longer Lead Time

S = SOIC
H = SSOP

Preferred Temperature

S = 0°C to +70°C
E = –40°C to +105°C

Speed

10 = 10 MHz

Environmental

C = Plastic Standard

Example:

Z 8E001 10 P S C is a Z86E001, 10 MHz, DIP, 0° to +70°C, Plastic Standard Flow

- C — Environmental Flow
- S — Temperature
- P — Package
- 10 — Speed
- 8E001 — Product Number
- Z — Zilog Prefix

Pre-Characterization Product:

The product represented by this CPS is newly introduced and Zilog has not completed the full characterization of the product. The CPS states what Zilog knows about this product at this time, but additional features or non-conformance with some aspects of the CPS may be found, either by Zilog or its customers in the course of further application and characterization work. In addition, Zilog cautions that delivery may be uncertain at times, due to start-up yield issues.

Low Margin:

Customer is advised that this product does not meet Zilog's internal guardbanded test policies for the specification requested and is supplied on an exception basis. Customer is cautioned that delivery may be uncertain and that, in addition to all other limitations on Zilog liability stated on the front and back of the acknowledgement, Zilog makes no claim as to quality and reliability under the CPS. The product remains subject to standard warranty for replacement due to defects in materials and workmanship.

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