Z9952

3.3V, 180MHz, Multi-Output Zero Delay Buffer

Product Features

- 180MHz Clock Support
- 150ps Maximum Output to Output Skew
- Supports PowerPC™, Intel and RISC Processors
- 11 Clock Outputs: Frequency Configurable
- Outputs Drive up to 22 Clock Lines
- LVCMOS/LVTTL Compatible Inputs
- Output Tri-state Control
- Spread Spectrum Compatible
- 3.3V Power Supply
- Pin Compatible with MPC952
- Industrial Temp. Range: -40°C to +85°C
- 32-Pin TQFP Package

Block Diagram

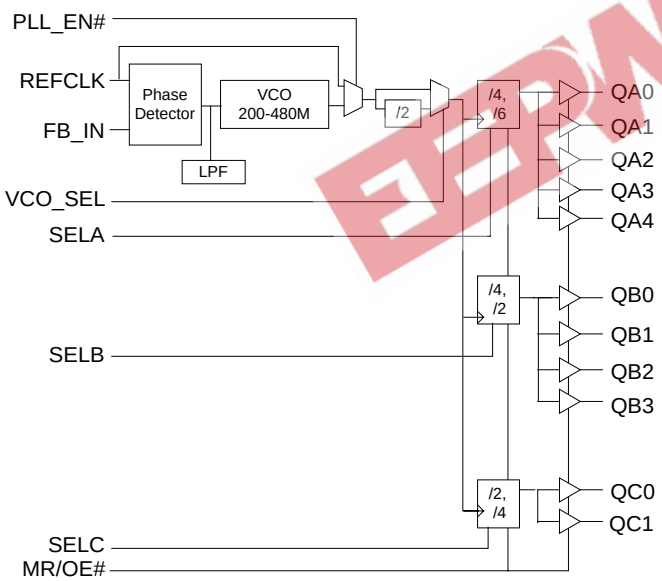


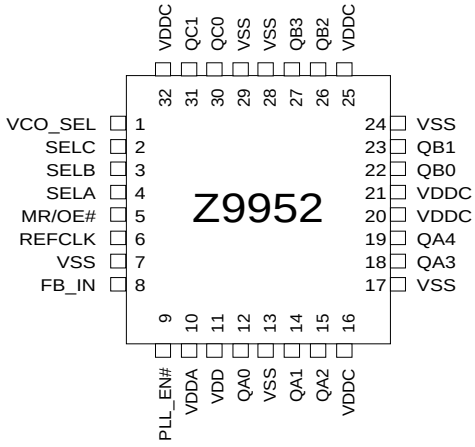
Figure 1

Frequency Table

VCO_SEL	SEL (A:C)	QA(0:4)	QB(0:3)	QC (0,1)
0	000	VCO/4	VCO/4	VCO/2
0	001	VCO/4	VCO/4	VCO/4
0	010	VCO/4	VCO/2	VCO/2
0	011	VCO/4	VCO/2	VCO/4
0	100	VCO/6	VCO/4	VCO/2
0	101	VCO/6	VCO/4	VCO/4
0	110	VCO/6	VCO/2	VCO/2
0	111	VCO/6	VCO/2	VCO/4
1	000	VCO/8	VCO/8	VCO/4
1	001	VCO/8	VCO/8	VCO/8
1	010	VCO/8	VCO/4	VCO/4
1	011	VCO/8	VCO/4	VCO/8
1	100	VCO/12	VCO/8	VCO/4
1	101	VCO/12	VCO/8	VCO/8
1	110	VCO/12	VCO/4	VCO/4
1	111	VCO/12	VCO/4	VCO/8

Table 1

Pin Configuration



Pin Description

PIN	NAME	PWR	I/O	Description
6	**REFCLK**		I	External Test Clock Input.
12, 14, 15, 18, 19	**QA(0:4)**	VDDC	O	Clock Output. See Frequency Table.
22, 23, 26, 27	**QB(0:3)**	VDDC	O	Clock Output. See Frequency Table.
30, 31	**QC(0,1)**	VDDC	O	Clock Outputs. See Frequency Table.
8	**FB_IN**		I	Feedback Clock Input. Connect to an output for normal operation.
1	**VCO_SEL**		I, PD	VCO Divider Select Input. When set high, the VCO output is divided by 2. When set low, the divider is bypassed. See Table 1
5	**MR/OE#**		I, PD	Master Reset/Output Enable Input. When asserted high, resets all of the internal flip-flops and also disables all of the outputs. When pulled low, releases the internal flip-flops from reset and enables all of the outputs.
9	**PLL_EN#**		I	PLL Enable Input. When asserted low, PLL is enabled. And when set high, PLL is bypassed.
2, 3, 4	**SEL(C:A)**		I, PD	Frequency Select Inputs. See Frequency Table. If SEL_ = 0, then QA, QB divider = ÷4, QC divider = ÷2 If SEL_ = 1, then QA divider = ÷6, QB divider = ÷2, QC divider = ÷4
16, 20, 21, 25, 32	**VDDC**			3.3V Power Supply for Output Clock Buffers.
10	**VDDA**			3.3V Power Supply for PLL
11	**VDD**			3.3V Power Supply for Core Logic
7, 13, 17, 24, 28, 29	**VSS**			Common Ground

PD = Internal Pull-Down

Maximum Ratings[1]

Maximum Input Voltage Relative to VSS: VSS - 0.3V
Maximum Input Voltage Relative to VDD: VDD + 0.3V
Storage Temperature: -65°C to + 150°C
Operating Temperature: -40°C to +85°C
Maximum ESD protection 2KV
Maximum Power Supply: 5.5V
Maximum Input Current: ±20mA

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, Vin and Vout should be constrained to the range:

VSS<(Vin or Vout)<VDD

Unused inputs must always be tied to an appropriate logic voltage level (either VSS or VDD).

DC Parameters

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Input Low Voltage	VIL	VSS	-	0.8	V	
Input High Voltage	VIH	2.0	-	VDD	V	
Input Low Current (@VIL = VSS)	IIL			10	µA	Note 2
Input High Current (@VIL =VDD)	IIH			120	µA	
Output Low Voltage	VOL			0.5	V	IOL = 20mA, Note 3
Output High Voltage	VOH	2.4			V	IOH = -20mA, Note 3
Quiescent Supply Current	IDDC	-	15	20	mA	All VDDC, VDDA, and VDD
PLL Supply Current	IDD	-	15	20	mA	VDDA only
Input Capacitance	Cin	-	-	4	pF	
VDDA = VDD = VDDC = 3.3V ±5%, TA = -40°C to +85°C						

Note 1: The voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.
Note 2: Inputs have internal pull-down resistors that affect input current.
Note 3: Driving series or parallel terminated 50Ω (or 50Ω to VDD/2) transmission lines.

AC Parameters[1]

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
Freq	Reference Input Frequency	Note 2		Note 2	MHz	
Fvco	PLL VCO Lock Range	200		480	MHz	
Tlock	Maximum PLL lock Time			10	ms	
Tr / Tf	Output Clocks Rise / Fall Time[4,5]	0.10		1.0	ns	0.8V to 2.0V
Fout	Maximum Output Frequency	-		180	MHz	QB, QC = (÷2)
				120		QA, QB, QC = (÷4)
				80		QA = (÷6)
FoutDC	Output Duty Cycle[4,5]	TCYCLE/2 – 750		TCYCLE/2 + 750	ps	
tpZL, tpZH	Output enable time (all outputs)	2		10	ns	
tpLZ, tpHZ	Output disable time (all outputs)	2		8	ns	
TCCJ	Cycle to Cycle Jitter (peak to peak)[5]		+/- 100		ps	
Tpd	REFCLK to FB_IN Delay[3,,4,5]	-200		200	ps	
TSKEW0	Any Output to Any Output Skew[4,5]	-		150	ps	Same frequencies
				250		Different frequencies
VDDA = VDD = VDDC = 3.3V +/- 5%, TA = -40°C to +85°C						

Note 1: Parameters are guaranteed by design and characterization. Not 100% tested in production. All parameters specified with loaded outputs.
Note 2: Maximum and minimum input reference is limited by the VCO lock range.
Note 3: The Tpd window is specified for a 50MHz input reference clock. The window will enlarge/reduce proportionally from the minimum limits with an increase/decrease of the input reference clock period.
Note 4: Driving series or parallel terminator 50Ω (or 50Ω to VDD/2).
Note 5: Outputs loaded with 30pF each

Description

The Z9952 has an integrated PLL that provides low skew and low jitter clock outputs for high performance microprocessors. The PLL is ensured stable operation given that the VCO is configured to run between 200 MHz to 480 MHz. This allows a wide range of output frequencies up to 180MHz. The Z9952 features three banks of individually configurable outputs: Bank A five outputs, Bank B four outputs, and Bank C two outputs. When MR/OE# input is set high, all the outputs are tri-stated. The Z9952 outputs are LVCMOS compatible and can drive two series terminated 50Ω transmission lines. With this capability the Z9952 has an effective fanout of 1:22. Low output-to-output skews make the Z9952 ideal for clock distribution in nested clock trees in the most demanding of synchronous systems.

The phase detector compares the input reference clock to the external feedback input. For normal operation, the external feedback input, FB_IN, is connected to one of the outputs. The internal VCO is running at multiples of the input reference clock set by SEL(A:C) select inputs, see Table 2. The VCO_SEL input allows for the choice of two VCO ranges to optimize PLL stability and jitter performance, see Table 1. The VCO frequency is then divided down to provide the required output frequencies. The use of even dividers ensures that the output duty cycle remains at 50%.

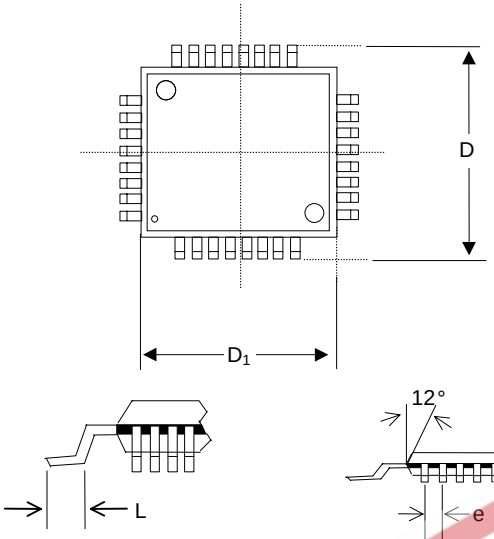
SELA	QA	SELB	QB	SELC	QC
0	÷4	0	÷4	0	÷2
1	÷6	1	÷2	1	÷4

Table 2

Zero Delay Buffer

When used as a zero delay buffer the Z9952 will likely be in a nested clock tree application. Any of the eleven outputs can be used as the feedback to the PLL. By using one of the outputs as a feedback to the PLL the propagation delay through the device is eliminated. The PLL works to align the output edge with the input reference edge thus producing a near zero delay. The reference frequency affects the static phase offset of the PLL and thus the relative delay between the inputs and outputs. Because the static phase offset is a function of the reference clock the Tpd of the Z9952 is a function of the configuration used.

Package Drawing and Dimensions



32 Pin TQFP Outline Dimensions

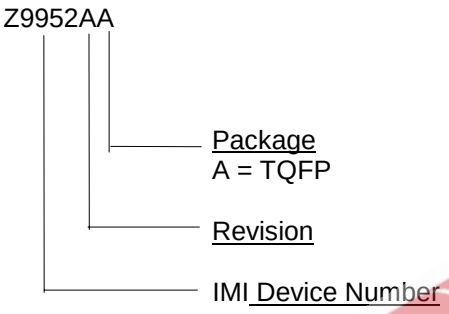
	INCHES			MILLIMETERS		
SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	0.047	-	-	1.20
A_1	0.002	-	0.006	0.05	-	0.15
A2	0.037	-	0.041	0.95	-	1.05
D	-	0.354	-	-	9.00	-
D_1	-	0.276	-	-	7.00	-
b	0.012	-	0.018	0.30	-	0.45
e	0.031 BSC			0.80 BSC		
L	0.018	-	0.030	0.45	-	0.75

Ordering Information

Part Number	Package Type	Production Flow
Z9952AA	32 PIN TQFP	Industrial, -40°C to +85°C

Note: The ordering part number is formed by a combination of device number, device revision, package style, and screening as shown below.

Marking: Example: Cypress
Z9952AA
Date Code, Lot #



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Document Title: Z9952 3.3V, 180 MHz Multi-Output Zero Delay Buffer **Document Number:** 38-07085				
Rev.	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	107121	06/05/01	IKA	Convert from IMI to Cypress
*A	108064	07/03/01	NDP	Changed Commercial to Industrial
*B	122770	12/22/02	RBI	Add power up requirements to maximum ratings information